

# 1.1-A, Single-Input, Single-Cell, Li-Ion Battery Charger With 50-mA LDO and 2.3-A Production Test Support

This user's guide describes the bq25040 evaluation module (EVM), how to setup the EVM to perform a stand-alone evaluation or interface with a system or host. The charger is designed to deliver up to 1.1 A of continuous current to the battery output in the adapter mode, ISET, or current limits the input to either 100 mA or 500 mA when in USB100/500 modes. The charge is programmed from the factory for 0.51 A in ISET mode. In the Protection Test Support (PTS) mode, the battery output is capable of delivering > 2.3 A of current for short pulses. The LDO regulator output can deliver up to 50 mA of current.

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## 1 Introduction

The bq25040 is an integrated Li-ion linear battery charger targeted at space-limited portable applications. It operates from either a USB port or ac adapter and charges a single-cell, Li-Ion battery with up to 1.1 A of charge current. The bq25040 has a single-power output that charges the battery. A system load can be placed in parallel with the battery. The charge current is programmed using the ISET and EN/SET inputs. The charge current is programmable to USB100, USB500, or a user-programmed charge current up to 1.1 A. Additionally, a 4.9-V, 3%, 50-mA LDO is integrated into the integrated circuit (IC) for supplying low-power external circuitry. The single-input interface (EN/SET) is used to select the charge current and to place the bq25040 into Production Test Mode (PTM). In PTM, the bq25040 operates as a linear regulator without a battery connected, where the output is regulated at 4.2 V and supplies up to 2.3 A to calibrate GSM transceivers.

The battery is charged in three phases: conditioning, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

The charger power stage and charge current sense functions are fully integrated. The charger function has accuracy current and voltage regulation loops, charge status display, and charge termination.

## 2 Considerations When Testing the bq25040 IC

The input current is regulated by the ISET loop or may be restricted by the USB current-limit circuitry when in either USB100 or USB500 mode.

The input connection to the LDO is connected upstream of the charge-sense circuit and is not part of the current-regulation or current-limit circuit. It is the designer's responsibility to ensure that excessive loading on the LDO output does not exceed USB specifications. The USB500 mode is set for a 400-mA current limit so that the LDO load does not cause the USB500 limit to be exceeded.

The LEDs can be run from any power source and are connected to the LDO from the factory. Moving the resistor from R20 to R21 connects the LEDs to the battery. Note that as the battery voltage decreases, the illuminated LED dims.

JMP6 is a connection to an onboard pulse generator circuit that can program the desired mode via pulses. Use only one shunt on JMP1 through JMP5 to program one through five pulses, respectively. The pulse generator always starts or stops in the low state, which leaves the IC in its active state. The part can only be programmed once unless it is reset by cycling power or removing JMP6. Removing JMP6 allows EN/SET to be pulled high and disables the IC. Reapplying the shunt to JMP6 pulls EN/SET low and enables the IC to the USB500 mode. Toggling switch S1 from the UP position to the DOWN position and back UP delivers the program pulse(s) to the IC.

## 3 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input dc voltage, $V_{IN}$	In recommended voltage range	4.75	5	6.5	V
Reduced performance range, $V_{in}$	Voltage outside recommended range <sup>(1)</sup>	3.5		30	V
Power dissipation	$P_{diss} = (V_{IN} - V_{out})^{(1)} I_{out}^{(2)}$			1.5	W
$I_{OUT}$	R1 = 1k		0.5	0.8	A

(1) Input voltage range is specified for normal operation. Input voltage between UVLO and 4.75 V has limitations and may have some functionality, but does not damage the IC nor present any safety issue with the battery. Input voltage above OVP and less than 30 Vdc has no operation and will not damage the IC. Lower input voltage (closer to dropout operation) produces less heat dissipation and potentially better performance.

(2) The junction temperature rise above ambient is proportional to the power dissipation. Once the junction temperature reaches ~125°C, thermal regulations reduces the charge current when not in PTS mode.

## 4 Test Summary

This section covers the setup and tests performed in evaluating the EVM.

### 4.1 Equipment

- Power supply +5.1  $\pm$ 0.1 V, current limit set to 1.5  $\pm$ 0.1 A
- Battery: 4.2 V LiCoO2 or equivalent
- LDO Load: from 100- $\Omega$  to 10k- $\Omega$  resistor
- Three Fluke 75 DMMs (equivalent or better)
- Oscilloscope, Model TDS220 (equivalent or better)

### 4.2 Equipment and EVM Setup

- Preset P/S#1 to 5.1  $\pm$ 0.1 V, 1.5  $\pm$ 0.1-A current limit, turn off and connect to J1 (+ to IN and - to GND).
- Connect a fully discharged battery to J2 (+ to BAT+ and - to BAT-).
- Apply a 1-k $\Omega$  load resistor to J3-1/2.
- Apply shunt jumpers to JMP1, JMP6, JMP7, and JMP8.
- Set switch, SW1, in the UP position.
- Adjust R7 fully CW, and then back off four turns CCW.
- Connect the DMMs and oscilloscope as shown in [Figure 1](#), if desired.

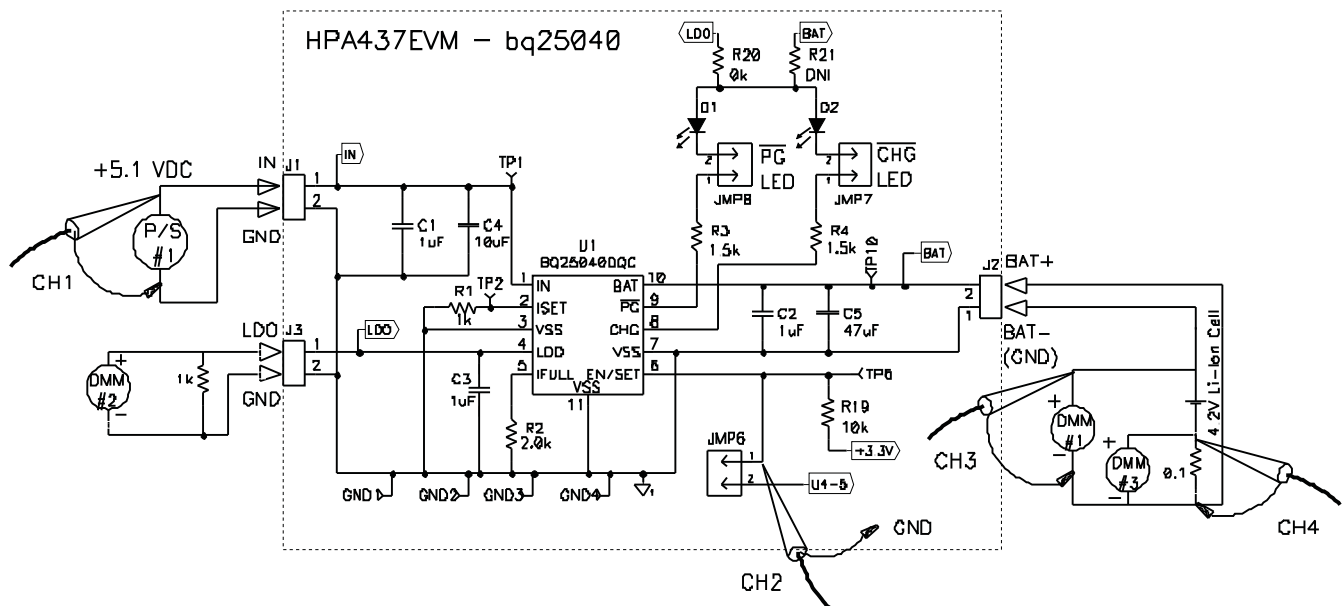
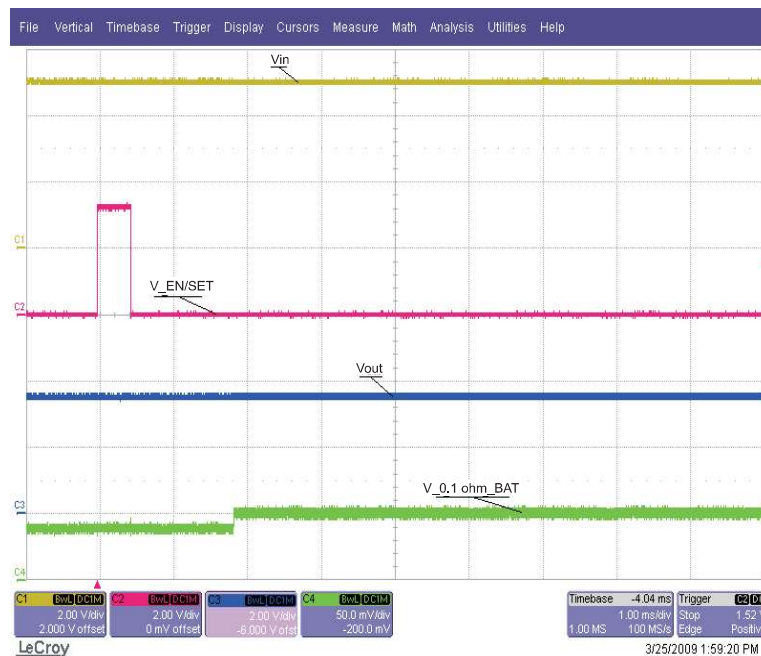


Figure 1. Evaluation Setup Charging Circuit Shown; Pulse Programming Circuit not Shown

### 4.3 Test Procedure

1. Make sure setup procedure was followed.
2. Turn on P/S#1; preset to 5.1 Vdc.
3. Verify that the PG (D1) and CHG (D2) LEDs turned on. Verify that the input/output current is around  $\sim$ 0.4 A (DMM3 is  $\sim$ 40 mV). This is the power-up USB500 default mode (no programming pulses have been delivered yet) and typically delivers up to  $\sim$ 400 mA. The charge current limit is set lower than 500 mA to ensure that the total charge and LDO (maximum of 50 mA) current do not exceed 500 mA on the input.
4. Set the scope to trigger off of CH2 (positive trigger, 1 ms/div), to capture the program pulse going to (EN/SET TP6). Note that only one shunt at a time should be placed on JMP1 through JMP5 to select the desired number of programmed pulses.

5. Switch, S1, DOWN, then back UP. The scope captures one pulse on CH2 (Figure 2). The pulse must be less than 1.5-ms wide. If too wide, the potentiometer, R7, can adjust the pulse width.
6. Verify that the input current changes from 0.4 A to 0.51 A (one pulse programmed the IC for ISET mode). The ISET resistor, 1 k $\Omega$ , programs the ISET mode to  $\sim$ 0.51 A. Note that the IC can only be programmed once. If a different program level is desired, the part must be reset by cycling power or pulling EN/SET high to disable the IC.
7. Remove shunt JMP6, and verify that the input current goes to zero. Removing the shunt, JMP6, allows EN/SET to be pulled up. This disables the charge and allows programming to be done once EN/SET is pulled back low by replacing the shunt JMP6.
8. Replace shunt on JMP6, and move shunt on JMP1 to JMP2 (two-pulse programming). The charger returns to the USB500 mode, delivering  $\sim$ 400 mA. If the IC comes up in a different mode, then while placing the shunt on JMP6, a contact bounce occurred and the IC was programmed. Remove and replace the shunt if this happens.
9. Switch, S1, DOWN, then UP to program charger to USB100 mode (Figure 3).
10. This procedure can be repeated (steps 7 to 9) for the shunt on any jumper JMP1 through JMP5 to program one to five pulses, respectively. Note that programming three pulses puts the IC in PTS mode and delivers  $>$  2.3 A if the source current is available and the load is great enough. This mode is intended for production testing without a battery. If a less-than-full battery is connected, the current may exceed the recommended charge current of the battery or the charger circuit. For maximum current, the duty cycle must be less than 20% and for no longer than 10 ms. See the data sheet for programming information (SLUS910).
11. Verify that the LDO output voltage on DMM#2 measures  $\sim$ 4.9 Vdc, 0.1 V.
12. Allow battery to charge to full and verify that D2 LED turns off.
13. Discharge battery below 4.1 V, and verify that the charging is enabled and the D2 CHG LED is off for the second and subsequent charges.
14. Figure 4 shows the power up and timing of the Stat pins and charge current.



**Figure 2. One-Pulse Programming Shows Change From USB500 to ISET Mode**

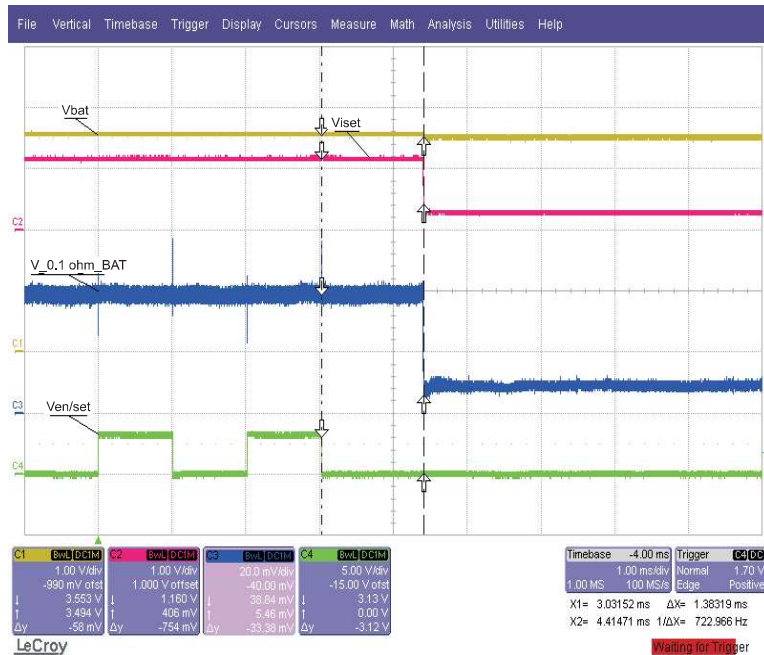


Figure 3. Two-Pulse Programming Shows Timing of Program Change From 0.4 A to 0.1 A

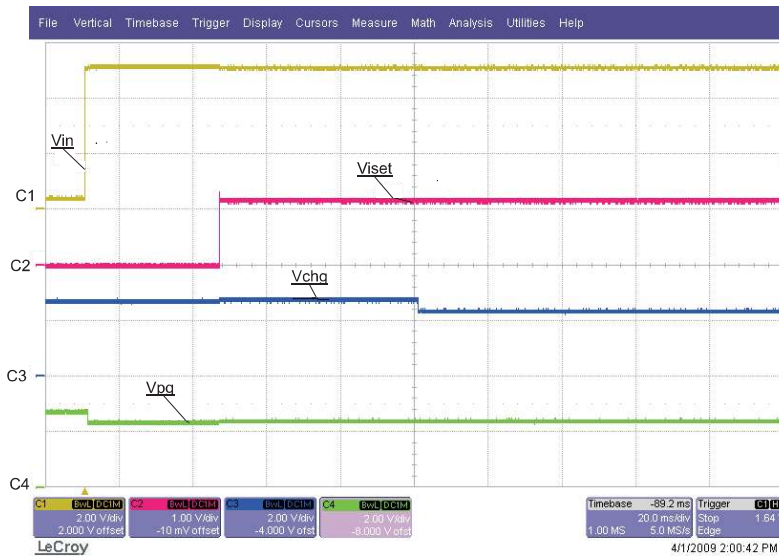
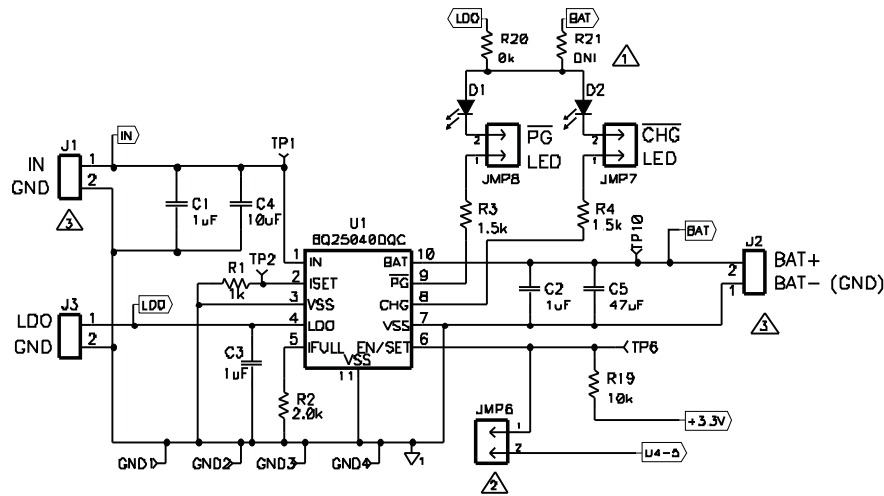


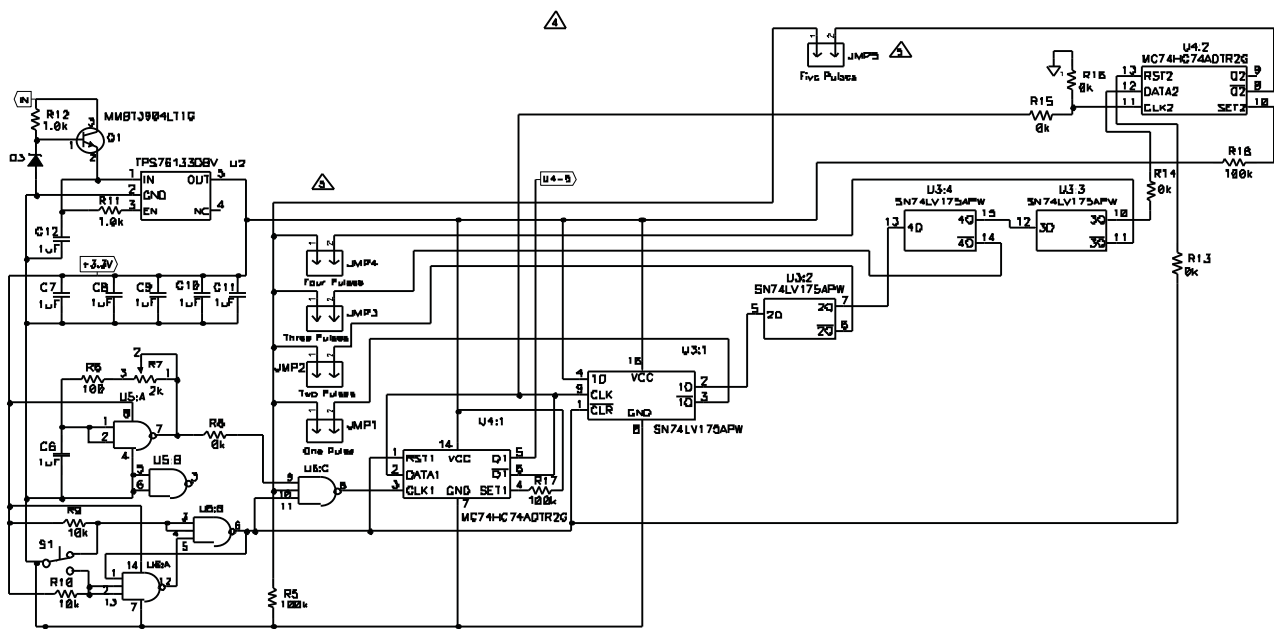
Figure 4. Power-Up Sequence Shows Timing Between  $V_{in}$ ,  $V_{iset}$ ,  $V_{pg}$ , and  $V_{chg}$ . C1: Chg @ JMP1; C4: PG @ JMP8; LEDs Pulled Up to 4.15-V Battery

5 Schematics



- ⚠ Do not install R21. R20 is the LDO pull-up for the LEDs. To pull up LEDs to BAT, remove R20 and place an R21.
- ⚠ Sheet 2 contains the hardware circuit that delivers the pulses to program the charge current. This is provided so the IC can be evaluated on a stand-alone basis. An external host can be used, instead of this circuit, by removing the shunt on JMP6 and connecting the host control signal to JMP6-1 and the return to any ground connection on the EVM
- ⚠ There is only one ground plane, therefore GND is the same as BAT-  
 J1-IN Voltage Range: 4.4V to 12V (Charge is disabled if OVP is reached)  
 J2-BAT+ Output regulates at 4.2V or Current Regulates (programmable) up to 0.8A.

Figure 5. Basic EVM Charger Circuit



- ⚠ The circuit on this sheet is typically not part of the charger design. This circuit generates the pulses to program the charge, which is normally done by the host.
- ⚠ Use only one Shunt on JMP1 through 5. Place shunt according to desired program pulses.

Figure 6. Circuit for Programming Pulse (Typically Done by Host)

6 Layout

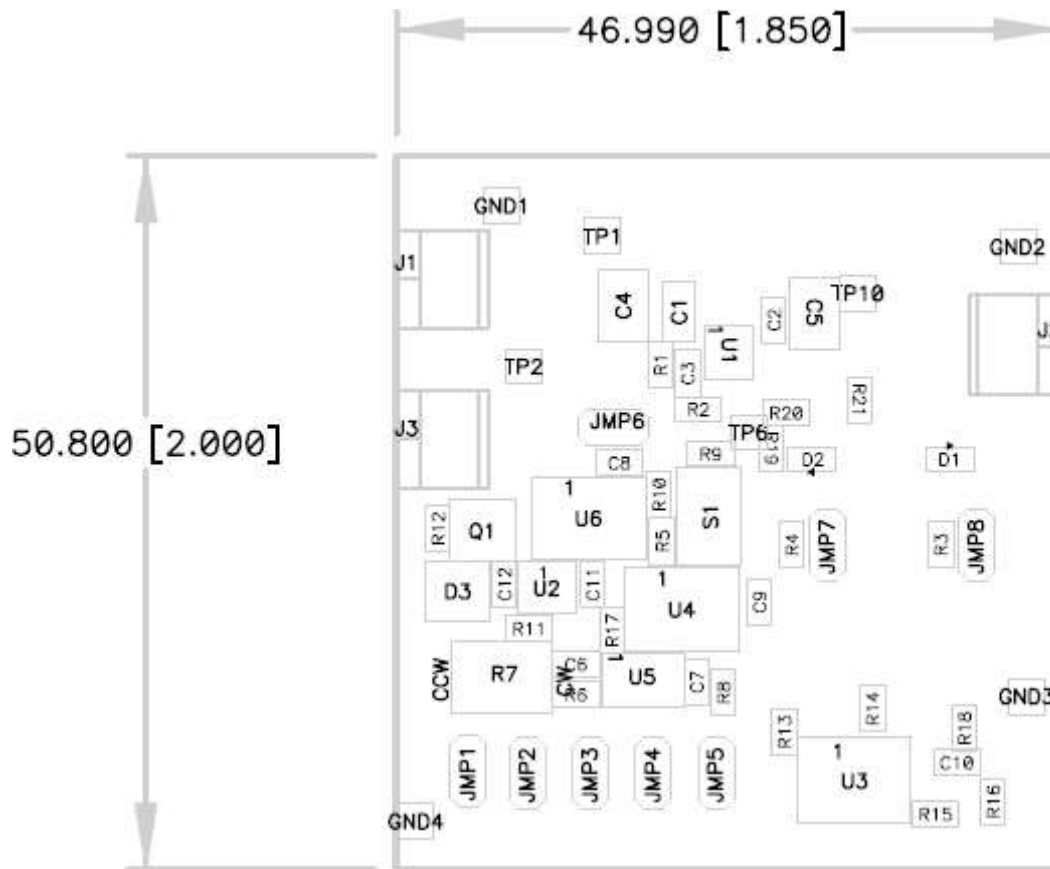


Figure 7. Assembly Layer

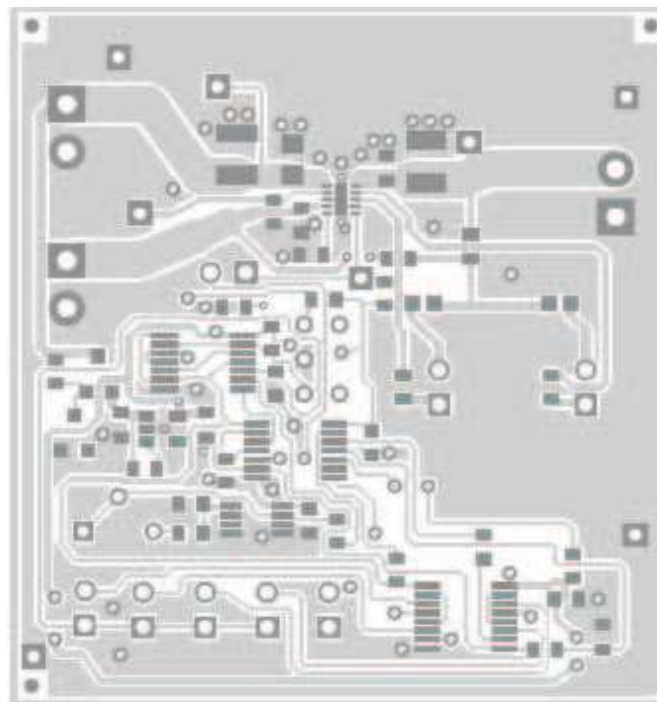
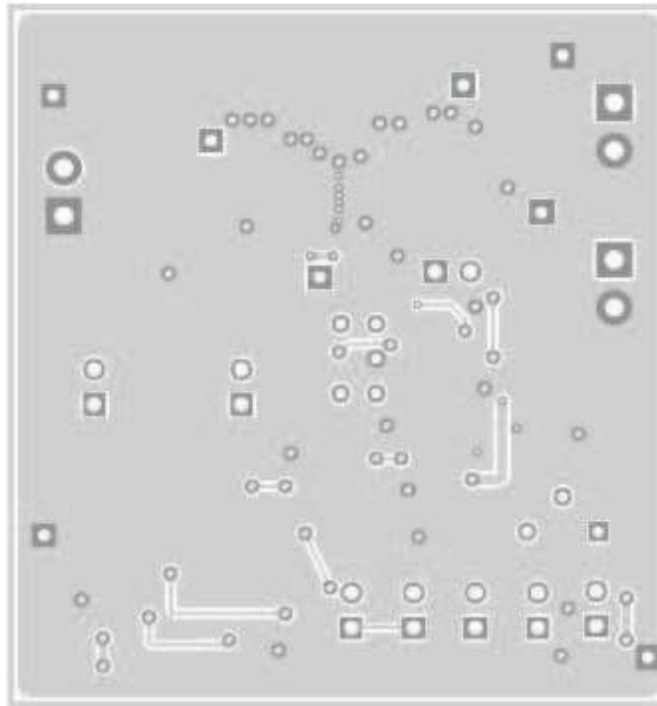


Figure 8. Top Copper Layer


**Figure 9. Bottom Copper Layer Bottom View**

## 7 Bill of Materials

**Table 1. HPA437A Bill of Materials - bq25040**

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	1 F	Capacitor, Ceramic, 25V, X5R, 10%	0805	ECJ-2FB1E105K	Panasonic
9	C2, C3, C6C12	1 F	Capacitor, Ceramic, 10V, X5R, 10%	0603	ECJ-1VB1A105K	Panasonic
1	C4	10 F	Capacitor, Ceramic, 25V, X5R, 10%	1210	ECJ-3YB1E106K	Panasonic
1	C5	47 F	Capacitor, Ceramic, 10V, XR5, 20%	1210	ECJ-4YB1A476M	Panasonic
2	D1, D2	LTST-C190GKT	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	0603	LTST-C190GKT	Lite On
1	D3	BZX84C10LT1G	Diode, Zener, 10-V, 350-mW	SOT-23	BZX84C10LT1G	On Semi
4	GND1 GND4	BLK	Test Point, 0.032 Hole		5011	Keystone
3	J1J3	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 0.25 inch	ED555/2DS	OST
8	JMP1JMP8	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch 2	PTC36SAAN	Sullins
1	Q1	MMBT3904LT1G	Bipolar, NPN, 40-V, 200-mA, 225-mW	SOT23	MMBT3904LT1G	On Semi
1	R1	1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R12	1.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R21	DNI	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	1.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R5, R17, R18	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	100	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	2k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	2k	Potentiometer, 1/4 in. Cermet, 12-Turn, Top-Adjust	0.25 0.17	3266W-202	Bourns
6	R8, R13R16, R20	0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R9, R10, R19	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std



**Table 1. HPA437A Bill of Materials - bq25040 (continued)**

Count	RefDes	Value	Description	Size	Part Number	MFR
1	S1	G12AP	Switch, ON-ON Mini Toggle	0.28 0.18 inch	G12AP	NKK
4	TP1, TP2, TP6, TP10	WHT	Test Point, 0.032 Hole		5012	Keystone
1	U1	BQ25040DQC	IC, 1.2A, Single-Input, 1 Cell Li-Ion CHARGER	TDFN-10	BQ25040DQC	TI
1	U2	TPS76133DBV	IC, Low-Power 100 mA LDO Regulator	SOT23-5	TPS76133DBV	TI
1	U3	SN74LV175APW	IC, Quad D-Flip Flop with Clear	TSSOP	SN74LV175APW	TI
1	U4	MC74HC74ADTR2G	IC, Dual D Flip Flop with Set and Reset	TSSOP	MC74HC74ADTR2G	On Semi
1	U5	SN74LVC2G132DCTR	IC, Dual 2-Input NAND Gate With Schmitt-Trigger Inputs	SSOP-8	SN74LVC2G132DCTR	TI
1	U6	SN74HC10QPWREP	IC, Triple 3-Input Positive NAND Gate	TSSOP	SN74HC10QPWREP	TI
4		929950-00	Shunts	100 mill	Black	3M
1			PCB, 1.9 In 2 In 0.031 In		HPA437	Any

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### EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 30 V and the output voltage range of 0 V to 4.25 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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