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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

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SH7264 CPU Board

M3A-HS64

User's Manual

Renesas 32-bit RISC Microcomputer
SuperH™ RISC engine Family/SH7260 Series

Renesas Electronics
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Rev.1.00 2009.04

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Chapter 1
Overview

1.1 Introduction

The SH7264 CPU board and its optional boards are designed for evaluating the features and performance of the SH7264 Group of Renesas Technology original microcomputers (MCUs), as well as for developing and evaluating application software for these MCUs. Following are features of the SH7264 CPU board and optional boards.

1.1.1 SH7264 CPU board (Part number: M3A-HS64)

The M3A-HS64 comes standard with 4-MB NOR flash memory (16-bit bus width), 16-MB SDRAM (16-bit bus width), 256-MB NAND flash memory (16-bit bus width) and 2-MB serial flash memory as its external memory. The M3A-HS64 has three boot options;

- Boot from NOR flash memory
- Boot from NAND flash memory
- Boot from serial flash memory

The M3A-HS64 comes standard with an RS-232C connector and a USB connector as the SH7264 peripheral interfaces.

The USB connector on the M3A-HS64 is a Series-A receptacle. The wiring pattern on the M3A-HS64 allows for connecting a Mini-B receptacle to evaluate the USB host and function modules.

The SH7264 data bus, address bus and internal peripheral pins are connected to expansion connectors on the M3A-HS64 to allow for timing evaluation with peripherals using measurement instruments, and the development of the optional board according to its application.

The Renesas Technology E10A-USB on-chip emulator (AUD trace enabled: 36-pin, AUB trace disabled: 14-pin) can be connected to the M3A-HS64.

1.1.2 Optional board for audio (Part number: M3A-HS64G01)

The M3A-HS64G01 is an evaluation board suitable for advance development of the audio system, which comes standard with an audio interface, CD deck interface and character LCD module connector.

Also, it comes with two channels of a D/A converter for audio output, and one channel of a D/A converter and an A/D converter for audio input and output as its audio interfaces.

It also comes standard with an LCD module interface connector, a UART interface connector, a CAN (Controller Area Network) connector, an IEBus™ connector, an IIC connector, and an SD card connector.

1.1.3 Optional board for graphic display (Part number: M3A-HS64G02)

The M3A-HS64G02 is an evaluation board, which comes standard with a video input interface, an audio interface and an LCD module interface for developing the video processing or music-playing applications.

All PWM output pins and timer output pins are inserted into connectors to allow for developing the automotive meter or brightness-control applications.

It comes standard with a CAN connector, an IEBus™ connector, an IIC connector and an SD card connector.

1.2 M3A-HS64 Configuration

The following figure shows an example of the system configuration using the M3A-HS64.

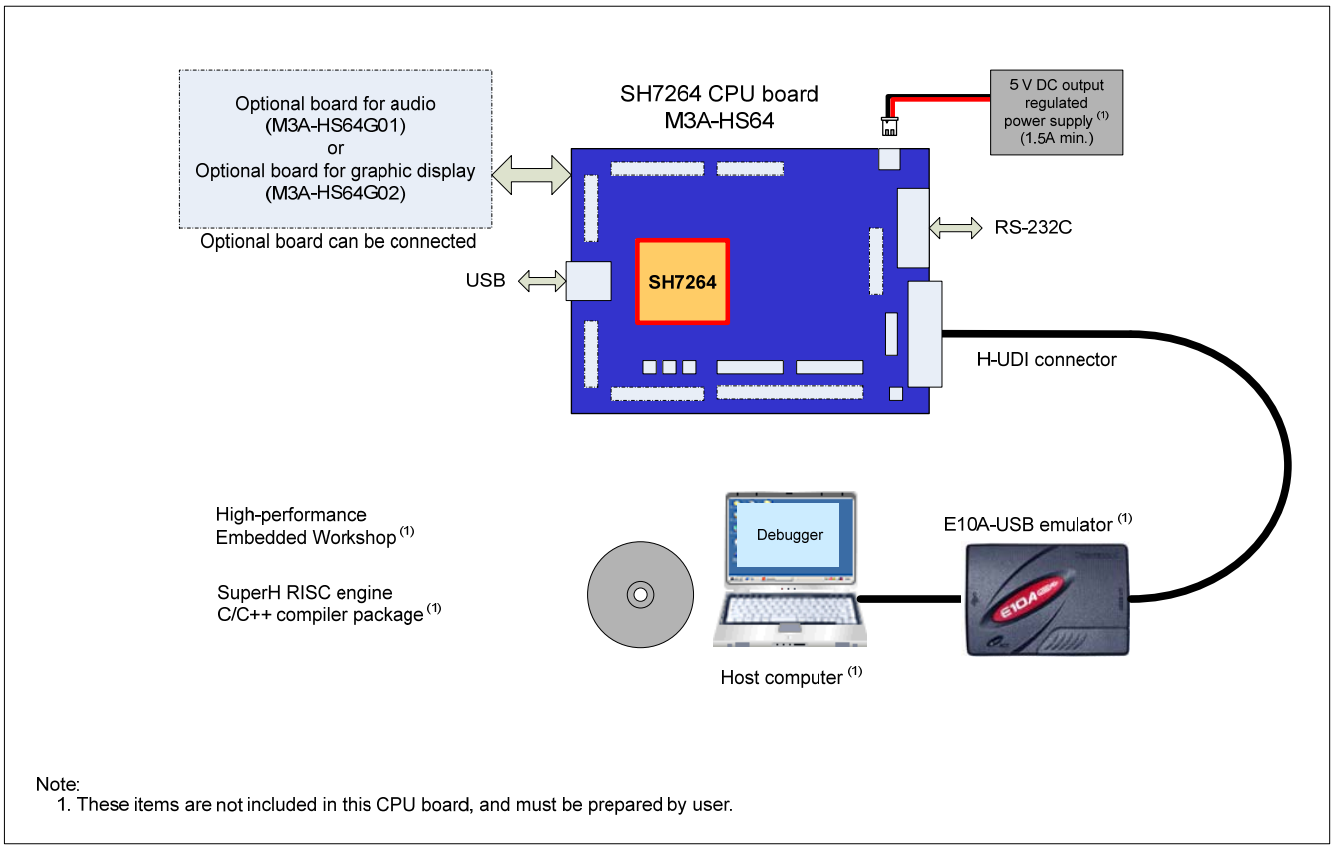


Figure 1.2.1 M3A-HS64 System Configuration Example

1.3 M3A-HS64 Board Specifications

Table 1.3.1 and Table 1.3.2 describe the board specifications of the M3A-HS64.

Table 1.3.1 Board Specifications (1/2)

No.	Item	Description
1	CPU	• SH7264 ・Input (XIN) clock: 18 MHz ・Bus clock: 72 MHz at maximum ・CPU clock: 144 MHz at maximum ・Internal memory Hi-speed internal RAM: 64 KB Large-capacity internal RAM: 1 MB Instruction cache: 8 KB Operand cache: 8 KB ・Power supply voltage: internal - 1.2 V, I/O - 3.3 V ・208-pin QFP, 0.5 mm pitch (package code: PLQP0208KB-A)
2	External memory	• SDRAM: 16 MB ・EDS1216AHTA-75E: 1 (Elpida) • NOR flash memory: 4 MB ・S29GL032N90TFI020: 1 (SPANSION) • NAND flash memory: 256 MB ・K9F2G08U0A-PCB0: 1 (Samsung) • Serial flash memory: 2 MB ・AT26DF161A-SU: 1 (ATMEL) • EEPROM: 16 KB ・HN58X24128FPIE: 1 (Renesas)
3	USB	• USB Series-A receptacle (Mini-B receptacle is optional)
4	Connectors and through-holes	• H-UDI connector (36-pin or 14-pin) • RS-232C connector (D-sub 9-pin) • 20-pin MIL-spec connectors ・SH7264 expansion connectors: 6 (Ports A, C to F, H, J, and K) • 30-pin MIL-spec connectors ・SH7264 expansion connectors: 2 (Ports B and G) • 40-pin MIL-spec connector ・SH7264 expansion connector: 1 (Ports E, F, and K)
5	LEDs	• Power supply LED: 1 • User LEDs: 2 (connected to the SH7264 I/O pins)
6	Switches	• Reset switch: 1 • NMI switch: 1 • IRQ1 switch: 1 • TEST switch: 1 • System setting DIP switches: 6/package • User DIP switches: 6/package

Table 1.3.2 Board Specifications (2/2)

No.	Item	Description
7	Board specifications	• Dimensions: 148 mm x 105 mm • Mounting form: 6 layers, double-sided • Board thickness: 1.6 mm • Number of boards: 1

1.4 M3A-HS64 Exterior

The following figure shows the exterior of the M3A-HS64.

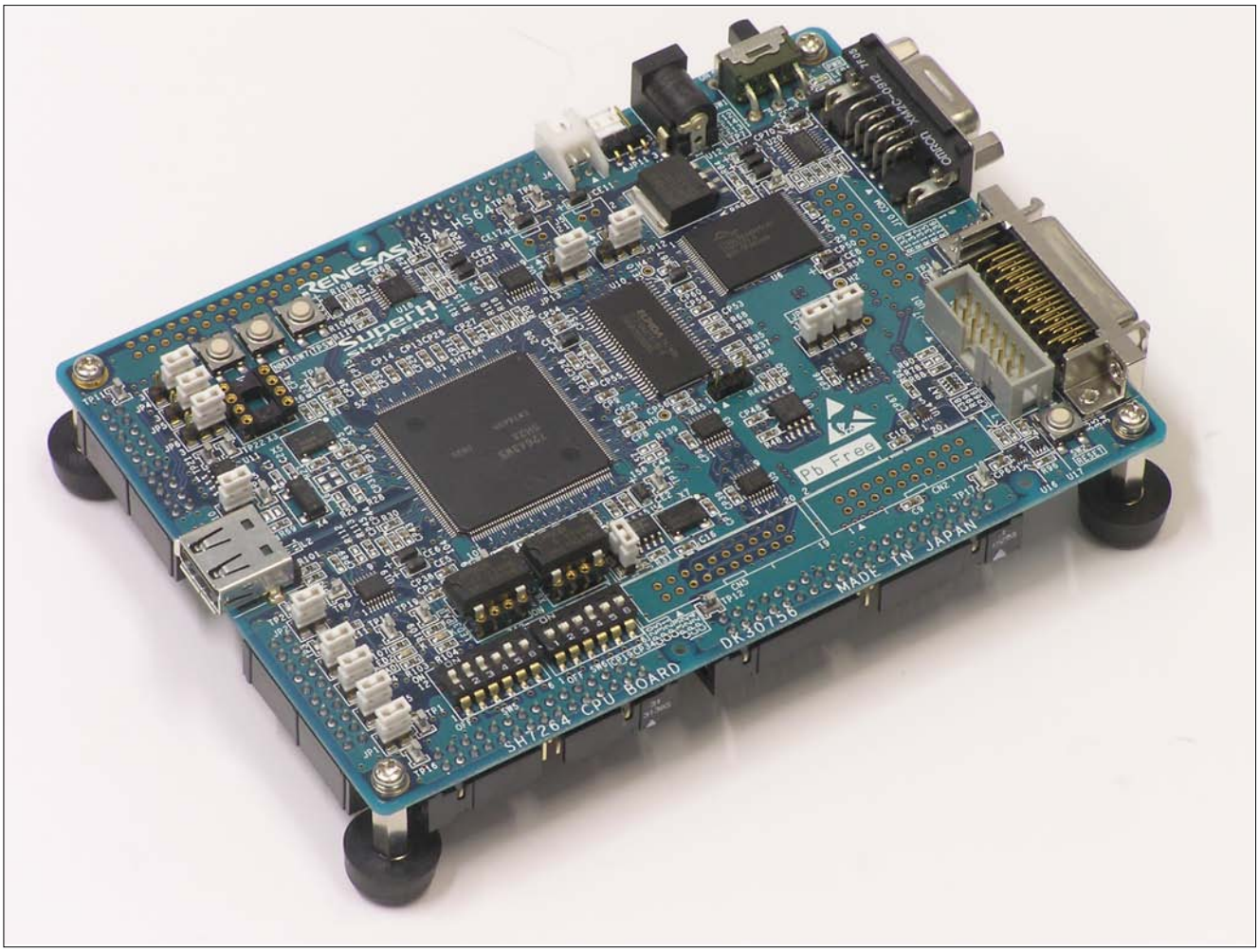


Figure 1.4.1 SH7264 CPU board Exterior

1.5 M3A-HS64 Block Diagram

The following figure shows the system block diagram of the M3A-HS64.

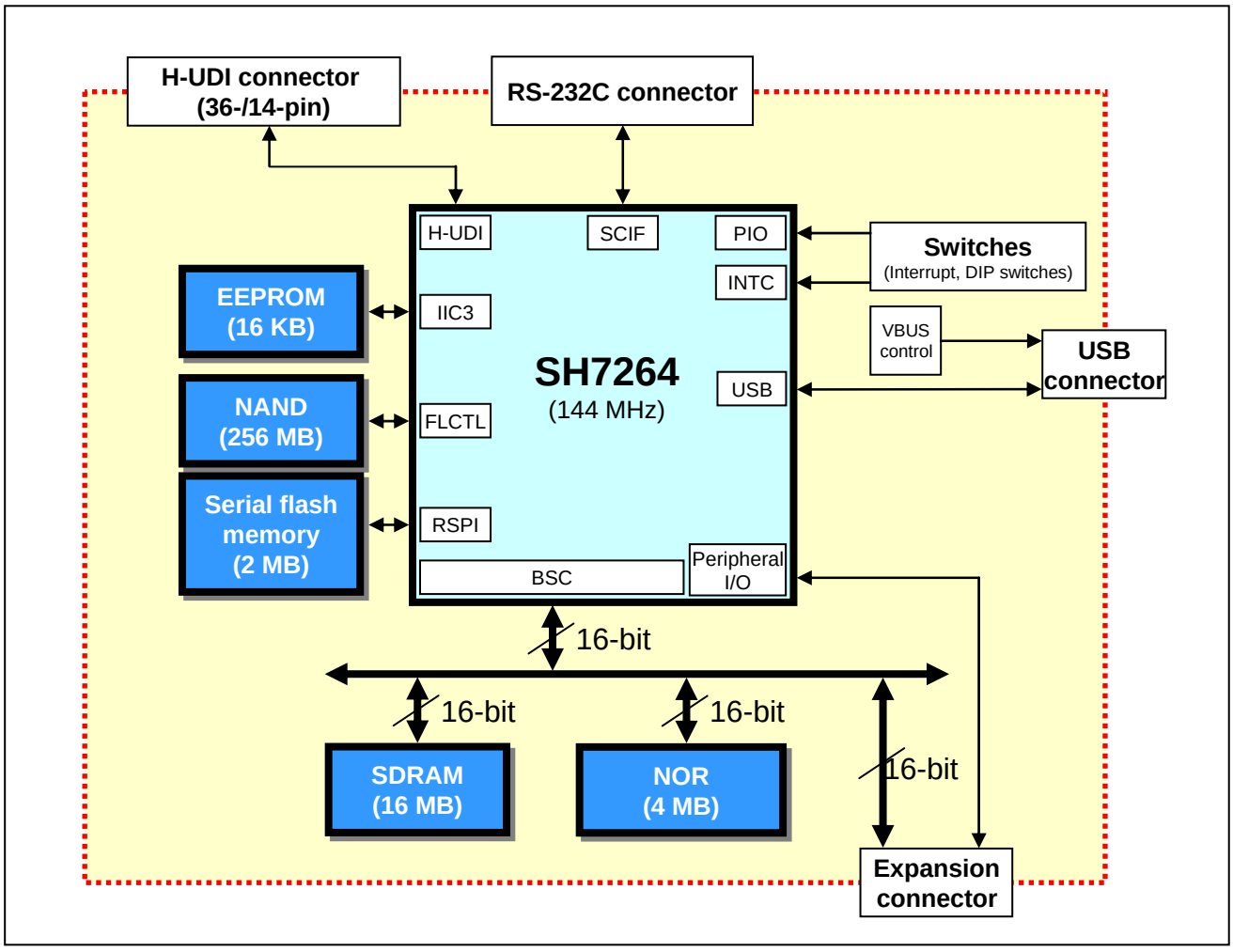


Figure 1.5.1 M3A-HS64 System Block Diagram

1.6 M3A-HS64 Major Components

Figure 1.6.1 and Figure 1.6.2 show the M3A-HS64 layout and locations of the major components (PCB drawing).

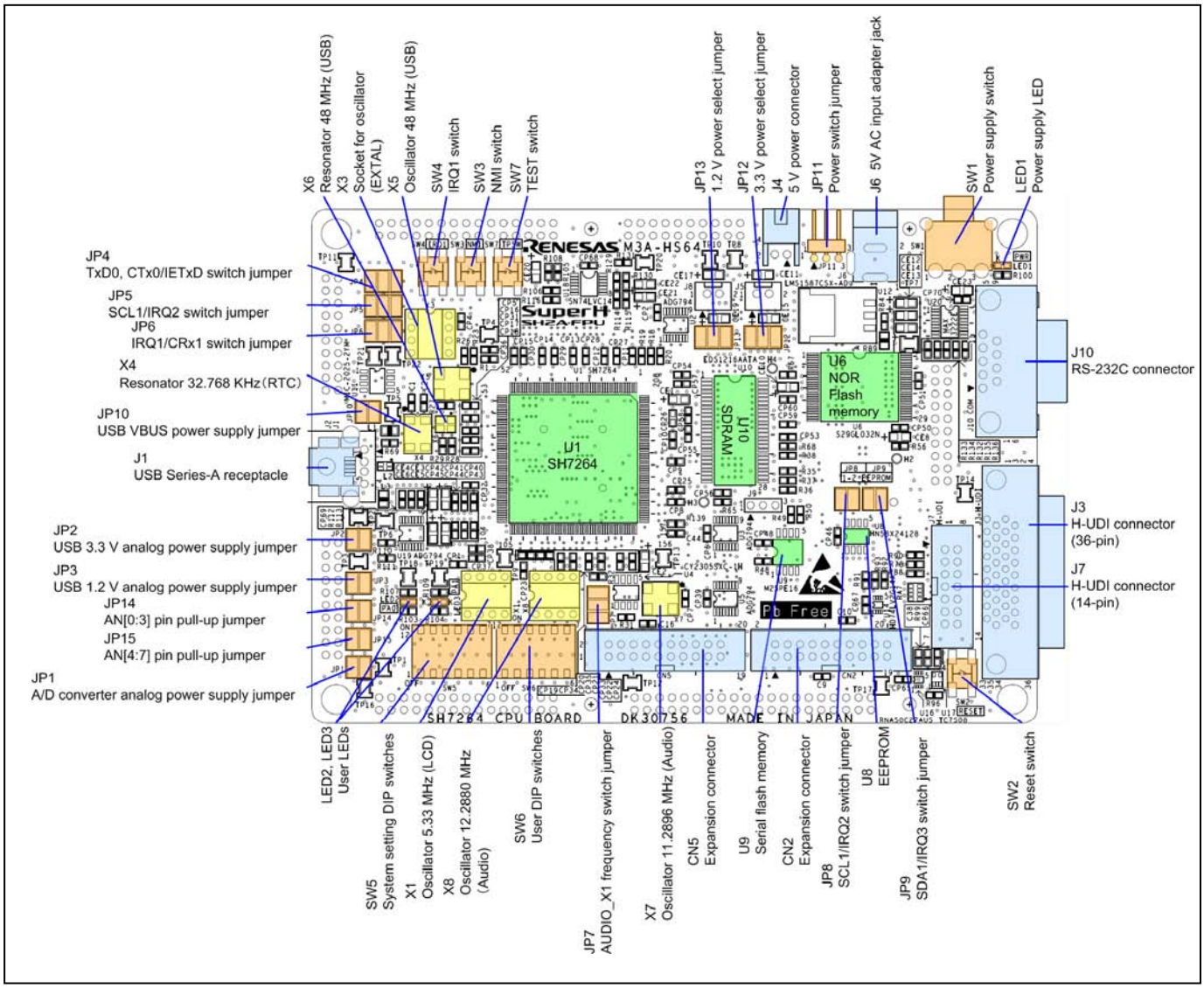


Figure 1.6.1 M3A-HS64 Component Layout and Placement (Top View of the Component Side)

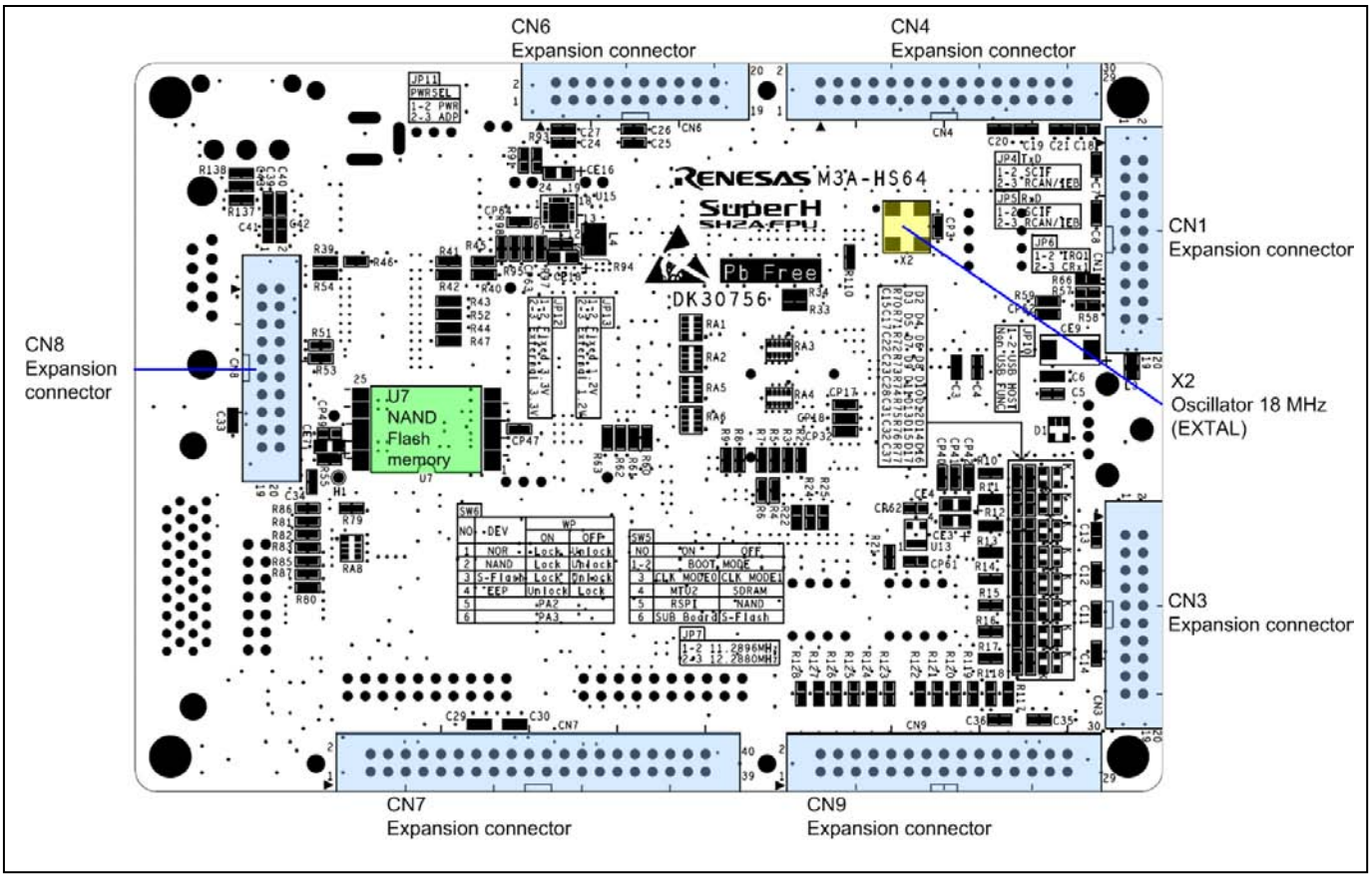


Figure 1.6.2 M3A-HS64 Layout and Component Placement (Top View of the Solder Side)

The following tables list the major components on the M3A-HS64.

Table 1.6.1 Major components on the M3A-HS64 - ICs (1/3)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	MCU	R5S72643P144FPU	Renesas	Main MCU	1
2	SDRAM	EDS1216AHTA-75E	ELPIDA	16-bit bus, 16 MB	1
3	NOR Flash memory	S29GL032N90TFI020	SPANSION	16-bit bus, 4 MB	1
4	NAND Flash memory	K9F2G08U0A-PCB0	SAMSUNG	8-bit bus, 256 MB	1
5	Serial Flash memory	AT26DF161A-SU	ATMEL	4-wire serial, 2 MB	1
6	EEPROM	HN58X24128FPIE	Renesas	2-wire serial 16 KB	1
7	Reset IC	RNA50C27AUS	Renesas		1
8	RS-232C driver	MAX3222ECUP	MAXIM		1
9	Adjustable regulator	LMS1587CSX-ADJ	NS	3.3 V	1
10	Adjustable regulator	R2A20101NP	Renesas	1.2 V	1
11	Voltage reference	LM4132AMF-3.3	NS	Reference power supply for ADC	1
12	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	4

Table 1.6.2 Major components on the M3A-HS64 - Connectors (2/3)

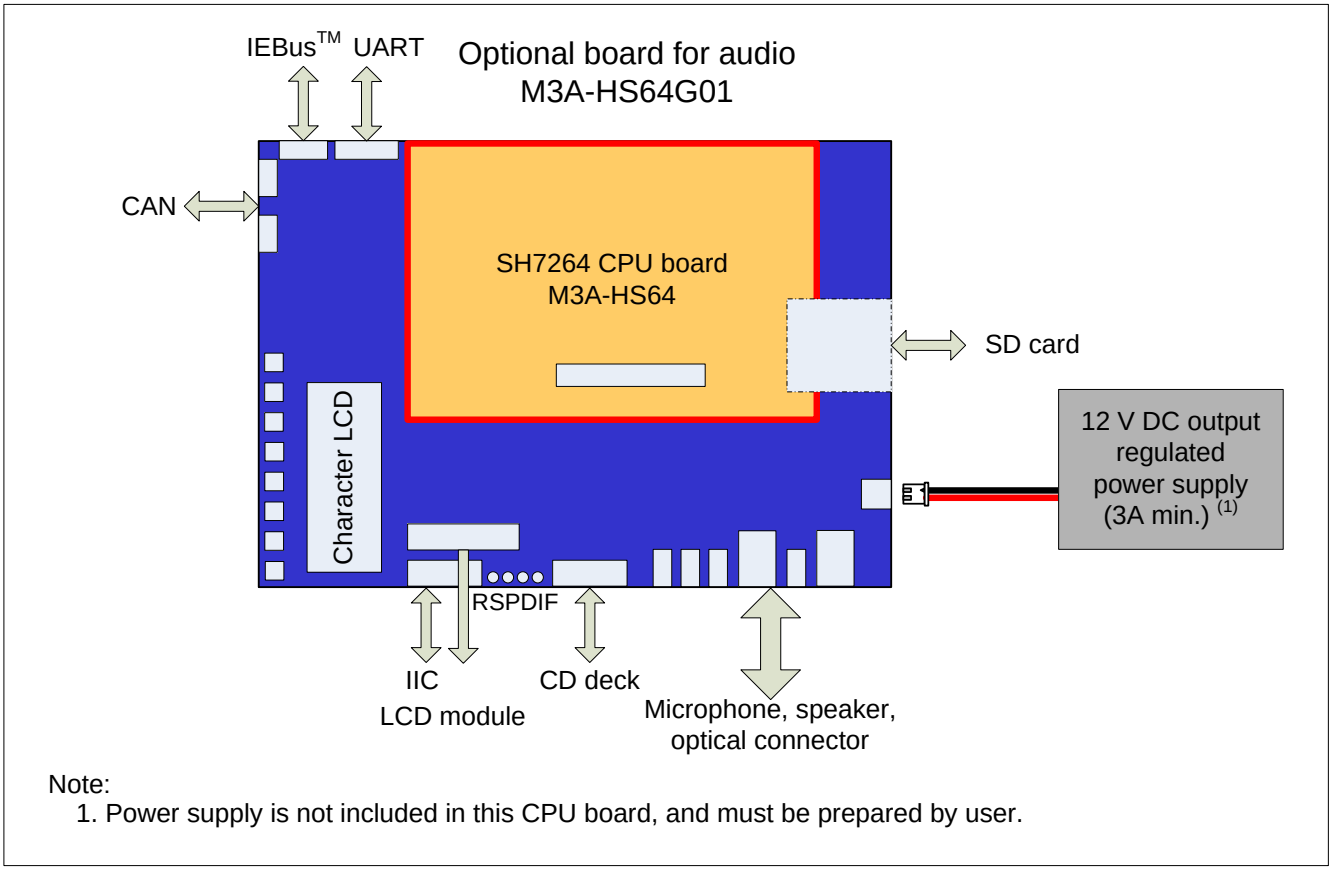
No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	36-pin H-UDI connector	DX10M-36SE	HRS		1
2	14-pin H-UDI connector	7614-6002	3M		1
3	RS-232C connector	XM2C-0942-132L	OMRON	D-sub 9-pin	1
4	20-pin expansion connectors	XG4C-2031	OMRON	20-pin MIL-spec connector	6
5	30-pin expansion connectors	XG4C-3031	OMRON	30-pin MIL-spec connector	2
6	40-pin expansion connector	XG4C-4031	OMRON	40-pin MIL-spec connector	1
7	DIP switches (6/package)	A6S-6104-H	OMRON	System setting and user DIP switches	2
8	USB Series-A receptacle	UBA-4R-D14T-4D	J.S.T	DIP type	1
9	USB Mini-B receptacle	54819-0572	MOLEX	Optional	0

Table1.6.3 Major components on the M3A-HS64 -USB and peripherals (3/3)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	USB power distribution switch	MIC-2025-2YM	MICREL	VBUS power control	1
2	Zener Diode	HZN6.2Z4MFA	Renesas	Optional	0
3	Ferrite Beads	BLM21PG600SN1	Murata	Optional	0
4	Common mode choke	DLW21HN900SQ2	Rohm	Optional	0

1.7 M3A-HS64G01 Configuration

The following figure shows an example of the system configuration using the M3A-HS64G01 (optional board for audio).



Note:
1. Power supply is not included in this CPU board, and must be prepared by user.

Figure 1.7.1 M3A-HS64G01 System Configuration Example

1.8 M3A-HS64G01 Board Specifications

The following table describes the board specifications of the M3A-HS64G01.

Table 1.8.1 Board Specifications

No.	Item	Description
1	LCD	Comes with following connecters to control an LCD module by the SH7264 on-chip Video Display Controller 3 (VDC3) • Flexible connectors for LCD module: 2 • MIL-spec connector for LCD module: 1 (30-pin)
2	Character LCD	Controls the character LCD module by the SH7264 on-chip general-purpose I/O ports • 16 x 2 semi-transmissive character LCD module with LED backlight: 1
3	Audio	Comes with audio codecs for audio input (AK4353) and audio input/output (AK4524) by the SH7264 on-chip Serial Sound Interface with FIFO (SSIF) • AK4353 (Asahi Kasei EMD Corporation): 2 ・96 KHz 24-bit DAC, on-chip digital audio transmitter ・Sampling frequency: 16 KHz to 96 KHz ・Stereo pin jacks: 2 ・Optical connectors: 2 • AK4524 (Asahi Kasei EMD Corporation): 1 ・24-bit stereo codec with microphone AMP ・Sampling frequency: 32 KHz to 48 KHz
4	CD deck	Inputs PCM data using the SH7264 on-chip SSIF and controls the CD deck by the Renesas Serial Peripheral Interface (RSPI) • Flexible connector for connecting a CD deck: 1
5	SD card interface	Accesses the SD card by the SH7264 on-chip SD host interface (SDHI) • SD card slot : 1 • Includes a card power control IC (Software control NOT allowed)
6	CAN	CAN (Controller Area Network) communication by the SH7264 on-chip CAN (RCAN-TL1) • HA13721FP (Renesas CAN driver IC), includes a voltage level shifter
7	IEBus™	IEBus™ communication by the SH7264 on-chip IEBus controller (IEB) • HA12187FP (Renesas IEBus driver IC), includes a voltage level shifter
8	UART interface	Connected to the SH7264 on-chip Serial Communication Interface with FIFO (SCIF) pin
9	IIC	Connected to the SH7264 on-chip IIC bus interface (IIC3) pin • MIL-spec connector for connecting an external IIC interface: 1 (20-pin)
10	Switches	Key input by the SH7264 on-chip A/D converter • Key input switches: 16 (4 switches x 4 inputs)
11	Board specifications	• Specifications: 210 mm x 148 mm • Mounting form: 4 layers, double-sided • Board thickness: 1.6 mm • Number of boards: 1 board

1.9 M3A-HS64G01 Exterior

The following figure shows the exterior of the M3A-HS64G01.

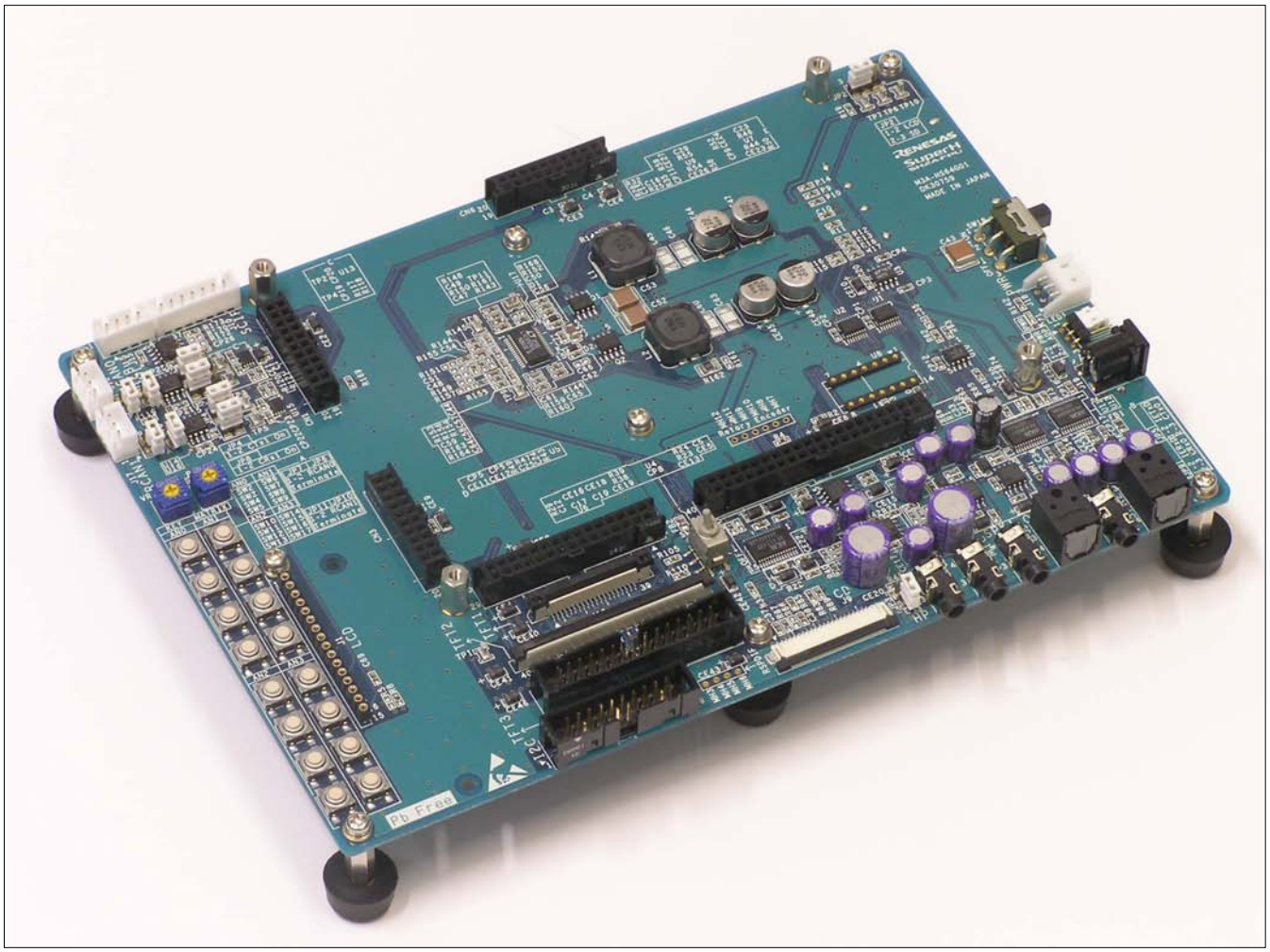


Figure 1.9.1 M3A-HS64G01 Exterior

1.10 M3A-HS64G01 Block Diagram

The following figure shows the block diagram of the M3A-HS64G01.

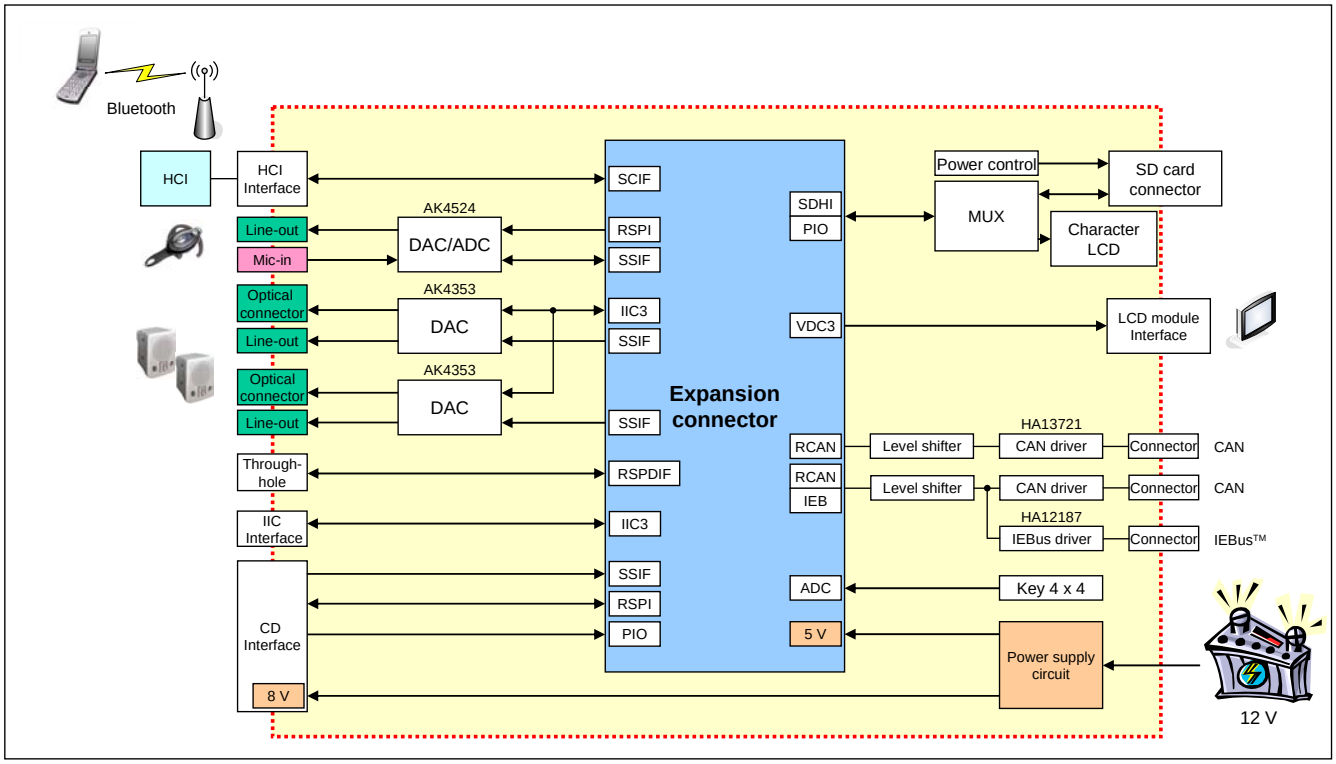


Figure 1.10.1 M3A-HS64G01 Block Diagram

1.11 M3A-HS64G01 Major Components

Figure 1.11.1 and Figure 1.11.2 show the M3A-HS64G01 layout and locations of the major components (PCB drawing).

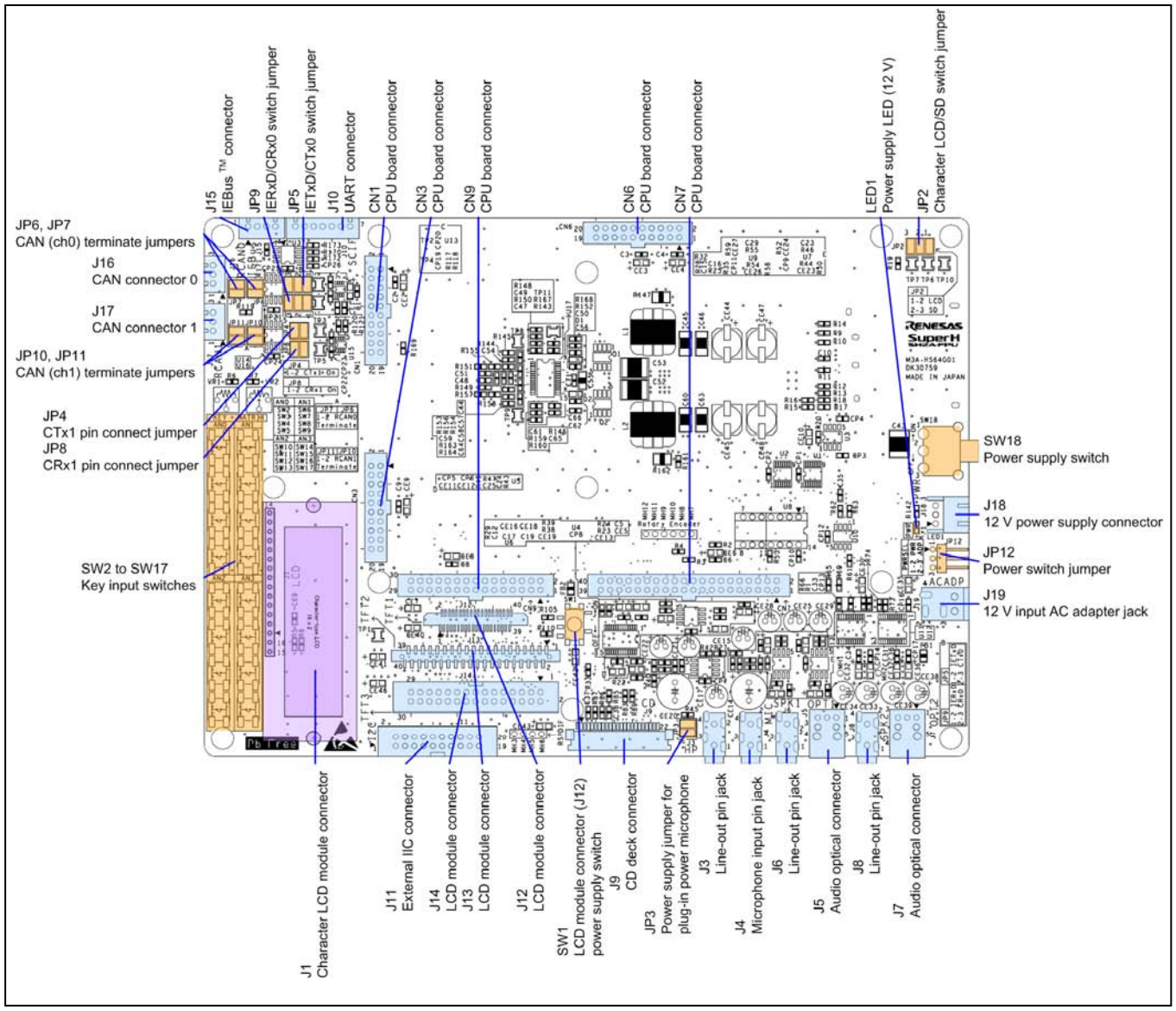


Figure 1.11.1 M3A-HS64G01 Layout and Component Placement (Top View of the Component Side)

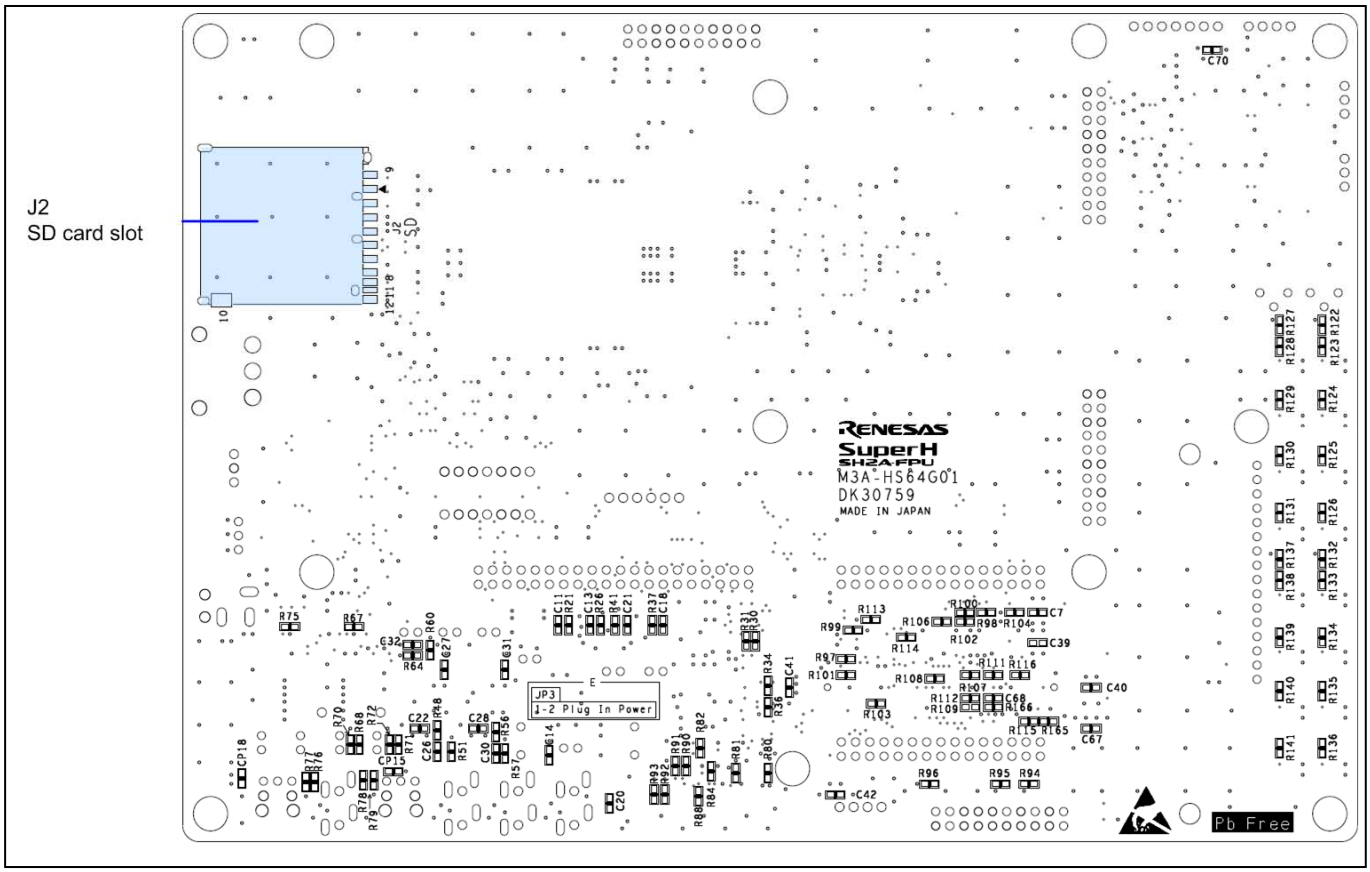


Figure 1.11.2 M3A-HS64G01 Layout and Component Placement (Top View of the Solder Side)

The following tables list the major components on the M3A-HS64G01.

Table 1.11.1 Major Components - ICs (1)

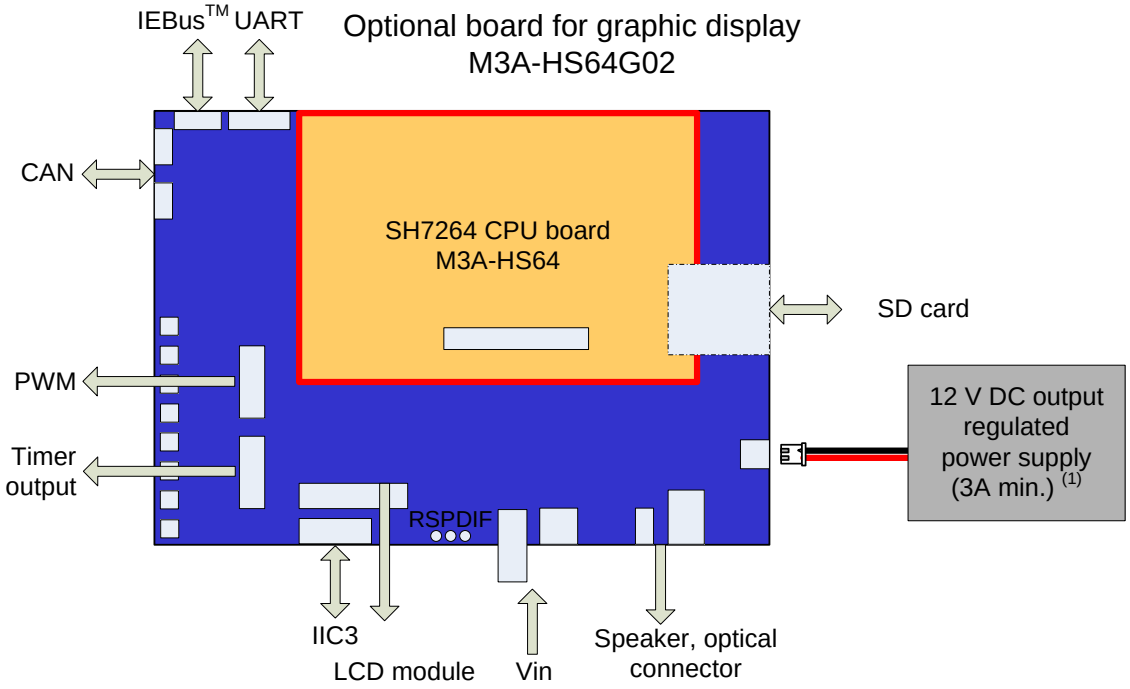
No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	Character LCD module	SD1602H	SUNLIKE	16 characters x 2 lines	1
2	Audio codec	AK4524VF	AKM	24-bit 96 kHz audio codec	1
3	D/A converters	AK4353VF	AKM	96 kHz 24-bit D/A converter	2
4	CAN drivers	HA13721FP	Renesas		2
5	IEBus™ driver	HA12187FP	Renesas		1
6	Adjustable regulator	LTC3727EG	LT	8 V/5 V	1
7	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	2

Table 1.11.2 Major Components -Connectors (2)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	20-pin expansion connectors	XG4C-2031	OMRON	20-pin MIL-spec connector	3
2	30-pin expansion connector	XG4C-3031	OMRON	30-pin MIL-spec connector	1
3	40-pin expansion connector	XG4C-4031	OMRON	40-pin MIL-spec connector	1
4	SD card slot	DM1B-DSF-PEJ	HRS	Reverse type	1
5	Optical connectors	TOTX147PL	TOSHIBA		2
6	CD deck connector	IMSA-9617S-22	IRISO	1 mm pitch FFC	1
7	UART connector	B7B-XH-A	J.S.T	TTL level	1
8	External IIC connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1
9	LCD module connector 1 (J12)	IMSA-9639S-40D	IRISO	0.5 mm pitch FFC, for TX09D55VM1CDA only	1
10	LCD module connector 2 (J13)	IMSA-9619S-40B	IRISO	1 mm pitch FFC, for TX09D14VM3CCA only	1
11	LCD module connector 3 (J14)	XG4C-3031	OMRON	30-pin MIL-spec connector General-purpose	1
12	IEBus™ connector	B4B-XH-A	J.S.T	2.5 mm pitch	1
13	CAN connectors	B3B-XH-A	J.S.T	2.5 mm pitch	2

1.12 M3A-HS64G02 Configuration

The following figure shows an example of the system configuration using the M3A-HS64G02 (optional board for graphic display).



Note:
1. Power supply is not included in this CPU board, and must be prepared by user.

Figure 1.12.1 M3A-HS64G02 System Configuration Example

1.13 M3A-HS64G02 Board Specifications

The following table describes the M3A-HS64G02 board specifications.

Table 1.13.1 Board Specifications

No.	Item	Description
1	LCD	Comes with following connectors to control an LCD module by the SH7264 on-chip VDC3 • Flexible connectors for LCD module: 2 • MIL-spec connector for LCD module: 1 (30-pin)
2	Video signal input	Inputs the video signal in the SH7264 on-chip VDC3 • AK8851 (Asahi Kasei EMD Corporation): 1 ・Decodes NTSC or PAL composite video signal and S-video signal digitally ・Includes two channels of a 10-bit ADC (Operates at 27 MHz) ・Composite video pin (RCA connector) ・S-video connector
3	Audio	Comes with an audio codec for audio output by the SH7264 on-chip SSIF • AK4353 (Asahi Kasei EMD Corporation): 1 ・96 KHz 24-bit D/A converter, on-chip digital audio transmitter ・Sampling frequency: 16 KHz to 96 KHz ・Stereo pin jack: 1 ・Optical connector: 1
4	PWM	Connected to the SH7264 on-chip Motor Control PWM timer pin • MIL-spec connector for PWM timer output: 1 (20-pin)
5	Timer output	Controls the LED brightness by the PWM mode in the SH7264 on-chip MTU2 • MIL-spec connector for timer output: 1 (20-pin)
6	SD card interface	Accesses the SD card by the SH7264 on-chip SDHI • SD card slot: 1 • Includes a card power control IC (Software control NOT allowed)
7	CAN	CAN communication by the SH7264 on-chip CAN (RCAN-TL1) • HA13721FP (Renesas CAN driver IC), includes a voltage level shifter
8	IEBus™	IEBus™ communication by the SH7264 on-chip IEBus controller (IEB) • HA12187FP (Renesas IEBus driver IC), includes a voltage level shifter
9	IIC	Connected to the SH7264 on-chip IIC bus interface (IIC3) pin • MIL-spec connector for connecting an external IIC interface: 1 (20-pin)
10	Switches	Key input by the SH7264 on-chip ADC • Key input switches: 16 (4 switches x 4 inputs)
11	Board specifications	• Dimensions: 210 mm x 148 mm • Mounting form: 4 layers, double-sided • Board thickness: 1.6 mm • Number of boards: 1

1.14 M3A-HS64G02 Exterior

The following figure shows the exterior of the M3A-HS64G02.

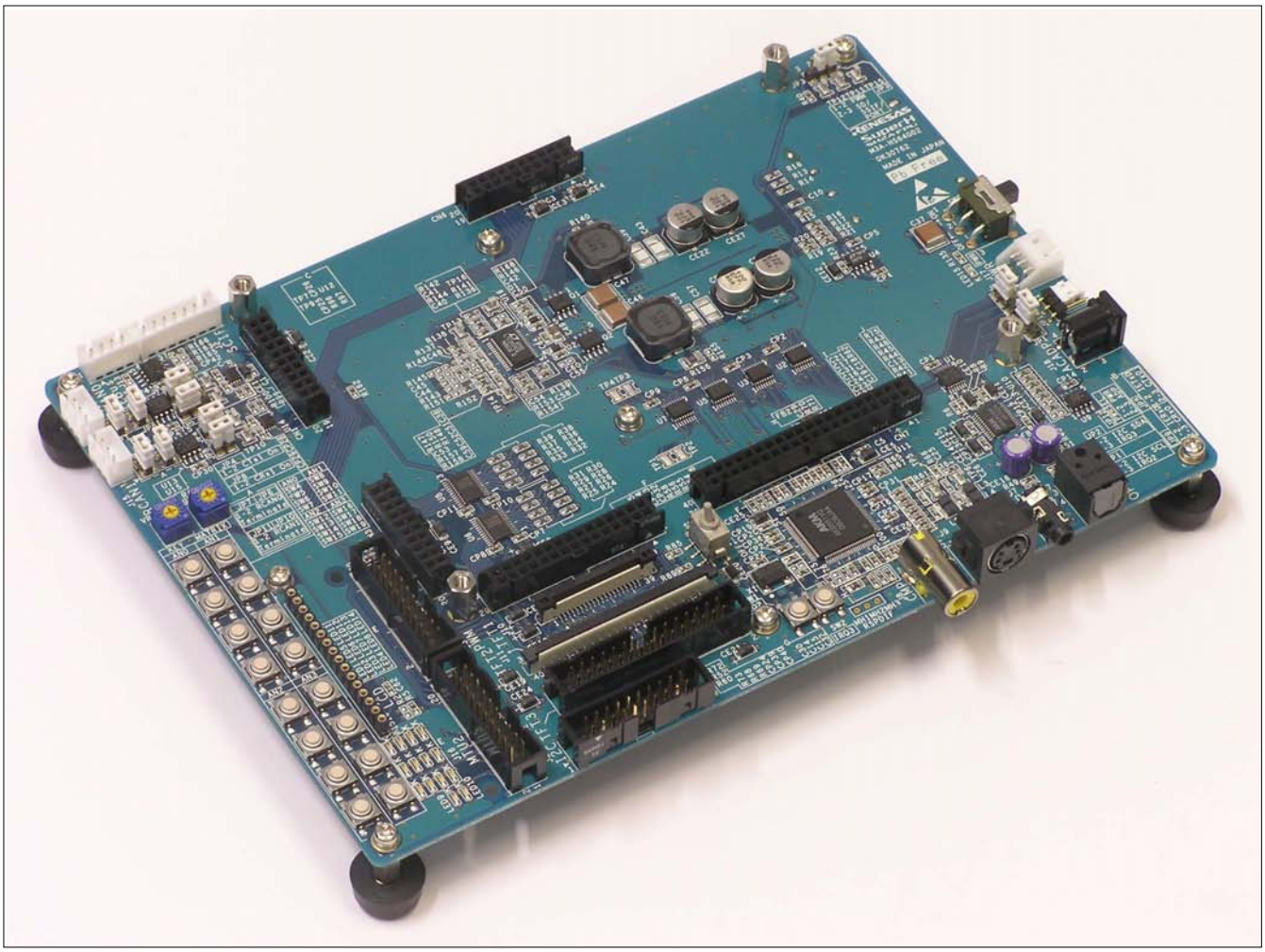


Figure 1.14.1 M3A-HS64G02 Exterior

1.15 M3A-HS64G02 Block Diagram

The following figure shows the block diagram of the M3A-HS64G02.

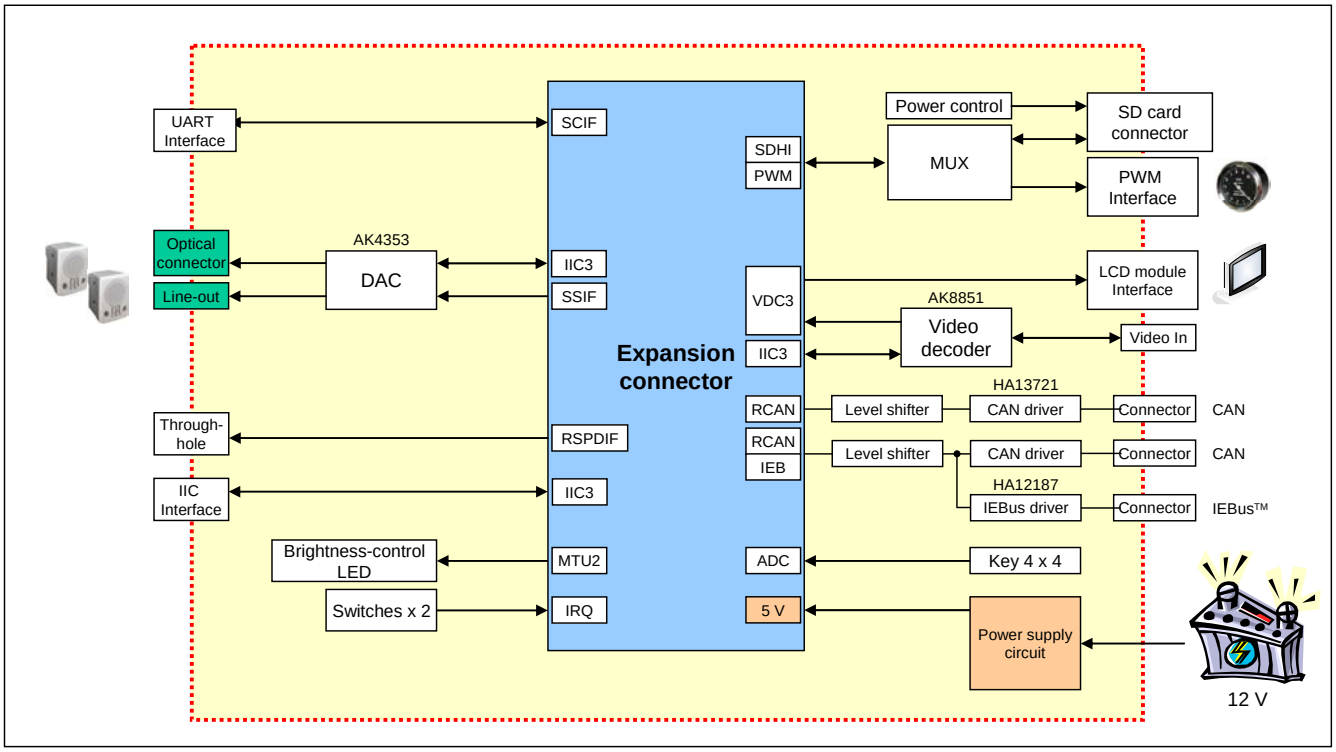


Figure 1.15.1 M3A-HS64G02 Block Diagram

1.16 M3A-HS64G02 Major Components

The following figure shows the M3A-HS64G02 layout and locations of the major components (PCB drawing).

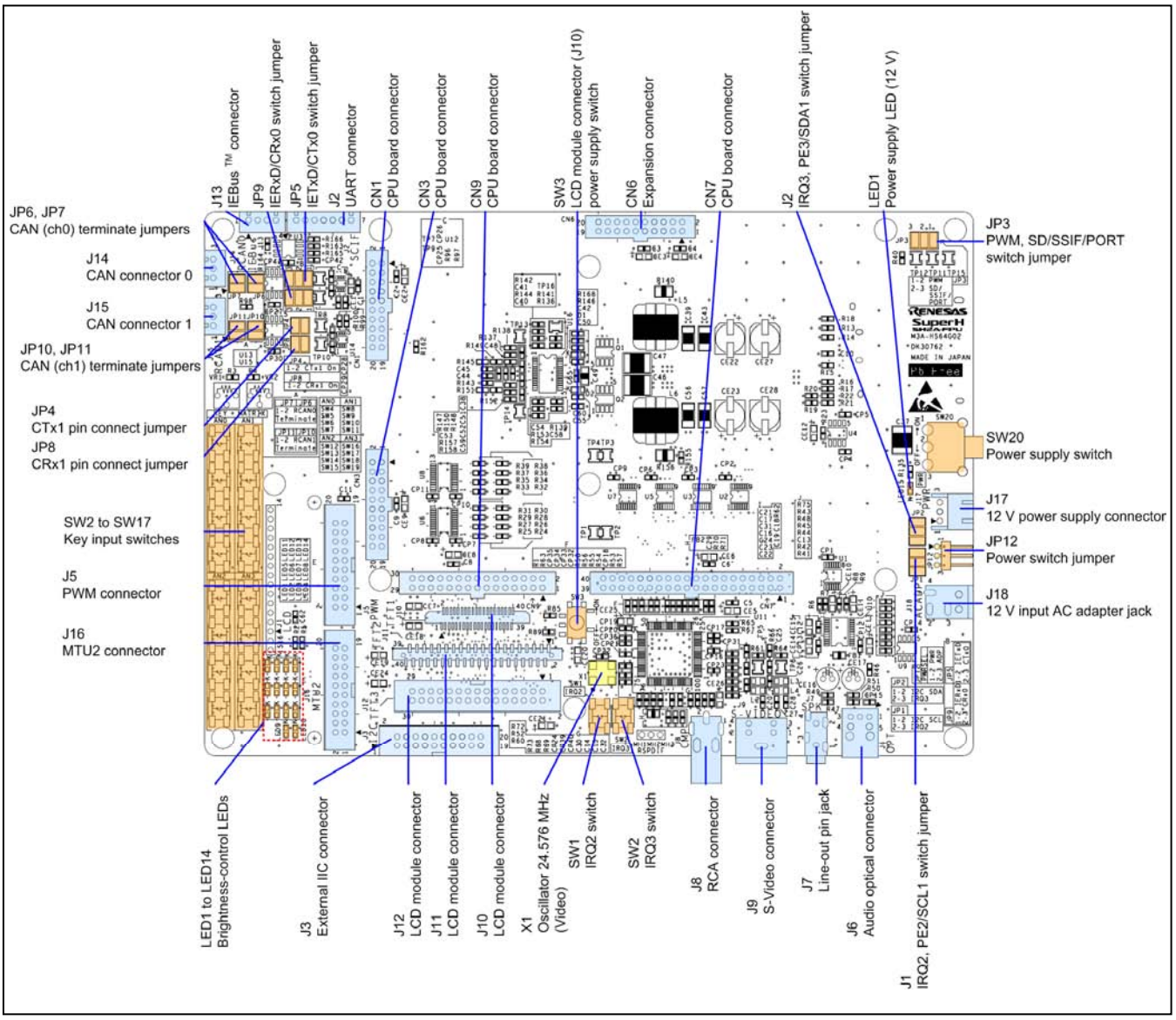


Figure 1.16.1 M3A-HS64G02 Layout and Component Placement (Top View of the Component Side)

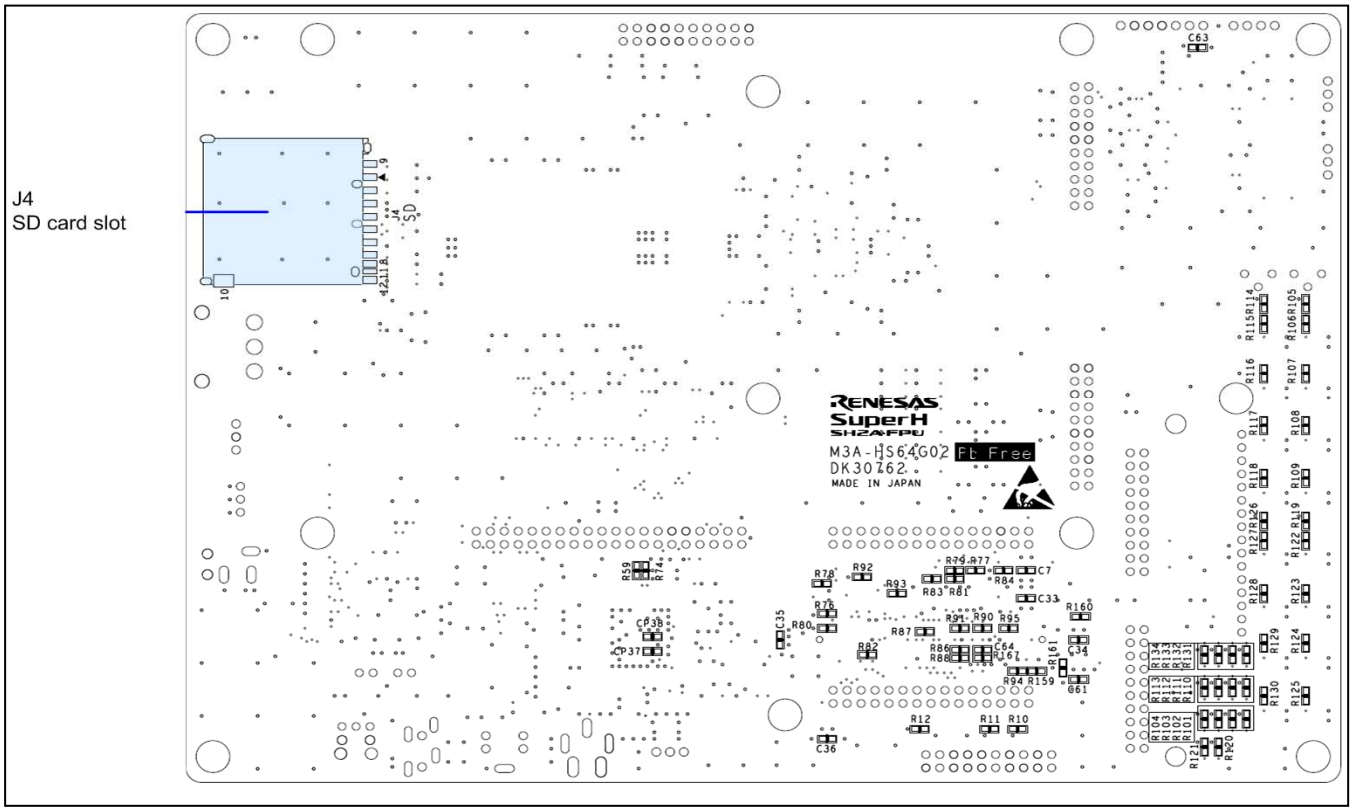


Figure 1.16.2 M3A-HS64G02 Layout and Component Placement (Top View of the Solder Side)

Table 1.16.1 and Table 1.16.2 list the major components on the M3A-HS64G02.

Table 1.16.1 Major Components - ICs (1/2)

No	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	Character LCD module	SD1602H	SUNLIKE	16 characters x 2 lines	1
2	Video decoder	AK8851VQ	AKM	Supports NTSC/PAL/ SECAM	1
3	D/A converter	AK4353VF	AKM	96 kHz, 24-bit D/A converter	1
4	CAN drivers	HA13721FP	Renesas		2
5	IEBus™ driver	HA12187FP	Renesas		1
6	Adjustable regulator	LTC3727EG	LT	8 V/5 V	1
7	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	4

Table 1.16.2 Major Components -Connectors (2/2)

No	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	20-pin expansion connectors	XG4C-2031	OMRON	20-pin MIL-spec connector	3
2	30-pin expansion connector	XG4C-3031	OMRON	30-pin MIL-spec connector	1
3	40-pin expansion connector	XG4C-4031	OMRON	40-pin MIL-spec connector	1
4	SD card slot	DM1B-DSF-PEJ	HRS	Reverse type	1
5	Optical connector	TOTX147PL	TOSHIBA		1
6	UART connector	B7B-XH-A	J.S.T	TTL level	1
7	External IIC connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1
8	LCD module connector 1 (J10)	IMSA-9639S-40D	IRISO	0.5 mm pitch FFC, for TX09D55VM1CDA only	1
9	LCD module connector 2 (J11)	IMSA-9619S-40B	IRISO	1 mm pitch FFC, for TX09D14VM3CCA only	1
10	LCD module connector 3 (J12)	XG4C-3031	OMRON	30-pin MIL-spec connector Multi-purpose	1
11	IEBus™ connector	B4B-XH-A	J.S.T	2.5 mm pitch	1
12	CAN connectors	B3B-XH-A	J.S.T	2.5 mm pitch	2
13	PWM connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1
14	MTU2 connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1

1.17 Memory Maps

The following figure shows memory map examples of the SH7264 and the M3A-HS64.

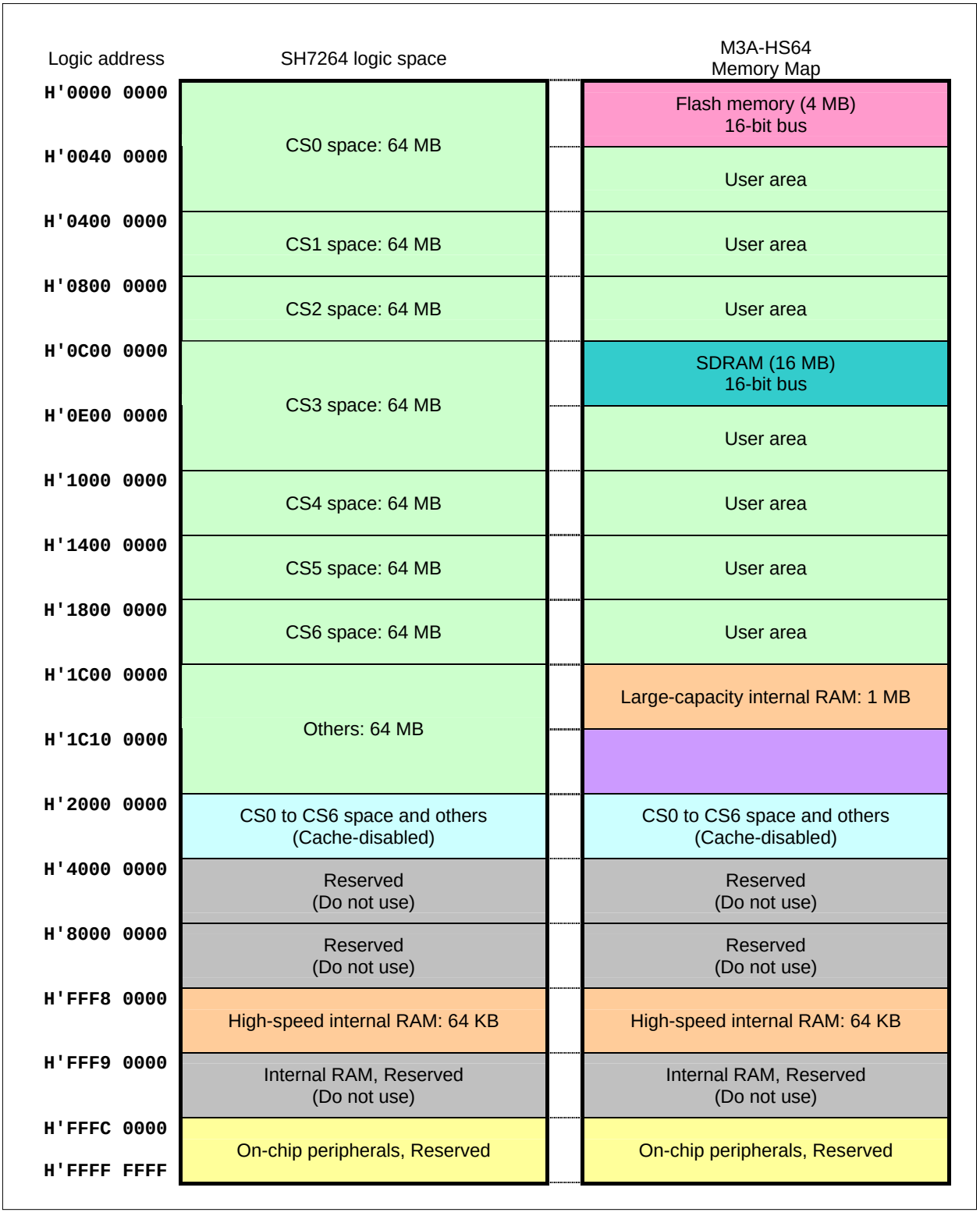


Figure 1.17.1 SH7264 Memory Map Example

1.18 Absolute Maximum Ratings

Table 1.18.1 and Table 1.18.2 list the absolute maximum ratings of the M3A-HS64, and its optional boards.

Table 1.18.1 Absolute Maximum Ratings on the M3A-HS64

Symbol	Parameter	Value	Remarks
VCC	5 V system power supply voltage	-0.3 to 6.0 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	-0.3 to 4.6 V	Reference voltage: VSS
1.2VCC	1.2 V system power supply voltage	-0.3 to 1.7 V	Reference voltage: VSS
Topr	Operating temperature	-10 to 55°C	Do not expose to condensation or corrosive gas
Tstr	Storage temperature	-20 to 60°C	Do not expose to condensation or corrosive gas

Note: Temperature refers to the air temperature in the vicinity of the board.

Table 1.18.2 Absolute Maximum Ratings on the SH7264 Optional Boards

Symbol	Parameter	Value	Remarks
12VCC	12 V system power supply voltage	-0.3 to 15.0 V	Reference voltage: VSS
8VCC	8 V system power supply voltage	-0.3 to 10.0 V	Reference voltage: VSS
5VCC	5 V system power supply voltage	-0.3 to 6.0 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	-0.3 to 4.6 V	Reference voltage: VSS
Topr	Operating temperature	-10°C to 55°C	Do not expose to condensation or corrosive gas
Tstr	Storage temperature	-20°C to 60°C	Do not expose to condensation or corrosive gas

Note: Temperature refers to the air temperature in the vicinity of the board.

1.19 Operating Conditions

Table 1.19.1 and Table 1.19.2 list the operating conditions of the M3A-HS64, and its optional boards.

Table 1.19.1 M3A-HS64 Operating Conditions

Symbol	Parameter	Value	Remarks
VCC	5 V system power supply voltage	4.75 to 5.25 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	3.0 to 3.6 V	Reference voltage: VSS
1.2VCC	1.2 V system power supply voltage	1.1 to 1.3 V	Reference voltage: VSS
-	Maximum current consumption	1.5 A max.	
Topr	Operating temperature	0°C to 40°C	Do not expose to condensation or corrosive gas

Table 1.19.2 SH7264 Optional Boards Operating Conditions

Symbol	Parameter	Value	Remarks
12VCC	12 V system power supply voltage	11.4 to 12.6 V	Reference voltage: VSS
8VCC	8 V system power supply voltage	7.6 to 8.4 V	Reference voltage: VSS
VCC	5 V system power supply voltage	4.75 to 5.25 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	3.0 to 3.6 V	Reference voltage: VSS
-	Maximum current consumption	3 A max.	Includes the M3A-HS64 (SH7264 CPU board)
Topr	Operating temperature	0°C to 40°C	Do not expose to condensation or corrosive gas

1.20 Usage Note

This section describes usage note the SH7264 CPU board and optional boards.

1.20.1 Configuring Unused Pins

Set the SH7264 unused (unconnected) multiplexed pins to output when not connecting the optional board with the SH7264 CPU board. Port H requires external resistors (R10 to R17) or must be set to an analog input.

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Chapter 2
M3A-HS64 Functions

2.1 Overview of Functions

M3A-HS64 includes the function modules listed in the following table.

Table 2.1.1 M3A-HS64 Function Modules

Section	Function	Description
2.2	CPU	• SH7264
2.3	Memory	• Connects the SH7264 external bus interface and an NOR flash memory - SH7264 Bus State Controller (BSC) recommended setting - Access timing example • Connects the SH7264 external bus interface and an SDRAM - SH7264 BSC recommended setting - Access timing example • Connects the SH7264 NAND flash memory controller (FLCTL) and NAND flash memory • Connects the SH7264 Renesas Serial Peripheral Interface (RSPI) and serial flash memory • Connects the SH7264 IIC bus interface 3 (IIC3) and an EEPROM
2.4	USB Interface	• Connects the SH7264 USB 2.0 Host/function module and a USB connector
2.5	RS-232C Interface	• Connects the SH7264 Serial Communication Interface with FIFO (SCIF) and an RS-232C connector
2.6	I/O Ports	• Connect the SH7264 I/O ports, LEDs, and DIP switches
2.7	Interrupt Switches	• Connects the SH7264 NMI pin, IRQ1 pin and push-button switches
2.8	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
2.9	Reset Module	• Resets devices on the M3A-HS64
2.10	Power Supply Module	• Controls the M3A-HS64 system power supply
2.11	E10A-USB Interface	• Connects the SH7264 user debug interface and an H-UDI connector
-	Operating Specifications	• Connectors, switches, and LEDs Refer to Chapter 5 for details.

2.2 CPU

2.2.1 SH7264 Overview

The M3A-HS64 includes the SH7264, the 32-bit RISC MCU that operates with a maximum frequency of 144 MHz.

2.2.2 SH7264 Pin Functions Used on the M3A-HS64

Table 2.2.1 to Table 2.2.6 list the SH7264 pin functions used on the M3A-HS64.

Table 2.2.1 SH7264 Pin Functions (1/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
1	PC2/RD/WR#	RD/WR#	Connected to the SDRAM WE# pin	CN6, pin 7	
2	PC3/WE0#/DQML	WE0#	Connected to the NOR flash memory WE# pin	CN6, pin 8	
		DQML	Connected to the SDRAM DQML pin		
3	Vss				
4	PC4/WE1#/DQMU/WE#	DQMU	Connected to the SDRAM DQMU pin	CN6, pin 9	
5	PVcc				
6	PC9/TIOC2A	-	-	CN6, pin 12	
7	PC10/TIOC2B	-	-	CN6, pin 13	
8	PC5/RAS#/TIOC4A/IRQ4	RAS#	Connected to the SDRAM RAS# pin	-	SW5-4: OFF
		-	-	CN6, pin 14	SW5-4: ON
9	PC6/CAS#/TIOC4B/IRQ5	CAS#	Connected to the SDRAM CAS# pin	-	SW5-4: OFF
		-	-	CN6, pin 15	SW5-4: ON
10	Vcc				
11	PC7/CKE/TIOC4C/IRQ6	CKE	Connected to the SDRAM CKE pin	-	SW5-4: OFF
		-	-	CN6, pin 16	SW5-4: ON
12	Vss				
13	PC8/CS3#/TIOC4D/IRQ7	CS3#	Connected to the SDRAM CS# pin	-	SW5-4: OFF
		-	-	CN6, pin 17	SW5-4: ON
14	PVcc				
15	PB1/A1	A1	Address bus	CN4, pin 1	
16	PB2/A2	A2	Address bus	CN4, pin 2	
17	PB3/A3	A3	Address bus	CN4, pin 3	
18	PB4/A4/TIOC0A	A4	Address bus	CN4, pin 4	
19	PB5/A5/TIOC0B	A5	Address bus	CN4, pin 5	
20	PB6/A6/TIOC0C	A6	Address bus	CN4, pin 6	
21	PB7/A7/TIOC0D	A7	Address bus	CN4, pin 9	
22	Vcc				
23	PB8/A8/TIOC1A	A8	Address bus	CN4, pin 10	
24	Vss				
25	PB9/A9/TIOC1B	A9	Address bus	CN4, pin 11	
26	PVcc				
27	PB10/A10/TIOC2A	A10	Address bus	CN4, pin 12	
28	PB11/A11/TIOC2B	A11	Address bus	CN4, pin 13	
29	PB12/A12/TIOC3A	A12	Address bus	CN4, pin 14	
30	PB13/A13/TIOC3B	A13	Address bus	CN4, pin 17	
31	PB14/A14/TIOC3C	A14	Address bus	CN4, pin 18	
32	PB15/A15/TIOC3D	A15	Address bus	CN4, pin 19	
33	Vcc				

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 2.2.2 SH7264 Pin Functions (2/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
34	PB16/A16/TIOC4A	A16	Address bus	CN4, pin 20	
35	Vss				
36	CKIO	CKIO	Connected to the SDRAM CLK pin	CN6, pin 20	
37	PVcc				
38	PB17/A17/TIOC4B	A17	Address bus	CN4, pin 21	
39	PB18/A18/TIOC4C	A18	Address bus	CN4, pin 22	
40	PB19/A19/TIOC4D	A19	Address bus	CN4, pin 25	
41	PB20/A20	A20	Address bus	CN4, pin 26	
42	PB21/A21	A21	Address bus	CN4, pin 27	
43	PB22/A22/CS4#	PB22	Switches the system setting/user interface	CN4, pin 28	Low: MD Hi: IO
44	PJ11/PWM2H/DACK1	-	-	CN1, pin 1	
45	Vcc				
46	PJ10/PWM2G/DREQ1	-	-	CN1, pin 2	
47	Vss				
48	PJ9/PWM2F/TEND1	-	-	CN1, pin 4	
49	PVcc				
50	PJ8/PWM2E/RTS3#	-	-	CN1, pin 5	
51	RES#	RES#	Reset input	CN7, pin 6	
52	NMI	NMI	Non-maskable interrupt		
53	PLLVcc				
54	PA3/MD_CLK0	PA3	Connected to SW6-6 as a user input port	CN1, pin 7	PB22: High
		MD_CLK0	Connected to SW5-1 as the clock mode input 0		PB22: Low
55	PLLVss				
56	PA2/MD_CLK1	PA21	Connected to SW6-5 as a user input port	CN1, pin 8	PB22: High
		MD_CLK1	Fixed high as the clock mode input 1		PB22: Low
57	EXTAL	EXTAL	Connects the system external clock to MCU	-	18 MHz
58	XTAL	XTAL	Open	-	
59	PA1/MD_BOOT0	PA1	Connected to LED3 as a user output port	CN1, pin 9	PB22: High
		MD_BOOT0	Connected to SW5-2 as the boot mode input 0		PB22: Low
60	PA0/MD_BOOT1	PA0	Connected to LED2 as a user output port	CN1, pin 10	PB22: High
		MD_BOOT1	Connected to SW5-3 as the boot mode input 1		PB22: Low
61	PJ7/TIOC1B/CTS3#	-	-	CN1, pin 12	
62	PJ6/TIOC1A/SCK3	-	-	CN1, pin 13	
63	PJ5/IERxD/TxD3	-	-	CN1, pin 14	
64	Vss				
65	PJ4/IETxD/RxD3	-	-	CN1, pin 15	
66	PVcc				
67	RTC_X1	RTC_X1	Connects a real-time clock resonator to MCU	-	32.768 kHz
68	RTC_X2	RTC_X2		-	
69	Vss				
70	PJ3/CRx1/CRx0/CRx1/IRQ1	IRQ1	IRQ1 switch	-	JP6: 1-2
		-	-	CN1, pin 17	JP6: 2-3
71	PJ2/CTx1/CTx0&CTx1/CS2#/ SCK0/LCD_M_DISP	-	-	CN1, pin 18	
72	Vcc				
73	PJ1/CRx0/IERxD/IRQ0/RxD0	RxD0	Connected to the RS-232C connector (J10)	-	JP5: 1-2
		-	-	CN1, pin 19	JP5: 2-3
74	Vss				
75	PJ0/CTx0/IETxD/CS1#/TxD0/A0	TxD0	Connected to the RS-232C connector (J10)	-	JP4: 1-2
		-	-	CN1, pin 20	JP4: 2-3

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 2.2.3 SH7264 Pin Functions (3/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
76	PVcc				
77	USB_X1	USB_X1	Connects the USB external clock to MCU	-	48 MHz
78	USB_X2	USB_X2	Open	-	
79	ASEMD#	ASEMD#	ASE mode select	-	H-UDI
80	USBDPVcc				
81	USBDPVss				
82	DM	DM	USB differential signal D- data	-	
83	DP	DP	USB differential signal D+ data	-	
84	VBUS	VBUS	VBUS input	-	
85	USBDVcc				
86	USBDVss				
87	REFRIN	REFRIN	Reference input	-	Connects a 5.6 kΩ ± 1% resistor
88	USBAPVcc				
89	USBAPVss				
90	USBAVcc				
91	USBAVss				
92	USBUVcc				
93	USBUVss				
94	PH0/AN0	-	-	CN3, pin 4	
95	PH1/AN1	-	-	CN3, pin 3	
96	PH2/AN2	-	-	CN3, pin 8	
97	PH3/AN3	-	-	CN3, pin 7	
98	PH4/AN4	-	-	CN3, pin 12	
99	PH5/AN5	-	-	CN3, pin 11	
100	AVss				
101	PH6/AN6	-	-	CN3, pin 16	
102	AVref				
103	PH7/AN7	-	-	CN3, pin 15	
104	AVcc				
105	TRST#	TRST#	Initialization-signal input pin	-	H-UDI
106	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Brake mode acknowledge	-	H-UDI
		ASEBRK#	Brake request		
107	TDO	TDO	Test data output	-	H-UDI
108	TDI	TDI	Test data input	-	H-UDI
109	TMS	TMS	Test mode select	-	H-UDI
110	TCK	TCK	Test clock	-	H-UDI
111	PG24/MISO1/TIOC0D	-	-	CN9, pin 29	
112	PG23/MOSI1/TIOC0C	-	-	CN9, pin 30	
113	PVcc				
114	PG22/SSL10/TIOC0B	-	-	CN9, pin 27	
115	Vss				
116	PG21/RSPCK1/TIOC0A	-	-	CN9, pin 28	
117	Vcc				
118	PG20/LCD_EXTCLK/MISO1/ TxD7	LCD_EXTCLK	Connects the LCD module external clock to MCU	CN9, pin 26	Default: 5.33 MHz
119	PG19/LCD_CLK/TIOC2B /MOSI1/RxD7	-	-	CN9, pin 23	
120	PG18/LCD_DE/TIOC2A/ SSL10/TxD6	-	-	CN9, pin 24	
121	PG17/LCD_HSYNC/TIOC1B/ RSPCK1/RxD6	-	-	CN9, pin 21	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 2.2.4 SH7264 Pin Functions (4/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
122	PG16/LCD_VSYNC/TIOC1A/ TxD3/CTS1#	-	-	CN9, pin 19	
123	PG15/LCD_DATA15/TIOC0D/ RxD3/RTS1#	-	-	CN9, pin 20	
124	PG14/LCD_DATA14/TIOC0C/ SCK1	-	-	CN9, pin 17	
125	PG13/LCD_DATA13/TIOC0B/ TxD1	-	-	CN9, pin 18	
126	PVcc				
127	PG12/LCD_DATA12/TIOC0A/ RxD1	-	-	CN9, pin 16	
128	Vss				
129	PG11/LCD_DATA11/SSITxD0/ IRQ3/TxD5/SIOFTxD	-	-	CN9, pin 13	
130	Vcc				
131	PG10/LCD_DATA10/SSIRxD0/ IRQ2/RxD5/SIOFRxD	-	-	CN9, pin 14	
132	PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC	-	-	CN9, pin 11	
133	PG8/LCD_DATA8/SSISCK0/ RxD4/SIOFSCK	-	-	CN9, pin 12	
134	PG7/LCD_DATA7/SD_CD/PINT7	-	-	CN9, pin 9	
135	PG6/LCD_DATA6/SD_WP/PINT6	-	-	CN9, pin 7	
136	PG5/LCD_DATA5/SD_D1/PINT5	-	-	CN9, pin 8	
137	PG4/LCD_DATA4/SD_D0/PINT4	-	-	CN9, pin 6	
138	PVcc				
139	PG3/LCD_DATA3/SD_CLK/ PINT3	-	-	CN9, pin 3	
140	Vss				
141	PG2/LCD_DATA2/SD_CMD/ PINT2	-	-	CN9, pin 4	
142	Vcc				
143	PG1/LCD_DATA1/SD_D3/PINT1	-	-	CN9, pin 1	
144	PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#	-	-	CN9, pin 2	
145	PK11/PWM2D/SSITxD0	-	-	CN7, pin 37	
146	PK10/PWM2C/SSIRxD0	-	-	CN7, pin 38	
147	PK9/PWM2B/SSIWS0	-	-	CN7, pin 35	
148	PK8/PWM2A/SSISCK0	-	-	CN7, pin 36	
149	AUDIO_X2	AUDIO_X2	Open	-	
150	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	-	Switched by JP 7
151	PF12/BS#/MISO0/TIOC3D/ SPDIF_OUT	MISO0	Connected to the serial flash memory SO pin	-	SW5-6: OFF
		-	-	CN7, pin 33	SW5-6: ON
152	PVcc				
153	PF11/A25/SSIDATA3/MOSI0/ TIOC3C/SPDIF_IN	MOSI0	Connected to the serial flash memory SI pin	-	SW5-6: OFF
		-	-	CN7, pin 31	SW5-6: ON
154	Vss				
155	PF10/A24/SSIWS3/SSL00/ TIOC3B/FCE#	SSL00	Connected to the serial flash memory CS# pin	-	SW5-5: ON SW5-6: OFF
		-	-	CN7, pin 32	SW5-5: ON SW5-6: ON
		FCE#	Connected to the NAND flash memory CE# pin	-	SW5-5: OFF

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 2.2.5 SH7264 Pin Functions (5/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
156	Vcc				
157	PF9/A23/SSISCK3/RSPCK0/ TIOC3A/FRB	RSPCK0	Connected to the serial flash memory SCK pin	-	SW5-5: ON SW5-6: OFF
		-	-	CN7, pin 30	SW5-5: OFF SW5-6: ON
		FRB	Connected to the NAND flash memory R/B# pin	-	SW5-5: OFF
158	PF8/CE2B#/SSIDATA3/DV_CLK	-	-	CN7, pin 27	
159	PF7/CE2A#/SSIWS3/DV_DATA7/ TCLKD	-	-	CN7, pin 28	
160	PF6/CS6#/CE1B#/SSISCK3/ DV_DATA6/TCLKB	-	-	CN7, pin 25	
161	PF5/CS5#/CE1A#/SSIDATA2/ DV_DATA5/TCLKC/AUDATA3	AUDATA3	Connected to the H-UDI connector (J3)	CN7, pin 23	AUD
		-	-		
162	PF4/ICIOWR#/AH#/SSIWS2/ DV_DATA4/TxD3/AUDATA2	AUDATA2	Connected to the H-UDI connector (J3)	CN7, pin 24	AUD
		-	-		
163	PF3/ICIORD#/SSISCK2/ DV_DATA3/RxD3/AUDATA1	AUDATA1	Connected to the H-UDI connector (J3)	CN7, pin 22	AUD
		-	-		
164	PF2/BACK#/SSIDATA1/ DV_DATA2/TxD2/DACK0/ AUDATA0	AUDATA0	Connected to the H-UDI connector (J3)	CN7, pin 19	AUD
		-	-		
165	PVcc				
166	PF1/BREQ#/SSIWS1/DV_DATA1/ RxD2/DREQ0/AUDSYNC#	AUDSYNC#	Connected to the H-UDI connector (J3)	CN7, pin 20	AUD
		-	-		
167	Vss				
168	PF0/WAIT#/SSISCK1/DV_DATA0 /SCK2/TEND0/AUDCK	AUDCK	Connected to the H-UDI connector (J3)	CN7, pin 17	AUD
		-	-		
169	Vcc				
170	PK7/PWM1H/SD_CD	-	-	CN7, pin 15	
171	PK6/PWM1G/SD_WP	-	-	CN7, pin 16	
172	PK5/PWM1F/SD_D1	-	-	CN7, pin 13	
173	PK4/PWM1E/SD_D0	-	-	CN7, pin 14	
174	PE5/SDA2/DV_HSYNC	-	-	CN7, pin 12	
175	PE4/SCL2/DV_VSYNC	-	-	CN7, pin 9	
176	PE3/SDA1/IRQ3	SDA1	Connected to the EEPROM SDA pin	CN7, pin 10	JP9: 1-2
		-	-		
177	PE2/SCL1/IRQ2	SCL1	Connected to the EEPROM SCL pin	CN7, pin 7	JP8: 1-2
		-	-		
178	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ ADTRG#	-	-	CN7, pin 8	
179	PE0/SCL0/AUDIO_CLK/IRQ0	-	-	CN7, pin 5	
180	PK3/PWM1D/SD_CLK	-	-	CN7, pin 3	
181	PVcc				
182	Vss				
183	PK2/PWM1C/SD_CMD	-	-	CN7, pin 4	
184	PK1/PWM1B/SD_D3	-	-	CN7, pin 1	
185	PK0/PWM1A/SD_D2	-	-	CN7, pin 2	
186	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 1	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 2.2.6 SH7264 Pin Functions (6/6)

No.	Name	Function	Description	Expansion connector	Remarks
187	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 3	
188	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 6	
189	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 8	
190	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 11	
191	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 13	
192	Vss				
193	PVcc				
194	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 16	
195	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 18	
196	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and the NAND flash memory WE# pin	CN8, pin 2	Auto-switch
197	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and the NAND flash memory ALE pin	CN8, pin 4	Auto-switch
198	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and the NAND flash memory CLE pin	CN8, pin 7	Auto-switch
199	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and the NAND flash memory RE# pin	CN8, pin 9	Auto-switch
200	PD3/D3/PWM1D	D3	Data bus	CN8, pin 12	
201	Vcc				
202	PD2/D2/PWM1C	D2	Data bus	CN8, pin 14	
203	Vss				
204	PD1/D1/PWM1B	D1	Data bus	CN8, pin 17	
205	PVcc				
206	PD0/D0/PWM1A	D0	Data bus	CN8, pin 19	
207	PC0/CS0#	CS0#	Connected to the NOR flash memory CE# pin	CN6, pin 5	
208	PC1/RD#	RD#	Connected to the NOR flash memory OE# pin	CN6, pin 6	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

2.2.3 M3A-HS64 Module Availability

The following table shows which combination of modules can/cannot be used.

Table 2.2.7 M3A-HS64 Module Availability

				M3A-HS64												
	SH7264 Peripheral Function	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory	USB	H-UDI (14-pin)	H-UDI (36-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C
M3A-HS64	BSC	U6	NOR flash memory		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	BSC	U10	SDRAM	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	FLCTL	U7	NAND flash memory	Y	Y		Y	*2	Y	Y	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y
	RSPI	U9	Serial flash memory	Y	Y	*2	Y		Y	Y	Y	Y	Y	Y	Y	Y
	USB	J1, and J2	USB	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y
	H-UDI,AUD	J3	H-UDI (36-pin)	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y
	I/O ports	LED2, and LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	*1	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y
	I/O ports	SW5, and SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	*1	Y	Y		Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	

Y: Yes N: No

Notes:
1: When using LED2, and LED3, SW5-1, SW5-2, and SW5-3 on the M3A-HS64 cannot be used.
2: PF9, and PF10 are multiplex pins. When setting SW5-5, and SW5-6, either serial or NAND can be used.

2.2.4 SH7264 Multiplex Pins Used on the M3A-HS64

Table 2.2.8 to Table 2.2.14 list SH7264 multiplex pin functions used on the M3A-HS64.

These multiplex pins are set as port input pins by default. Set the MD bit in the port control register to use the SH7264 peripheral functions (except I/O ports).

Table 2.2.8 SH7264 Multiplex Pin Functions (BSC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
BSC	CS0#	PCCR0	PC0MD0 = B'1	PC0/CS0# (1)
	CS3#	PCCR2	PC8MD[1:0] = B'01	PC8/CS3#/TIOC4D/IRQ7
	RD#	PCCR0	PC1MD0 = B'1	PC1/RD# (1)
	WE0#/DQML	PCCR0	PC3MD0 = B'1	PC3/WE0#/DQML
	WE1#/DQMU/WE#	PCCR1	PC4MD0 = B'1	PC4/WE1#/DQMU/WE#
	RAS#	PCCR1	PC5MD[1:0] = B'01	PC5/RAS#/TIOC4A/IRQ4
	CAS#	PCCR1	PC6MD[1:0] = B'01	PC6/CAS#/TIOC4B/IRQ5
	CKE	PCCR1	PC7MD[1:0] = B'01	PC7/CKE/TIOC4C/IRQ6
	RD/WR#	PCCR0	PC2MD0 = B'1	PC2/RD/WR#
	A21	PBCR5	PB21MD0 = B'1	PB21/A21
	D15	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H (1)
	D14	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G (1)
	D13	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F (1)
	D12	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E (1)
	D11	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D (1)
	D10	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C (1)
	D9	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B (1)
	D8	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A (1)
	D7	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H (1)
	D6	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G (1)
	D5	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F (1)
	D4	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E (1)
	D3	PDCR0	PD3MD[1:0] = B'01	PD3/D3/PWM1D (1)
	D2	PDCR0	PD2MD[1:0] = B'01	PD2/D2/PWM1C (1)
	D1	PDCR0	PD1MD[1:0] = B'01	PD1/D1/PWM1B (1)
	D0	PDCR0	PD0MD[1:0] = B'01	PD0/D0/PWM1A (1)

Note 1: For boot modes 1 to 3

Table 2.2.9 SH7264 Multiplex Pin Functions (INTC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
INTC	IRQ1	PJCR0	PJ3MD[1:0] = B'11	PJ3/CRx1/CRx0&CRx1/IRQ1

Table 2.2.10 SH7264 Multiplex Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SCIF	RxD0	PJCR0	PJ1MD[2:0] = B'100	PJ1/CRx0/IERxD/IRQ0/RxD0
	TxD0	PJCR0	PJ0MD[2:0] = B'100	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 2.2.11 SH7264 Multiplex Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
IIC3	SDA1	PECR0	PE3MD[1:0] = B'01	PE3/SDA1/IRQ3
	SCL1	PECR0	PE2MD[1:0] = B'01	PE2/SCL1/IRQ2

Table 2.2.12 SH7264 Multiplex Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E
	FCE#	PFCR2	PF10MD[2:0] = B'101	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	FRB	PFCR2	PF9MD[2:0] = B'101	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 2.2.13 SH7264 Multiplex Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
RSPI	MISO0	PFCR3	PF12MD[2:0] = B'011	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
	MOSI0	PFCR2	PF11MD[2:0] = B'011	PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN
	SSL00	PFCR2	PF10MD[2:0] = B'011	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	RSPCK0	PFCR2	PF9MD[2:0] = B'011	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 2.2.14 SH7264 Multiplex Pin Functions (PORT)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
PORT	PB22	PBCR5	PB22MD[1:0] = B'00	PB22/A22/CS4#

2.3 Memory

The M3A-HS64 includes the SH7264 internal RAM, an external flash memory, an external SDRAM, and an external EEPROM.

2.3.1 SH7264 Internal RAM

The SH7264 includes 64 KB internal RAM that allows high-speed access to MCU, and a 1 MB large-capacity internal RAM of which 32-KB is used for data retention.

2.3.2 NOR Flash Memory Interface

The M3A-HS64 comes standard with an NOR flash memory listed in the table below to store the user program.
The NOR flash memory works at 16-bit mode, and 3.3 V-only single power supply. It is write-protected or write-enabled by system setting DIP switches. The figure below shows the NOR flash memory block diagram. Table 2.3.2 lists the DIP switches setting (SW6-1).

Table 2.3.1 NOR Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
S29GL032N90TFI020	16-bit	4 MB (16-bit x 2 M Words x 1)	90 ns

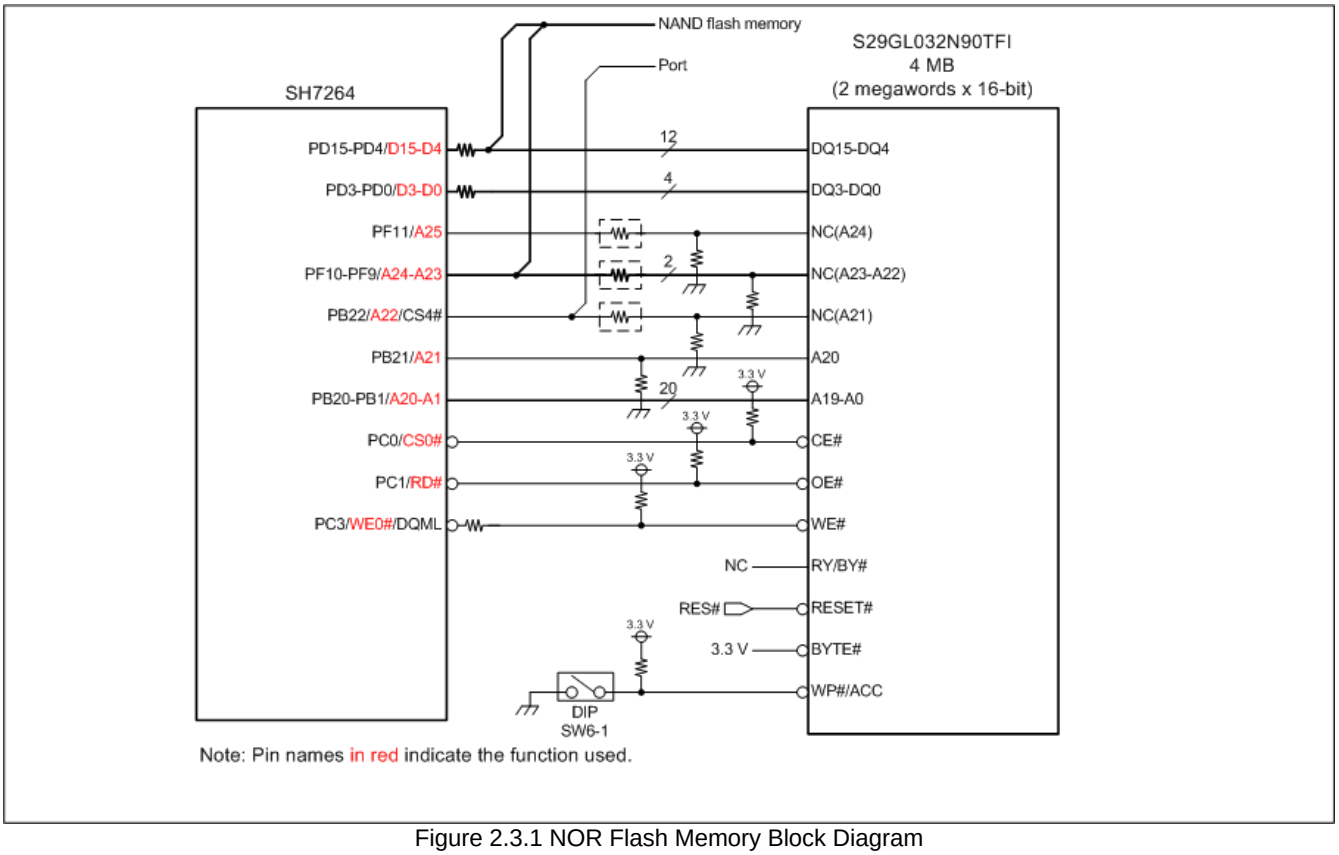

Figure 2.3.1 NOR Flash Memory Block Diagram

Table 2.3.2 DIP Switches Setting (SW6-1)

Number	Function	
	OFF (High)	ON (Low)
SW6-1	NOR flash memory is write-enabled (default)	NOR flash memory is write-protected

The figure below shows the write and read access timing example of the NOR flash memory. The table below lists the bus state controller settings (write/read) when the SH7264 bus clock works at 72 MHz.

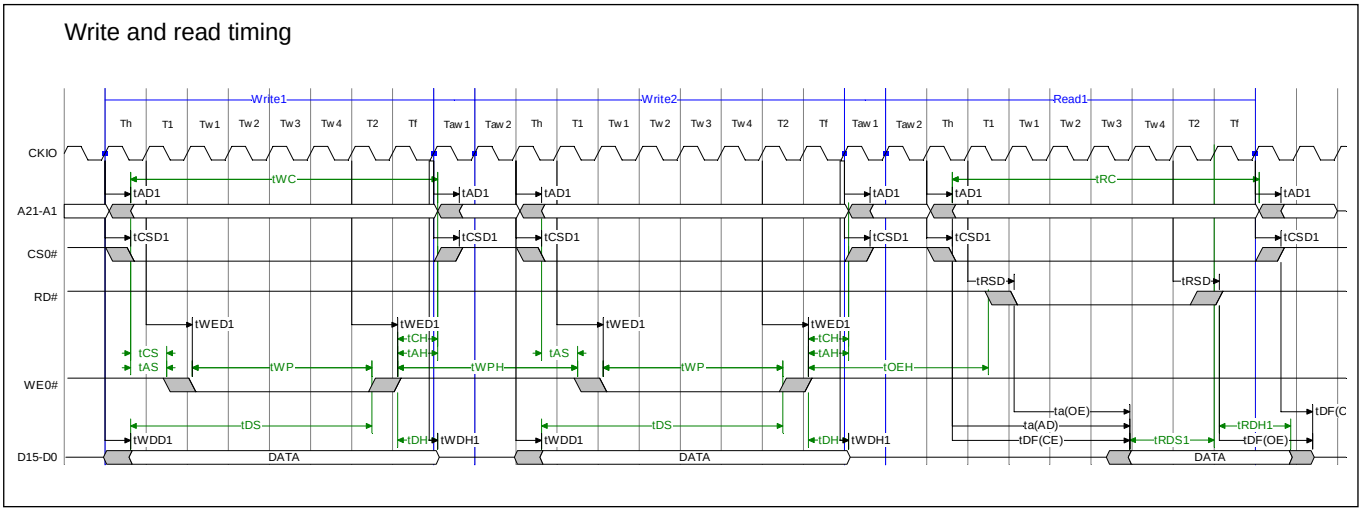

Figure 2.3.2 NOR Flash Memory write/read Access Timing Example

Table 2.3.3 Bus State Controller Setting (Write and read the NOR flash memory)

User area	Target device	Setting
CS0	S29GL032N90TFI020	CS0 Space Bus Control Register (CS0BCR): Initial value: H'36DB 0400 (MD = Low) Recommended value: H'1240 0400 • Idle Cycles between Write-Read Cycles and Write-Write Cycles IWW[2:0] = B'001; 1 idle cycle inserted • Idle Cycles for Another Space Read-Write IWRWD[2:0] = B'001; 1 idle cycle inserted • Idle Cycles for Read-Write in the Same Space IWRWS[2:0] = B'001; 1 idle cycle inserted • Data bus width BSZ[1:0] = B'10; 16-bit CS0 Space Wait Control Register (CS0WCR): Initial value: H'0000 0500 Recommended value: H'0000 0B41 • Number of Delay Cycles from address, CS0# Assertion to RD#, WEn# Assertion: SW[1:0] = B'01; 1.5 cycles • Number of Access Wait Cycles WR[3:0] = B'0110; 6 cycles • External WAIT Mask Specification WM = B'1; Ignore external WAIT input • Number of Delay Cycles from RD#, WEn# Negation to address, CS0# Negation HW[1:0] = B'01; 1.5 cycles

2.3.3 External SDRAM Interface

The M3A-HS64 comes standard with an SDRAM listed in the table below. The SDRAM is controlled by the SH7264 on-chip Bus State Controller (BSC). The M3A-HS64 allows 16-bit bus access only.

The figure below shows the SDRAM block diagram, and Table 2.3.5 lists the DIP switches setting (SW5-4).

Table 2.3.4 SDRAM Specifications

Item	Description
Part number	EDS1216AHTA-75E
Configuration	16 MB (Bus size: 16-bit) x 1
Capacity	16 MB
Access time	7.5 ns
CAS latency	2 (When the system clock works at 72 MHz)
Refresh	4096 cycles every 64 ms
Row address	A11 to A0
Column address	A8 to A0
Number of banks	4 (controlled by BA0, and BA1)

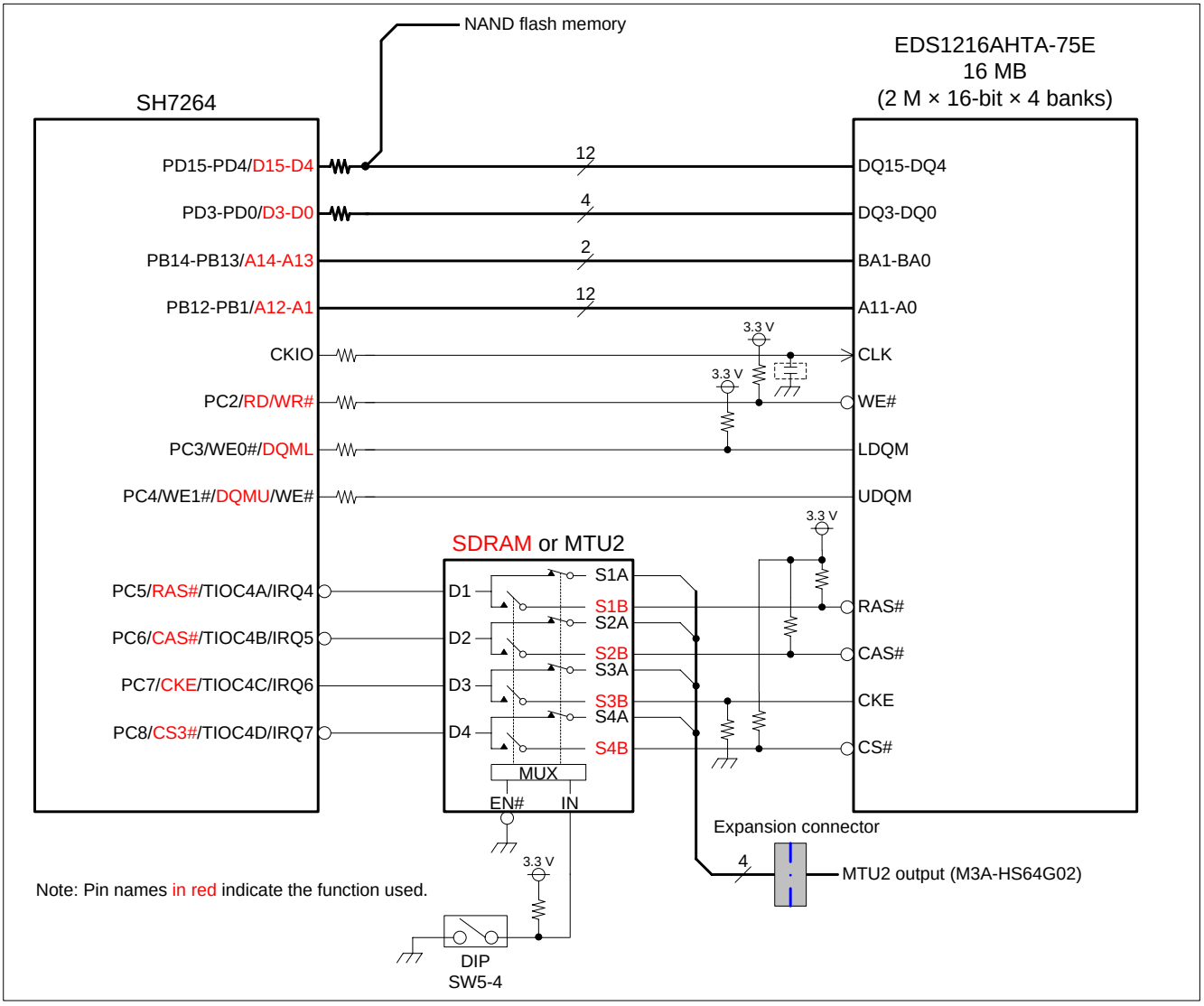

Figure 2.3.3 External SDRAM Block Diagram

Table 2.3.5 DIP Switches Setting (SW5-4)

Number	Function	
	OFF(High)	ON (Low)
SW5-4	Connected to the SDRAM (default)	Connected to the MTU2 interface

The following figure shows the single read and write timing example of the SDRAM. Table 2.3.6 lists the bus state controller setting when the SH7264 bus clock works at 72 MHz.

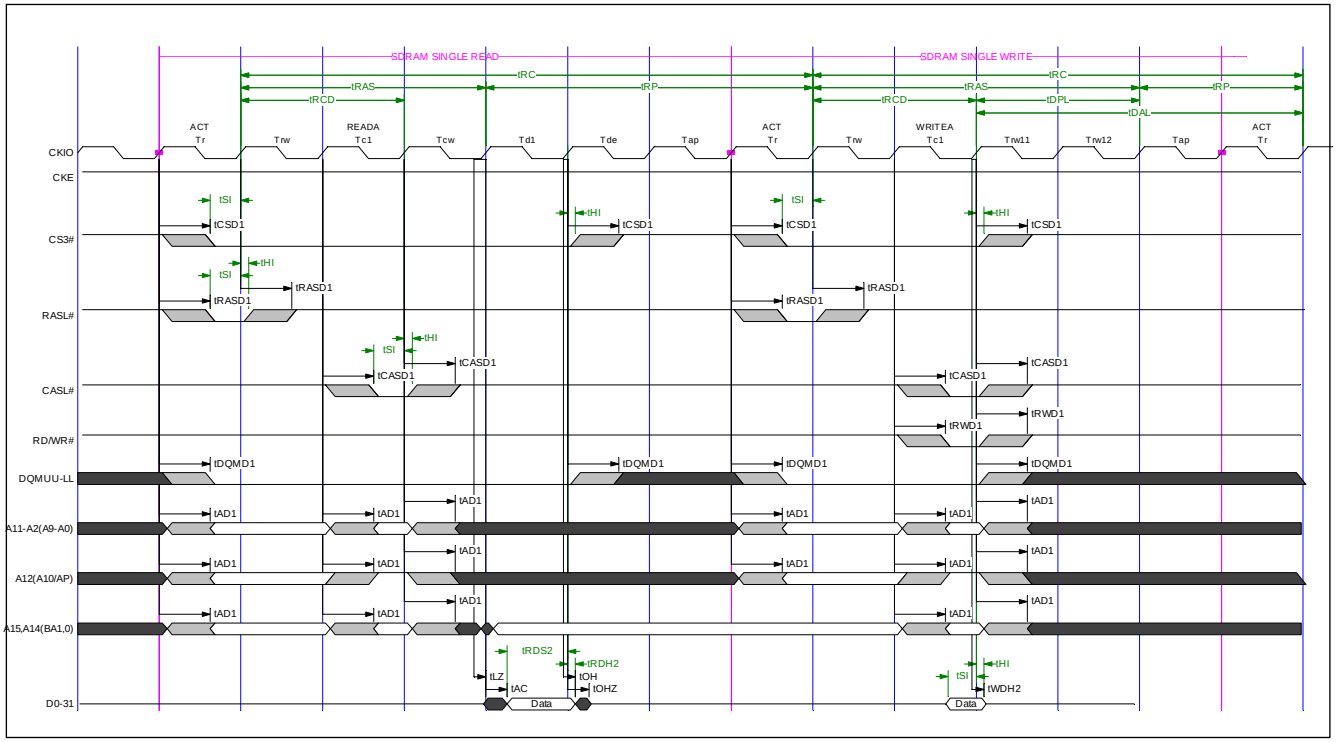

Figure 2.3.4 SDRAM Single Read/Write Timing Example

Table 2.3.6 Bus State Controller Setting (Read and Write the SDRAM)

User Area	Target Device	Setting
CS3	EDS1216AHTA-75E	CS3 space bus control register (CS3BCR): Initial value: H'36DB 0400 Recommended value: H'0000 4400 • Memory TYPE[2:0] = B'100; SDRAM • Data bus width BSZ[1:0] = B'10; 16-bit CS3 space wait control register (CS3WCR): Initial value: H'0000 0500, Recommended value: H'0000 288A • Number of Auto-Precharge Completion Wait Cycles: WTRP[1:0] = B'01; 1 cycle • Number of Wait Cycles between ACTV Command and READ (A)/WRIT(A) Command WTRC [1:0] = B'10; 2 cycles • CAS Latency for Area 3 A3CL[1:0] = B'01; 2 cycles • Number of Auto-Precharge Startup Wait Cycles TRWL[1:0] = B'01; 1 cycle • Number of Idle Cycles from REF Command/Self-Refresh Release to ACTV/REF/MRS Command: WTRC [1:0] = B'10; 5 cycles SDRAM control register (SDCR): Initial value: H'0000 0000, Recommended value: H'0000 0809 • Refresh Control RFSH = B'1; SDRAM is refreshed • Refresh Control RMODE = B'0; Auto-refreshed • Bank Active Mode BACTV = B'0; Auto-precharge mode • Number of Bits of Row Address for Area 3 A3ROW[1:0] = B'01; 12 bits • Number of Bits of Column Address for Area 3 A3COL[1:0] = B'01; 9 bits Refresh Timer Control/Status Register (RTCSR): Initial value: H'0000 0000, Recommended value: H'A55A 0010 • Clock Select CKS[2:0] = B'010; BΦ/16 • Refresh Count RRC[2:0] = B'000; 1 time Refresh Time Constant Register (RTCOR): Initial value: H'0000 0000, Recommended value: H'A55A 0046 The refresh request interval when the clock select is set to BΦ/16 is as follows: 1 cycle: 222 nsec (72 MHz/16 = 4.5 MHz) Refresh request interval in this SDRAM: 15.625 µsec/time 15.625 usec/222 nsec = 70 (0x46) cycles/refresh counts

2.3.4 NAND Flash Memory Interface

The M3A-HS64 comes standard with an NAND flash memory listed in the table below.

NAND flash memory works at 8-bit mode, and 3.3 V-only single power supply. It is write-protected or write-enabled by system setting DIP switches.

The SH7264 NAND flash memory controller pin (FLCTL) is also used as the data bus (D15 to D4) and the channel 0 pin of the Renesas Serial Peripheral Interface (RSPI). When connecting it with NAND flash memory, set SW5-5 to OFF. The figure below shows the NAND flash memory block diagram. Table 2.3.8 lists the DIP switches setting (SW5-5, and SW6-2).

Table 2.3.7 NAND Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
K9F2G08U0A-PCB0	8-bit	256 MB (8-bit x 256 M Words x 1)	Random: 25 µs (max.) Page: 25 ns (min.)

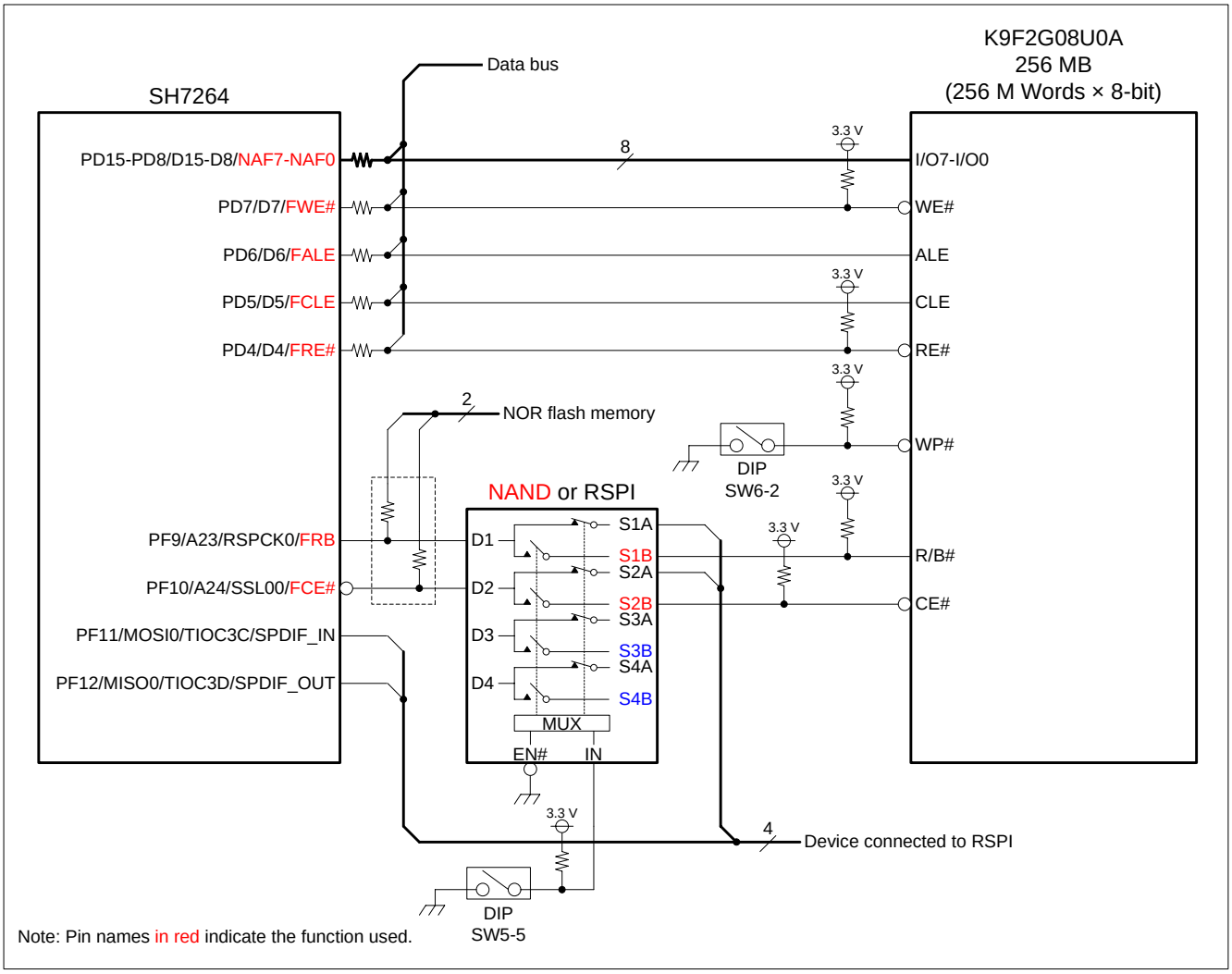

Figure 2.3.5 NAND Flash Memory Block Diagram

Table 2.3.8 DIP Switches Setting (SW5-5, and SW6-2)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI (default)
SW6-2	NAND flash memory is write-enabled (default)	NAND flash memory is write-protected

2.3.5 External Serial Flash Memory Interface

The M3A-HS64 comes standard with a serial flash memory listed in the table below. The serial flash memory is controlled by the RSPI built in the SH7264.

The SH7264 RSPI channel 0 pin is also used as the FLCTL pin. When connecting it with serial flash memory, set SW5-5 to ON, and SW6-6 to OFF.

Serial flash memory is write-protected or write-enabled by the system setting DIP switches.

The figure below shows the serial flash memory block diagram. Table 2.3.10 lists the DIP switch setting (SW5, and SW6).

Table 2.3.9 Serial Flash Memory Specifications

Part Number	Interface	Capacity	Package
AT26DF161A-SU	4-wire serial (RSPI)	2 MB	8-pin, SOP

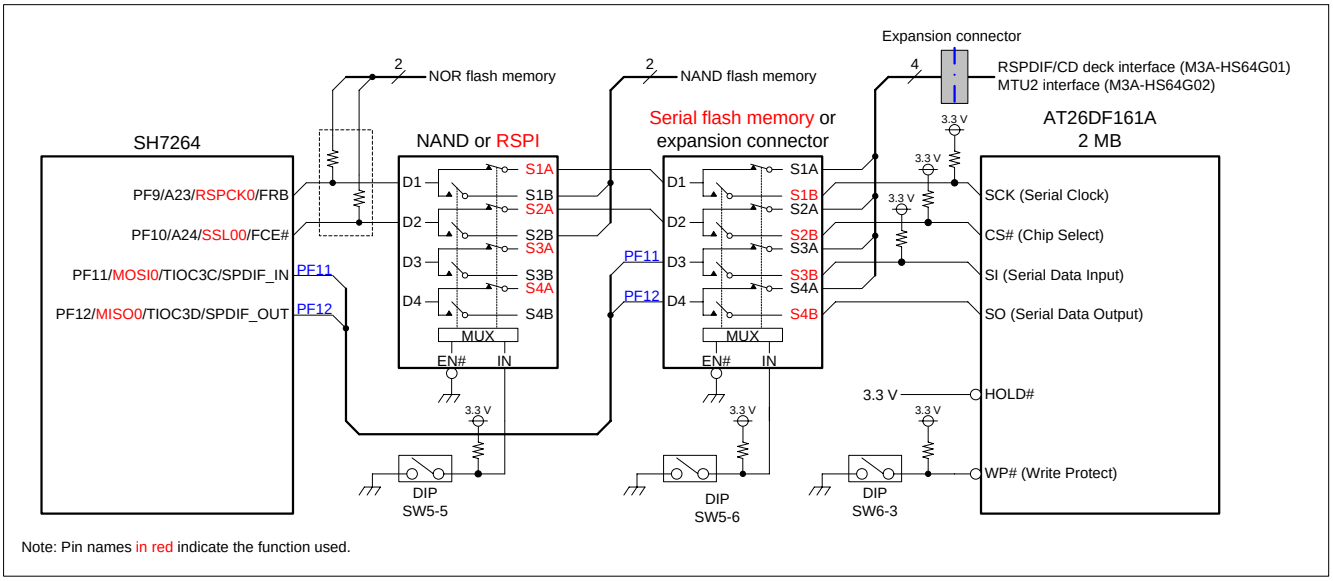

Figure 2.3.6 Serial Flash Memory Interface Block Diagram

Table 2.3.10 DIP Switches Setting (SW5, and SW6)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI (default)
SW5-6	Connected to the serial flash memory	Connected to the expansion connector (CD deck/RSPDIF/MTU2 - default)
SW6-3	Serial flash memory is write-enabled (default)	Serial flash memory is write-protected

2.3.6 External EEPROM Interface

The M3A-HS64 comes standard with an EEPROM listed in the table below. The EEPROM is controlled by the IIC bus interface 3 (IIC3) built in the SH7264.

The EEPROM is write-protected or write-enabled by system setting DIP switches.

The figure below shows the EEPROM Interface Block Diagram. Table 2.3.12 lists the DIP switches setting (SW6-4), and Table 2.3.13 lists the jumpers setting (JP8, and JP9).

Table 2.3.11 EEPROM Specifications

Part Number	Interface	Capacity	Package
HN58X24128FPIE	2-wire serial (IIC)	16 KB (16 kwords x 8-bit)	8-pin, SOP

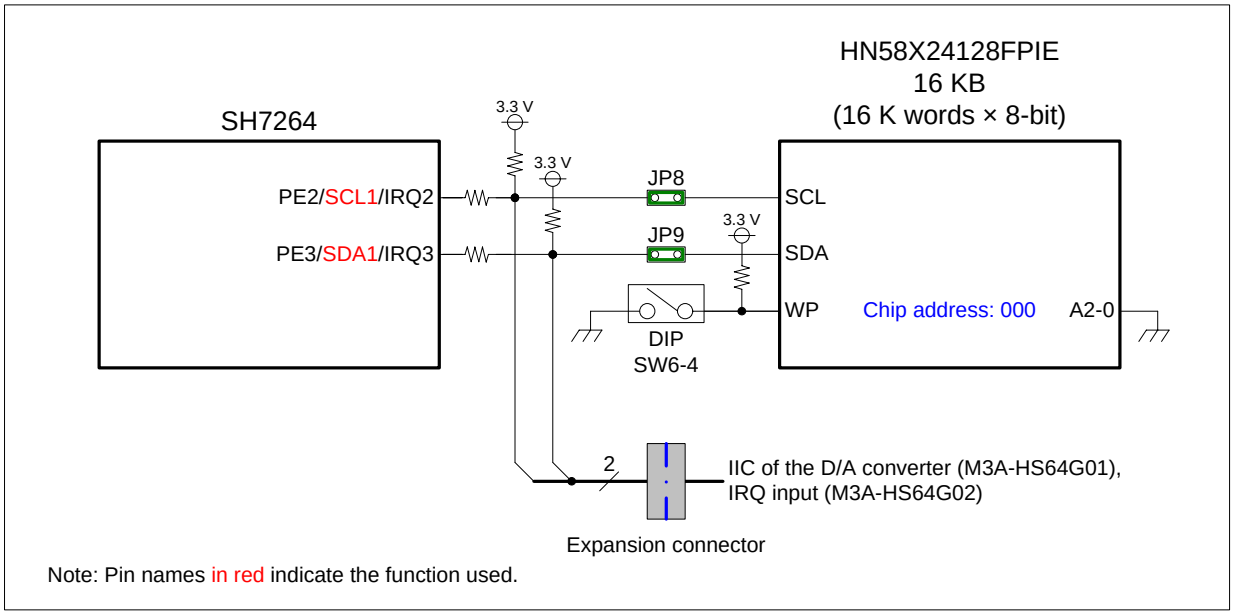

Figure 2.3.7 EEPROM Interface Block Diagram

Table 2.3.12 DIP Switches Setting (SW6-4)

Number	Function	
	OFF (High)	ON (Low)
SW6-4	EEPROM is write-protected	EEPROM is write-enabled (default)

Table 2.3.13 Jumpers Setting (JP8, and JP9)

Number	1-2	None (Open)
JP8	IIC3 mode (PE2 is SCL1 output pin, default)	IRQ mode (PE2 is IRQ2 input pin)
JP9	IIC3 mode (PE3 is SDA1 I/O pin, default)	IRQ mode (PE3 is IRQ3 input pin)

2.4 USB Interface

The M3A-HS64 comes standard with a USB Series-A receptacle. The wiring pattern on the M3A-HS64 allows for connecting a Mini-B receptacle to evaluate the USB host and function modules. Remove the series-A receptacle to connect a USB mini-B receptacle. The figure below shows the USB interface block diagram. The table below lists the jumper settings (JP10).

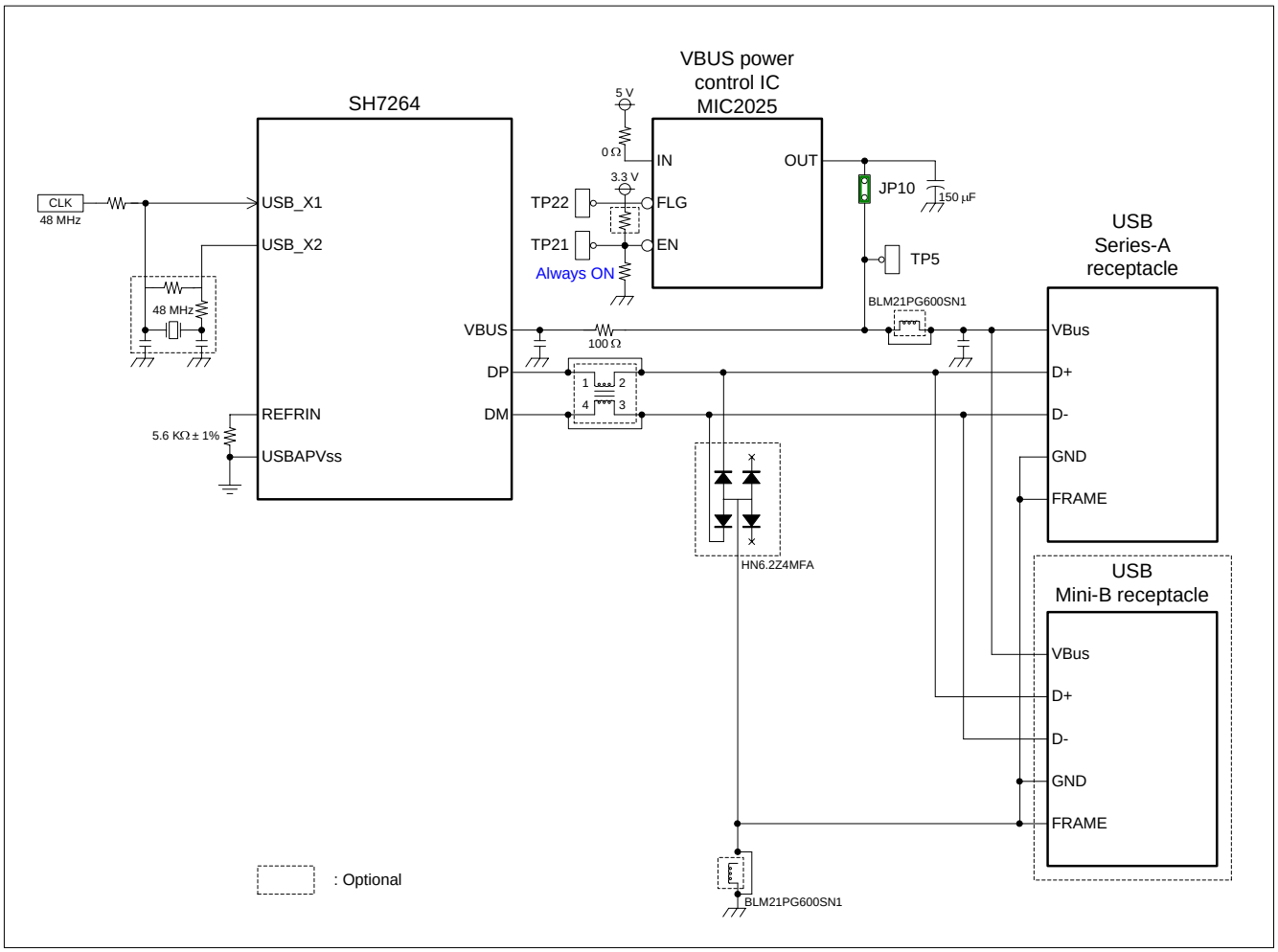

Figure 2.4.1 USB Interface Block Diagram

Table 2.4.1 Jumper Setting (JP10)

Number	1-2	None (Open)
JP10	USB host mode (Supplies the VBUS power, default)	USB function mode (Does not supply the VBUS power)

2.5 RS-232C Interface

The SH7264 includes a serial communication interface with FIFO (SCIF). D-sub 9-pin connector on the M3A-HS64 is connected to the SH7264 SCIF channel 0 pin via an RS-232C driver IC.

The SH7264 SCIF channel 0 pin is also used as the channel 0 pin of the Controller Area Network (RCAN-TL1).

The following figure shows the RS-232C interface block diagram. The table below lists the jumpers setting (JP4, and JP5).

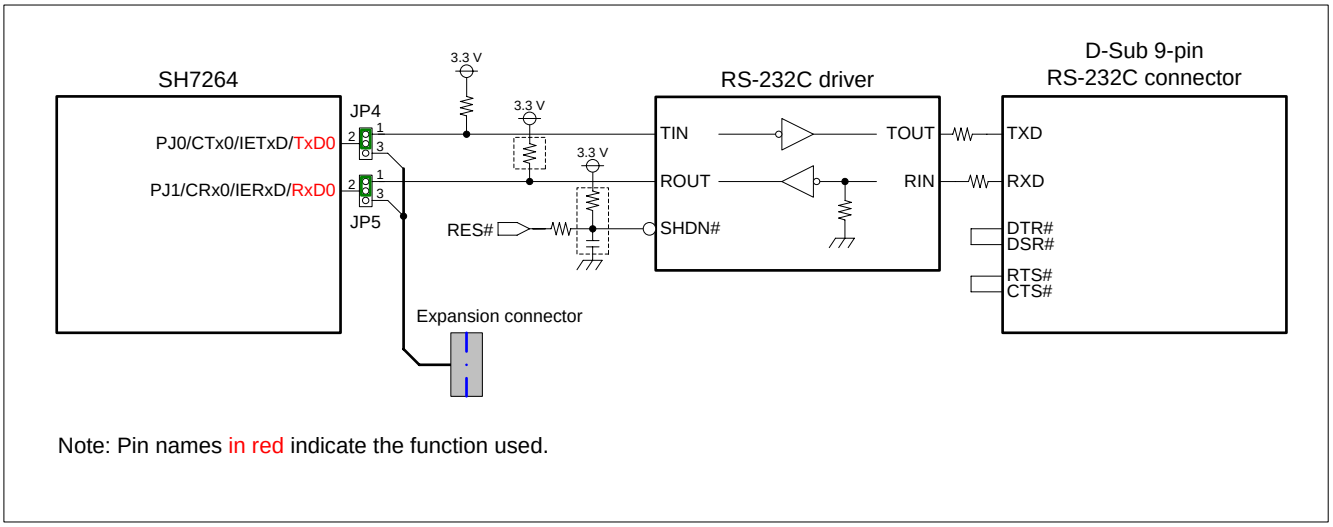

Figure 2.5.1 RS-232C Interface Block Diagram

Table 2.5.1 Jumpers Setting (JP4, and JP5)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) /IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) /IERxD (IEB) pins

2.6 I/O Ports

SH7264 I/O ports are connected to switches and LEDs on the M3A-HS64.

Ports PH7 to PH0 can be used as analog input pins (AN7 to AN0). Remove JP15 to use PH7 to PH4 as an analog input pin.

Port A can be used as a user interface by setting PB22 pin to high output.

The following figure shows the I/O ports block diagram. Table 2.6.1 lists the jumpers setting (JP14, and JP15). Table 2.6.2 shows Port A function switching.

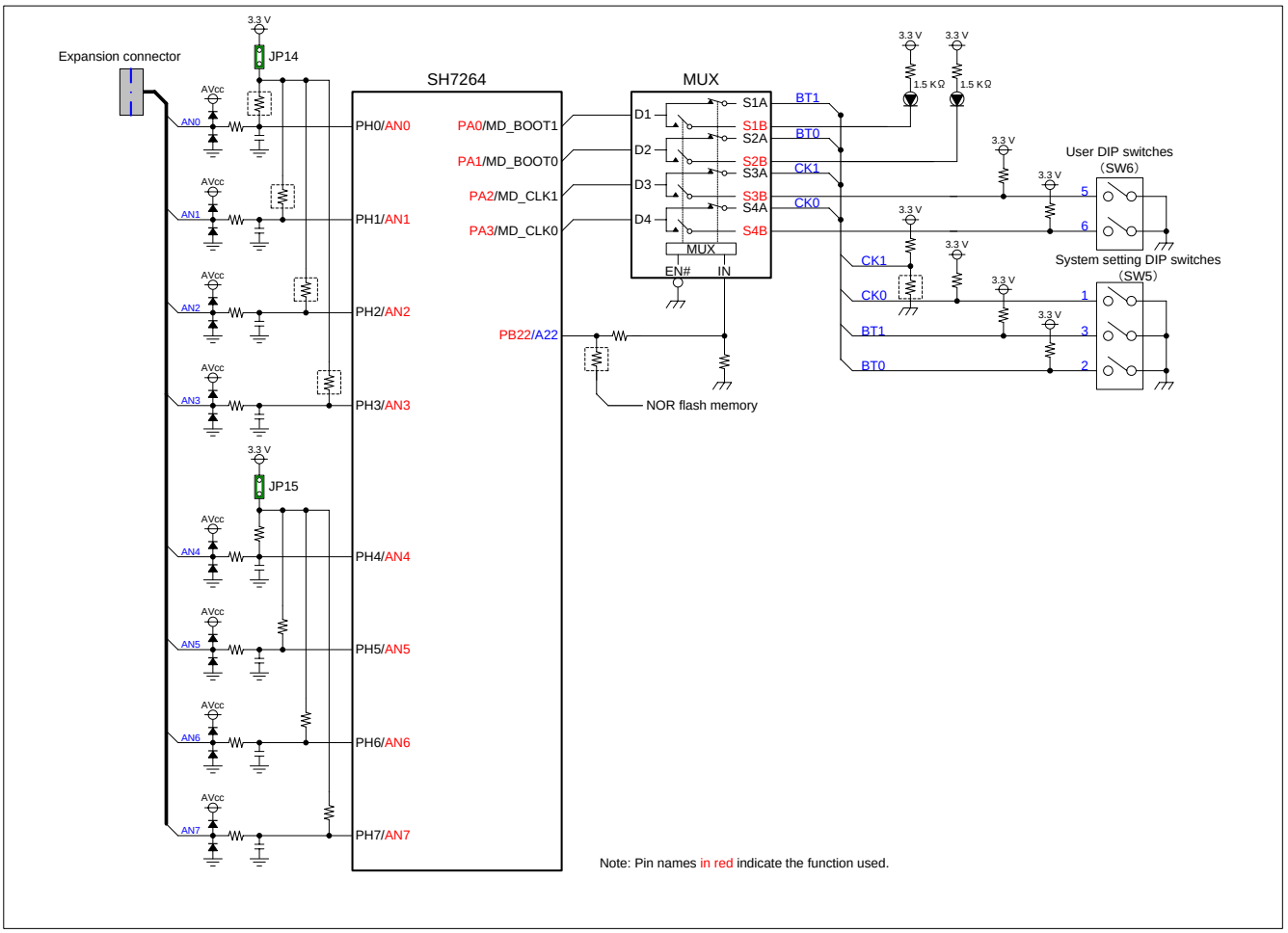

Figure 2.6.1 I/O Ports Block Diagram

Table 2.6.1 Jumpers Setting (JP14, JP15)

Number	1-2	None (Open)
JP14	Uses PH [0:3] as an input port (default) (1)	Uses PH [0:3] as an analog input pin
JP15	Uses PH [4:7] as an input port (default)	Uses PH [4:7] as an analog input pin (2)

Notes: (1) Mount R10 to R13 when using PH [0:3] as an input port.

(2) Remove R14 to R17 when using PH [4:7] as an analog input pin.

Table 2.6.2 Port A Function Switching

Number	High output	Low output
PB22	Uses Port A as a user interface	Mode sampling (At power-up)

2.7 Interrupt Switches

The M3A-HS64 includes two push-button switches (NMI switch and IRQ1 switch) for the NMI and IRQ1 interrupt signals input from the SH7264, and a push-button switch (TEST switch) for test signals.

The TEST switch is open to allow for connecting a desired pin. Set JP6 to use IRQ1 switch.

The figure below shows the interrupt switch block diagram. The table below lists the jumper setting (JP6).

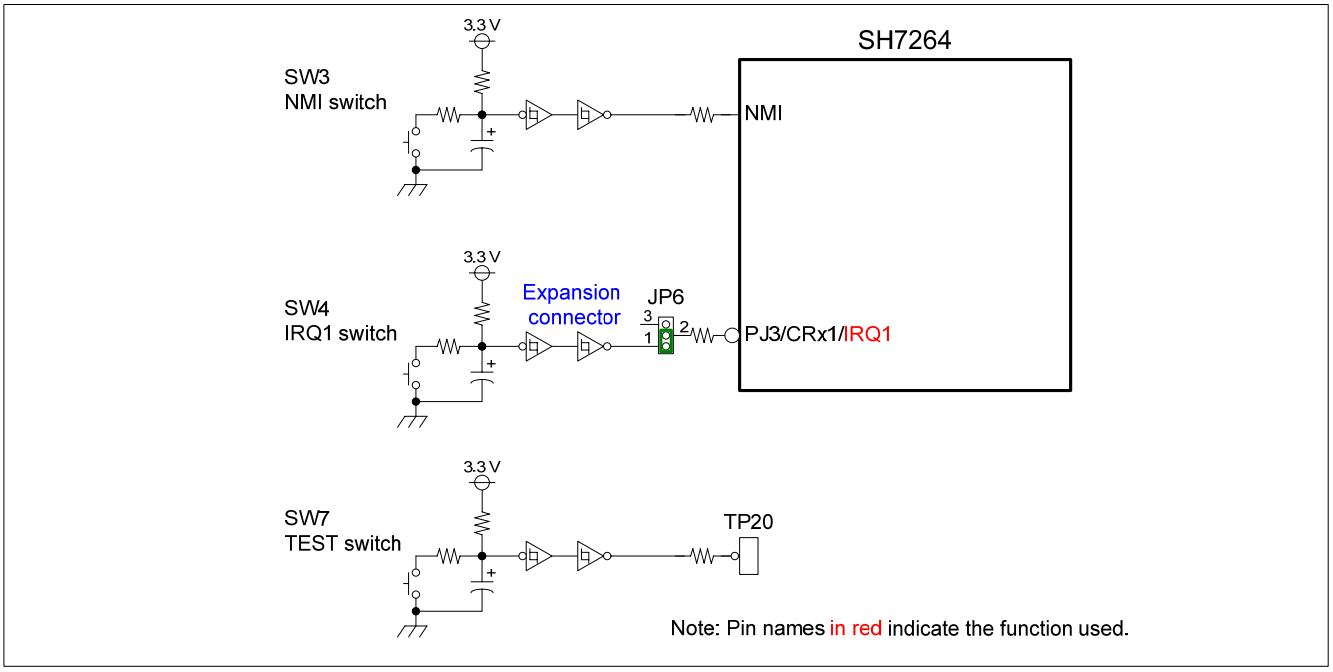

Figure 2.7.1 Interrupt Switch Block Diagram

Table 2.7.1 Jumper Setting (JP6)

Number	1-2	2-3
JP6	Uses PJ3 as the IRQ1 input pin (default)	Uses PJ3 as the CRx1 input pin

2.8 Clock Modules

Provide following clocks with the SH7264 on the M3A-HS64.

- SH7264 input clock: 18 MHz
- SH7264 RTC clock: 32.768 kHz
- SH7264 audio clock: 12.2880 MHz, and 11.2896 MHz (default)
- SH7264 USB clock: 48.00 MHz
- SH7264 LCD clock: 5.33 MHz

➢ How to select the system clock frequency of AK4353 (D/A converter), and AK4524 (audio codec)

SH7264 audio clock provides either 12.2880 MHz or 11.2896 MHz with AK4353 and AK4524 by switching JP7.

The following figure shows the clock module block diagram, and the table below lists the audio clock switching.

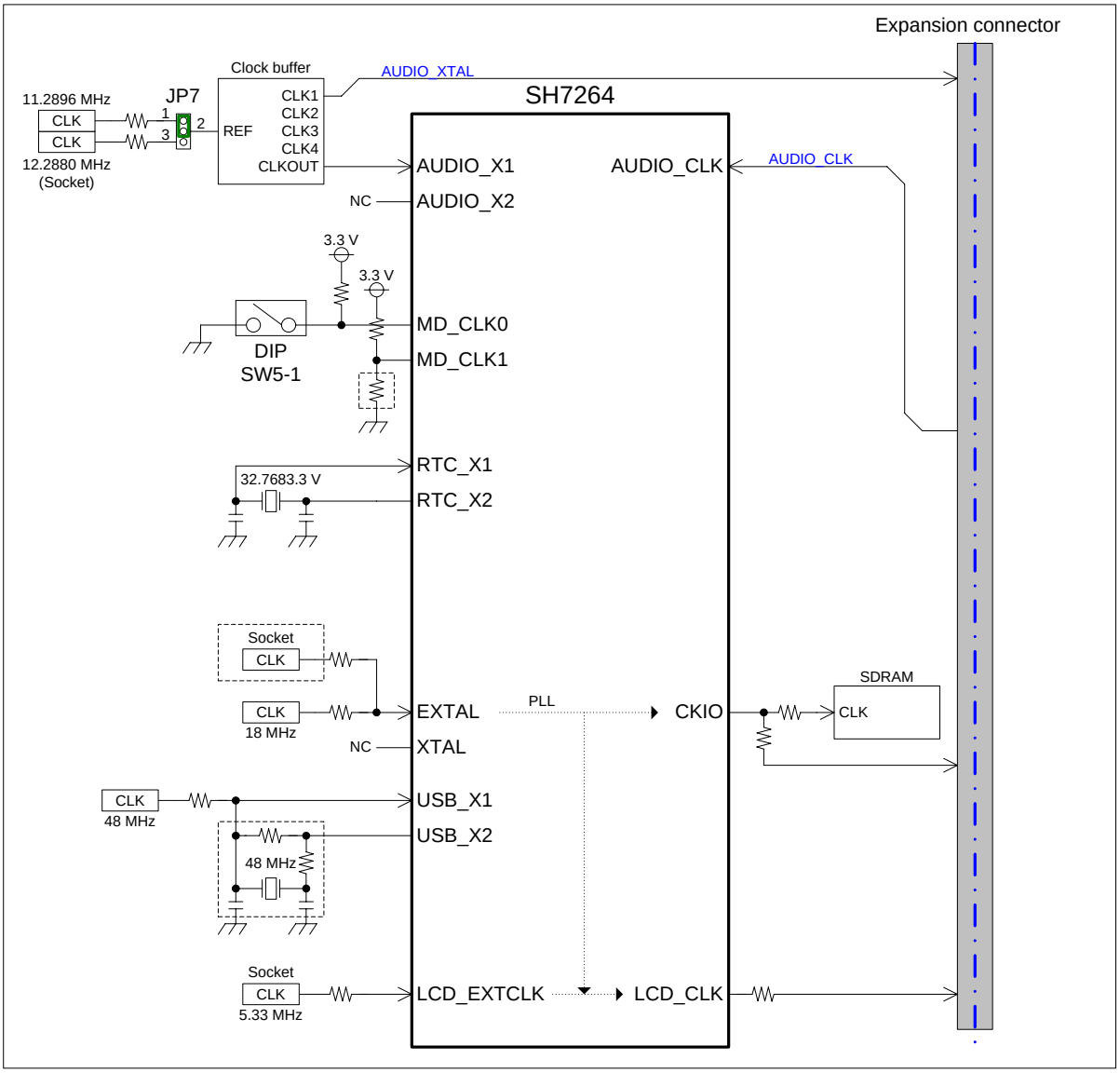

Figure 2.8.1 Clock Module Block Diagram

Table 2.8.1 Audio Clock Switching

Number	1-2	2-3
JP7	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

2.9 Reset Module

A reset IC controls reset signals connected to the SH7264, flash memory and peripheral I/Os on the M3A-HS64. There are two system reset options; power-on reset, and reset by switch.

The following figure shows the reset module block diagram.

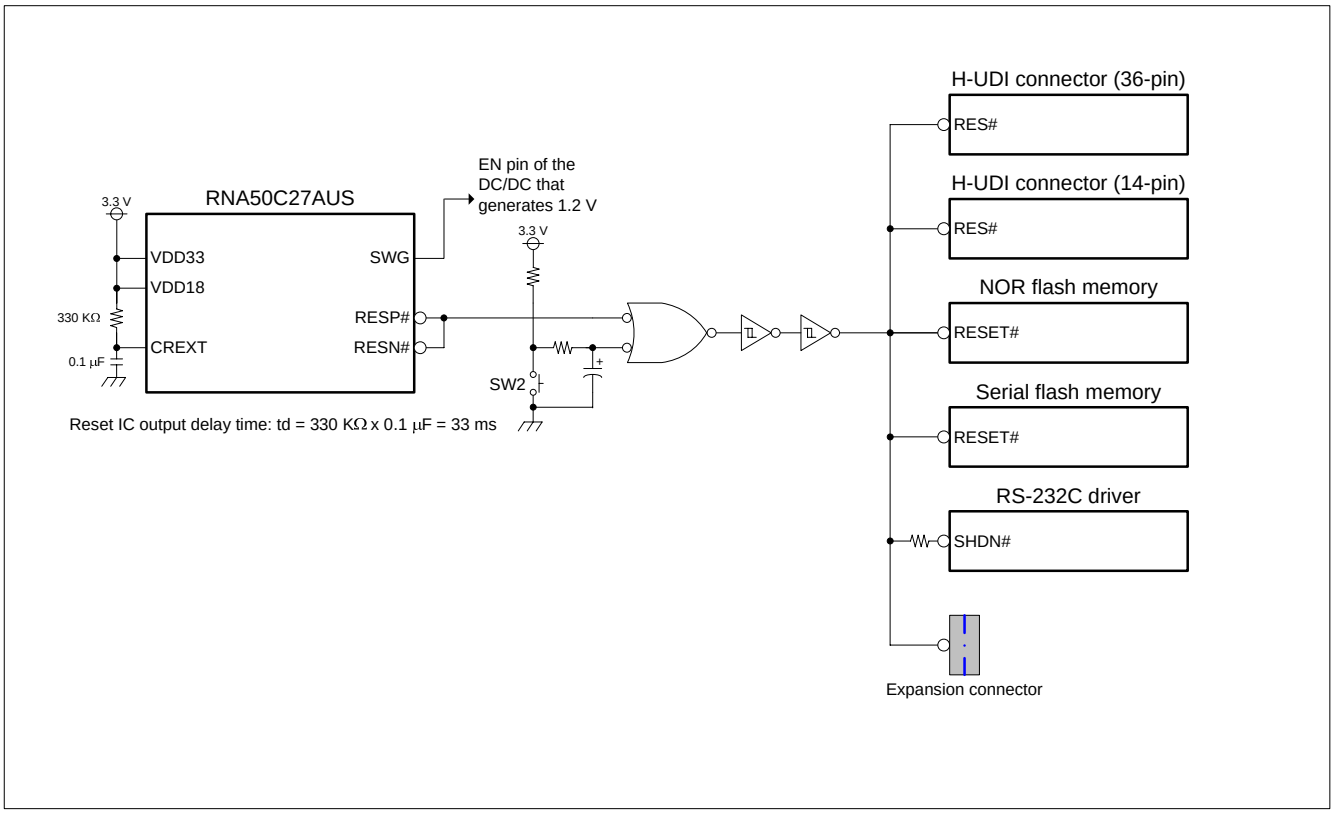

Figure 2.9.1 Reset Module Block Diagram

2.10 Power Supply Module

The M3A-HS64 is supplied 5 V power supply, the voltage regulator on the M3A-HS64 generates 3.3 V voltage, the reference voltage for the A/D converter (3.3 V), and 1.2 V. CPU 3.3 V and 1.2 V power can be externally-supplied.

The following figure shows the power supply module block diagram.

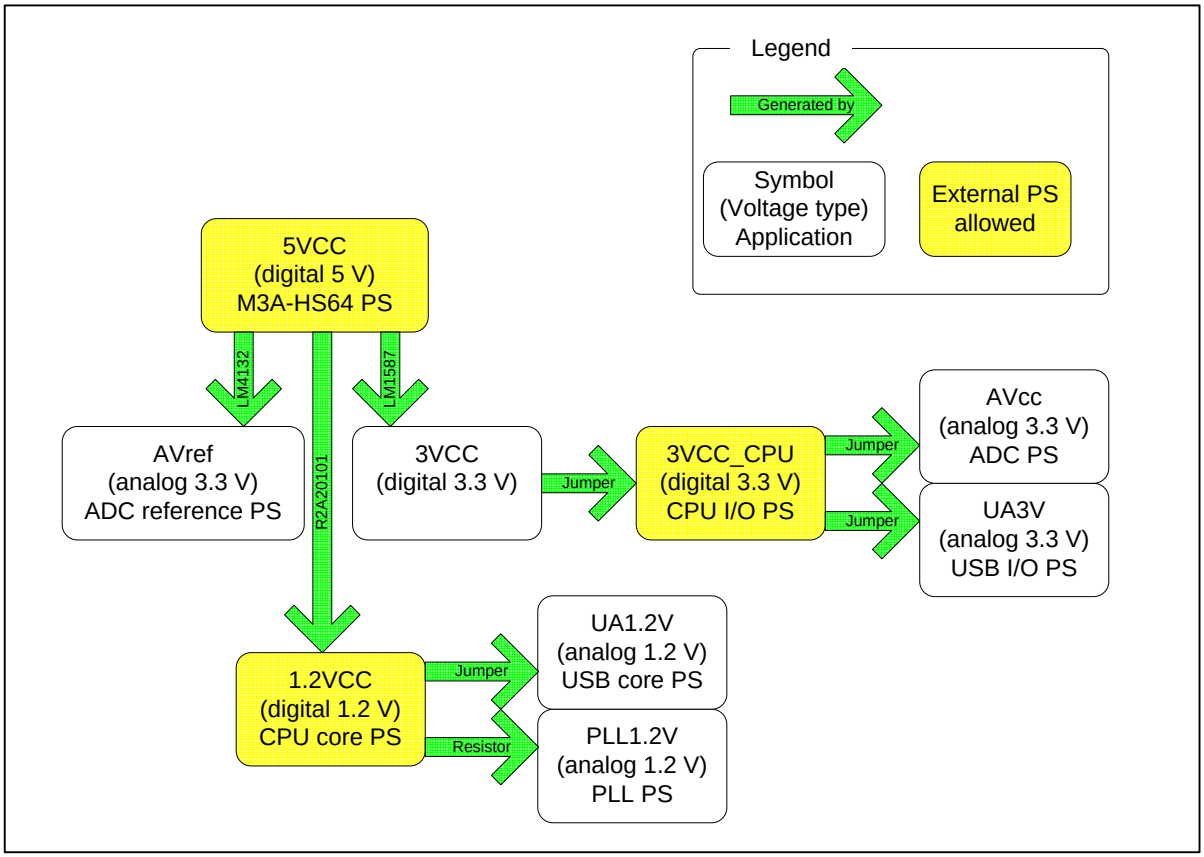

Figure 2.10.1 Power Supply Module Block Diagram

2.11 E10A-USB Interface

The M3A-HS64 includes two H-UDI connectors (14-pin and 36-pin) to connect to the E10A-USB emulator.

The AUD pin is also used as SSIF (Serial Sound Interface with FIFO) pin, and VDC3 (Video Display Controller 3) pin.

AUD function can be used when the M3A-HS64 is used only. (Do not use the AUD function when connecting optional boards.)

When using AUD function, set the AUDCK frequency to 30 MHz or lower.

The following figure shows the E10A-USB interface block diagram.

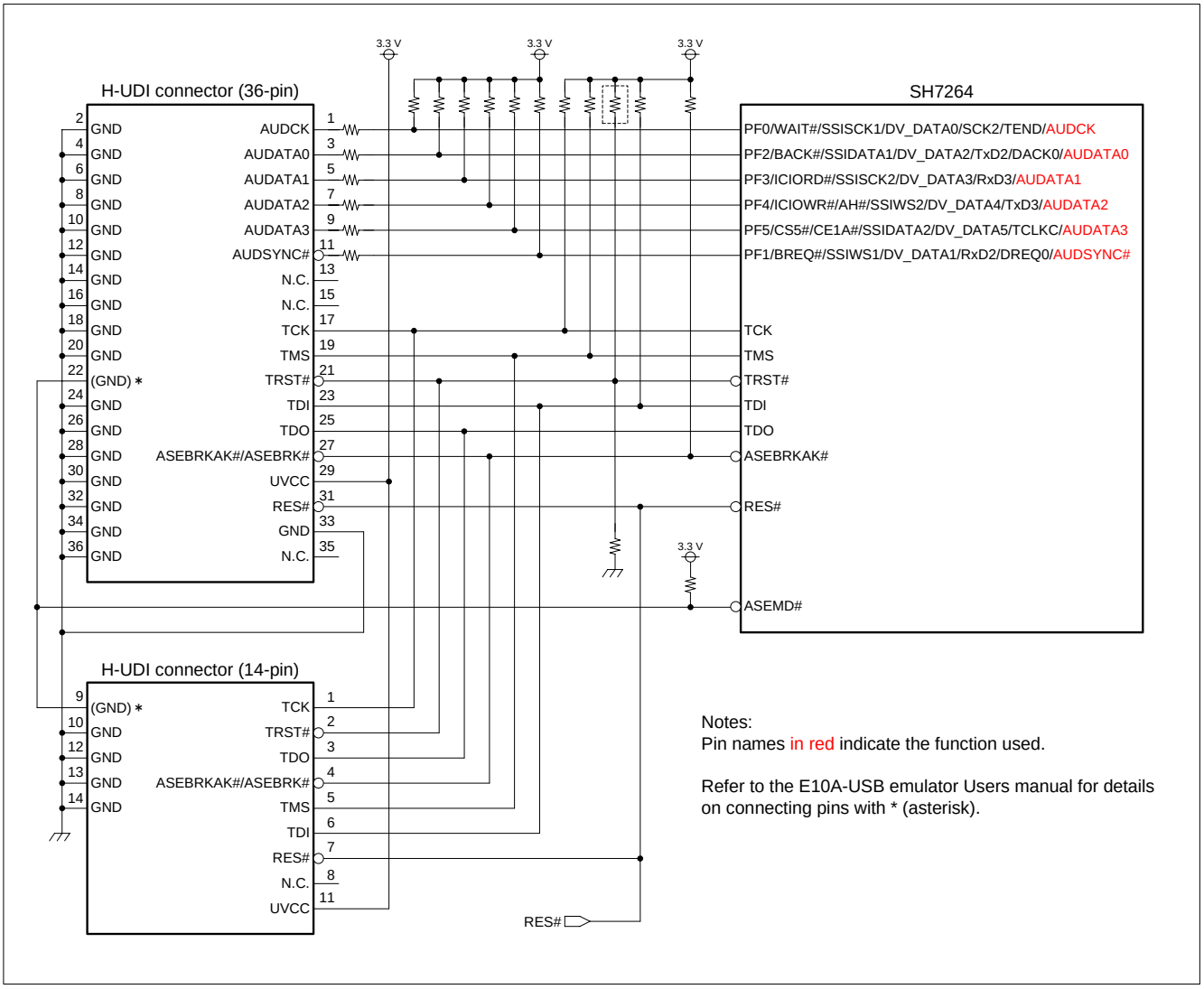

Figure 2.11.1 E10A-USB Interface Block Diagram

Chapter 3
M3A-HS64G01 Functions

3.1 Overview of Functions

M3A-HS64G01 includes the function modules listed in the following table.

Table 3.1.1 M3A-HS64G01 Function Modules

Section	Function	Description
3.2	CPU	• SH7264
3.3	LCD Module Interface	• LCD module interface - Connects the SH7264 Video Display Controller 3 (VDC3) and LCD module connectors - Flexible connectors for LCD module are included • Character LCD module with LED backlight
3.4	Audio Modules	• Connects the SH7264, D/A converters, and an audio codec - 96 kHz 24-bit D/A converters: 2 - 24-bit stereo codec with microphone AMP: 1
3.5	CD Deck Interface	• Connects RSPI, SSIF and a CD deck
3.6	SD Card Interface	• Connects the SH7264 SD Host Interface (SDHI) and an SD card slot
3.7	UART Interface	• Connects the SH7264 Serial Communication Interface with FIFO (SCIF) and a UART connector
3.8	CAN Interface	• Connects the SH7264 Controller Area Network (RCAN-TL1) and a CAN connector
3.9	IEBus™ Interface	• Connects the SH7264 IEBus™ controller (IEB) and IEBus™ connector
3.10	I/O Ports	• Connect the SH7264 I/O ports, LEDs, and DIP switches
3.11	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
3.12	Reset Module	• Resets devices on the M3A-HS64G01
3.13	Power Supply Module	• Controls the M3A-HS64G01 system power supply
-	Operating Specifications	• Connectors, switches, and LEDs Refer to Chapter 6 for details.

3.2 CPU

3.2.1 SH7264 Overview

The M3A-HS64 includes the SH7264, the 32-bit RISC MCU that operates with a maximum frequency of 144 MHz.

3.2.2 SH7264 Pin Functions Used on the M3A-HS64G01

Table 3.2.1 to Table 3.2.6 list the SH7264 pin functions used on the M3A-HS64G01.

Table 3.2.1 SH7264 Pin Functions (1/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
1	PC2/RD/WR#	RD/WR#	Connected to the SDRAM WE# pin	CN6, pin 7	
2	PC3/WE0#/DQML	WE0#	Connected to the NOR flash memory WE# pin	CN6, pin 8	
		DQML	Connected to the SDRAM DQML pin		
3	Vss				
4	PC4/WE1#/DQMU/WE#	DQMU	Connected to the SDRAM DQMU pin	CN6, pin 9	
5	PVcc				
6	PC9/TIOC2A	PC9	Connected to the RS pin of the character LCD	CN6, pin 12	
7	PC10/TIOC2B	PC10	Connected to the E pin of the character LCD	CN6, pin 13	
8	PC5/RAS#/TIOC4A/IRQ4	RAS#	Connected to the SDRAM RAS# pin	-	SW5-4: OFF
		-	-	CN6, pin 14	SW5-4: ON
9	PC6/CAS#/TIOC4B/IRQ5	CAS#	Connected to the SDRAM CAS# pin	-	SW5-4: OFF
		-	-	CN6, pin 15	SW5-4: ON
10	Vcc				
11	PC7/CKE/TIOC4C/IRQ6	CKE	Connected to the SDRAM CKE pin	-	SW5-4: OFF
		-	-	CN6, pin 16	SW5-4: ON
12	Vss				
13	PC8/CS3#/TIOC4D/IRQ7	CS3#	Connected to the SDRAM CS pin	-	SW5-4: OFF
		-	-	CN6, pin 17	SW5-4: ON
14	PVcc				
15	PB1/A1	A1	Address bus	CN4, pin 1	
16	PB2/A2	A2	Address bus	CN4, pin 2	
17	PB3/A3	A3	Address bus	CN4, pin 3	
18	PB4/A4/TIOC0A	A4	Address bus	CN4, pin 4	
19	PB5/A5/TIOC0B	A5	Address bus	CN4, pin 5	
20	PB6/A6/TIOC0C	A6	Address bus	CN4, pin 6	
21	PB7/A7/TIOC0D	A7	Address bus	CN4, pin 9	
22	Vcc				
23	PB8/A8/TIOC1A	A8	Address bus	CN4, pin 10	
24	Vss				
25	PB9/A9/TIOC1B	A9	Address bus	CN4, pin 11	
26	PVcc				
27	PB10/A10/TIOC2A	A10	Address bus	CN4, pin 12	
28	PB11/A11/TIOC2B	A11	Address bus	CN4, pin 13	
29	PB12/A12/TIOC3A	A12	Address bus	CN4, pin 14	
30	PB13/A13/TIOC3B	A13	Address bus	CN4, pin 17	
31	PB14/A14/TIOC3C	A14	Address bus	CN4, pin 18	
32	PB15/A15/TIOC3D	A15	Address bus	CN4, pin 19	
33	Vcc				
34	PB16/A16/TIOC4A	A16	Address bus	CN4, pin 20	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 3.2.2 SH7264 Pin Functions (2/6)

No	Name	Symbol	Description	Expansion connector	Remarks
35	Vss				
36	CKIO	CKIO	Connected to the SDRAM CLK pin	CN6, pin 20	
37	PVcc				
38	PB17/A17/TIOC4B	A17	Address bus	CN4, pin 21	
39	PB18/A18/TIOC4C	A18	Address bus	CN4, pin 22	
40	PB19/A19/TIOC4D	A19	Address bus	CN4, pin 25	
41	PB20/A20	A20	Address bus	CN4, pin 26	
42	PB21/A21	A21	Address bus	CN4, pin 27	
43	PB22/A22/CS4#	PB22	Switches the system setting/user interface	CN4, pin 28	Low: MD Hi: IO
44	PJ11/PWM2H/DACK1	-	-	CN1, pin 1	
45	Vcc				
46	PJ10/PWM2G/DREQ1	PJ10	Connected to the TRANS pin of the CD deck	CN1, pin 2	
47	Vss				
48	PJ9/PWM2F/TEND1	PJ9	Connected to FLAG6 pin of the CD deck	CN1, pin 4	
49	PVcc				
50	PJ8/PWM2E/RTS3#	RTS3#	Connected to the UART connector (J10)	CN1, pin 5	TTL level
51	RES#	RES#	Reset input	CN7, pin 6	
52	NMI	NMI	Non-maskable interrupt	-	
53	PLLVcc				
54	PA3/MD_CLK0	PA3	Connected to SW6-6 as the user input port	CN1, pin 7	PB22: High
		MD_CLK0	Connected to SW5-1 as the clock mode input 0		PB22: Low
55	PLLVss				
56	PA2/MD_CLK1	PA21	Connected to SW6-5 as the user input port	CN1, pin 8	PB22: High
		MD_CLK1	Fixed high as the clock mode input 1		PB22: Low
57	EXTAL	EXTAL	Connects the system external clock to MCU	-	18 MHz
58	XTAL	XTAL	Open	-	
59	PA1/MD_BOOT0	PA1	Connected to LED3 as the user output port	CN1, pin 9	PB22: High
		MD_BOOT0	Connected to SW5-2 as the boot mode input 0		PB22: Low
60	PA0/MD_BOOT1	PA0	Connected to LED2 as the user output port	CN1, pin 10	PB22: High
		MD_BOOT1	Connected to SW5-3 as the boot mode input 1		PB22: Low
61	PJ7/TIOC1B/CTS3#	CTS3#	Connected to the UART connector (J10)	CN1, pin 12	TTL level
62	PJ6/TIOC1A/SCK3	SCK3	Connected to the UART connector (J10)	CN1, pin 13	TTL level
63	PJ5/IERxD/TxD3	TxD3	Connected to the UART connector (J10)	CN1, pin 14	TTL level
64	Vss				
65	PJ4/IETxD/RxD3	RxD3	Connected to the UART connector (J10)	CN1, pin 15	TTL level
66	PVcc				
67	RTC_X1	RTC_X1	Connects the real-time clock resonator to MCU	-	32.768 kHz
68	RTC_X2	RTC_X2		-	
69	Vss				
70	PJ3/CRx1/CRx0/CRx1/IRQ1	IRQ1	IRQ1 switch	-	JP6: 1-2
		CRx1	Connected to the CAN driver IC (U16)	CN1, pin 17	JP6: 2-3
71	PJ2/CTx1/CTx0&CTx1/CS2# /SCK0/LCD_M_DISP	CTx1	Connected to the CAN driver IC (U16)	CN1, pin 18	
		LCD_M_DISP	LCD AC control signal		
72	Vcc				
73	PJ1/CRx0/IERxD/IRQ0/RxD0	RS-232C	Connected to the RS-232C connector (J10)	CN1, pin 19	JP5: 1-2
		CRx0	Connected to the CAN driver IC (U14)		JP5: 2-3
		IERxD	Connected to the IEBus™ driver IC		
74	Vss				
75	PJ0/CTx0/IETxD/CS1#/TxD0 /A0	TxD0	Connected to the RS-232C connector (J10)	CN1, pin 20	JP4: 1-2
		CTx0	Connected to the CAN driver IC (U14)		JP4: 2-3
		IETxD	Connected to the IEBus™ driver IC		
76	PVcc				

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 3.2.3 SH7264 Pin Functions (3/6)

No	Name	Function	Description	Expansion connector	Remarks
77	USB_X1	USB_X1	Connects the USB external clock to MCU	-	48 MHz
78	USB_X2	USB_X2	Open	-	
79	ASEMD#	ASEMD#	ASE mode select	-	H-UDI
80	USBDPVcc				
81	USBDPVss				
82	DM	DM	USB differential signal D- data	-	
83	DP	DP	USB differential signal D+ data	-	
84	VBUS	VBUS	VBUS input	-	
85	USBDVcc				
86	USBDVss				
87	REFRIN	REFRIN	Reference input	-	Connects a 5.6 kΩ ± 1% resistor
88	USBAPVcc				
89	USBAPVss				
90	USBAVcc				
91	USBAVss				
92	USBUVcc				
93	USBUVss				
94	PH0/AN0	AN0	Connected to the push-button switch as key input	CN3, pin 4	
95	PH1/AN1	AN1	Connected to the push-button switch as key input	CN3, pin 3	
96	PH2/AN2	AN2	Connected to the push-button switch as key input	CN3, pin 8	
97	PH3/AN3	AN3	Connected to the push-button switch as key input	CN3, pin 7	
98	PH4/AN4	-	-	CN3, pin 12	
99	PH5/AN5	-	-	CN3, pin 11	
100	AVss				
101	PH6/AN6	-	-	CN3, pin 16	
102	AVref				
103	PH7/AN7	AN7	Connected to the TMZ pin of the LCD module	CN3, pin 15	
104	AVcc				
105	TRST#	TRST#	Initialization-signal input pin	-	H-UDI
106	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Brake mode acknowledge	-	H-UDI
		ASEBRK#	Brake request		
107	TDO	TDO	Test data output	-	H-UDI
108	TDI	TDI	Test data input	-	H-UDI
109	TMS	TMS	Test mode select	-	H-UDI
110	TCK	TCK	Test clock	-	H-UDI
111	PG24/MISO1/TIOC0D	PG24	Connected to the PDN# pins of AK4524 and AK4353	CN9, pin 29	
112	PG23/MOSI1/TIOC0C	MOSI1	Connected to the CDTI pin of AK4524 (U6)	CN9, pin 30	
113	PVcc				
114	PG22/SSL10/TIOC0B	SSL10	Connected to the CS pin of AK4524 (U6)	CN9, pin 27	
115	Vss				
116	PG21/RSPCK1/TIOC0A	RSPCK1	Connected to the CCLKI pin of AK4524 (U6)	CN9, pin 28	
117	Vcc				
118	PG20/LCD_EXTCLK/ MISO1/TxD7	LCD_EXTCLK	Connects the LCD module external clock to MCU	CN9, pin 26	Default: 5.33 MHz
119	PG19/LCD_CLK/ TIOC2B/MOSI1/RxD7	LCD_CLK	Connected to the CLK pin of the LCD module	CN9, pin 23	
120	PG18/LCD_DE/TIOC2A/ SSL10/TxD6	LCD_DE	Connected to the EN pin of the LCD module	CN9, pin 24	
121	PG17/LCD_HSYNC/TIO C1B/RSPCK1/RxD6	LCD_HSYNC	Connected to the HSYNC pin of the LCD module	CN9, pin 21	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 3.2.4 SH7264 Pin Functions (4/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
122	PG16/LCD_VSYNC/TIOC1A/ TxD3/CTS1#	LCD_VSYNC	Connected to the VSYNC pin of the LCD module	CN9, pin 19	
123	PG15/LCD_DATA15/TIOC0D/ RxD3/RTS1#	LCD_DATA15	Connected to D15 pin of the LCD module	CN9, pin 20	R5
124	PG14/LCD_DATA14/TIOC0C/ SCK1	LCD_DATA14	Connected to D14 pin of the LCD module	CN9, pin 17	R4
125	PG13/LCD_DATA13/TIOC0B/ TxD1	LCD_DATA13	Connected to D13 pin of the LCD module	CN9, pin 18	R3
126	PVcc				
127	PG12/LCD_DATA12/TIOC0A/ RxD1	LCD_DATA12	Connected to D12 pin of the LCD module	CN9, pin 16	R2
128	Vss				
129	PG11/LCD_DATA11/SSITxD0/ IRQ3/TxD5/SIOFTxD	LCD_DATA11	Connected to D11 pin of the LCD module	CN9, pin 13	R1 and R0
130	Vcc				
131	PG10/LCD_DATA10/SSIRxD0/ IRQ2/RxD5/SIOFRxD	LCD_DATA10	Connected to D10 pin of the LCD module	CN9, pin 14	G5
132	PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC	LCD_DATA9	Connected to D9 pin of the LCD module	CN9, pin 11	G4
133	PG8/LCD_DATA8/SSISCK0/ RxD4/SIOFSCK	LCD_DATA8	Connected to D8 pin of the LCD module	CN9, pin 12	G3
134	PG7/LCD_DATA7/SD_CD/PINT7	LCD_DATA7	Connected to D7 pin of the LCD module	CN9, pin 9	G2
135	PG6/LCD_DATA6/SD_WP/PINT6	LCD_DATA6	Connected to D6 pin of the LCD module	CN9, pin 7	G1
136	PG5/LCD_DATA5/SD_D1/PINT5	LCD_DATA5	Connected to D5 pin of the LCD module	CN9, pin 8	G0
137	PG4/LCD_DATA4/SD_D0/PINT4	LCD_DATA4	Connected to D4 pin of the LCD module	CN9, pin 6	B5
138	PVcc				
139	PG3/LCD_DATA3/SD_CLK/ PINT3	LCD_DATA3	Connected to D3 pin of the LCD module	CN9, pin 3	B4
140	Vss				
141	PG2/LCD_DATA2/SD_CMD/ PINT2	LCD_DATA2	Connected to D2 pin of the LCD module	CN9, pin 4	B3
142	Vcc				
143	PG1/LCD_DATA1/SD_D3/PINT1	LCD_DATA1	Connected to D1 pin of the LCD module	CN9, pin 1	B2
144	PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#	LCD_DATA0	Connected to D0 pin of the LCD module	CN9, pin 2	B1, and B0
145	PK11/PWM2D/SSITxD0	SSITxD0	Connected to the SDTI pin of AK4524 (U6)	CN7, pin 37	
146	PK10/PWM2C/SSIRxD0	SSIRxD0	Connected to the SDTO pin of AK4524 (U6)	CN7, pin 38	
147	PK9/PWM2B/SSIWS0	SSIWS0	Connected to the LRCK pin of AK4524 (U6)	CN7, pin 35	
148	PK8/PWM2A/SSISCK0	SSISCK0	Connected to the BICK pin of AK4524 (U6)	CN7, pin 36	
149	AUDIO_X2	AUDIO_X2	Open	-	
150	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	-	Switched by JP7
151	PF12/BS#/MISO0/TIOC3D/ SPDIF_OUT	MISO0	Connected to the serial flash memory SO pin	-	SW5-6: OFF
		MISO0	Connected to the CDSO pin of the CD deck	CN7, pin 33	SW5-6: ON
		SPDIF_OUT	Connected to the through-hole (MH5)		
152	PVcc				
153	PF11/A25/SSIDATA3/MOSI0/ TIOC3C/SPDIF_IN	MOSI0	Connected to the serial flash memory SI pin	-	SW5-6: OFF
		MOSI0	Connected to the CDSI pin of the CD deck	CN7, pin 31	SW5-6: ON
		SPDIF_IN	Connected to the through-hole (MH4)		
154	Vss				

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 3.2.5 SH7264 Pin Functions (5/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
155	PF10/A24/SSIWS3/SSL00/ TIOC3B/FCE#	SSL00	Connected to the serial flash memory CS# pin	-	SW5-5: ON SW5-6: OFF
		SSL00	Connected to the CDFS pin of the CD deck	CN7, pin 32	SW5-5: ON SW5-6: ON
		FCE#	Connected to the NAND flash memory CE# pin	-	SW5-5: OFF
156	Vcc				
157	PF9/A23/SSISCK3/RSPCK0/ TIOC3A/FRB	RSPCK0	Connected to the serial flash memory SCK pin	-	SW5-5: ON SW5-6: OFF
		RSPCK0	Connected to the CDCK pin of the CD deck	CN7, pin 30	SW5-5: ON SW5-6: ON
		FRB	Connected to the NAND flash memory R/B# pin	-	SW5-5: OFF
158	PF8/CE2B#/SSIDATA3/DV_CLK	SSIDATA3	Connected to the IIS_DATA pin of the CD deck	CN7, pin 27	
159	PF7/CE2A#/SSIWS3/DV_DATA7/ TCLKD	SSIWS3	Connected to the IIS_LRCK pin of the CD deck	CN7, pin 28	
		TCLKD	Connected to the through-hole (MH11)		
160	PF6/CS6#/CE1B#/SSISCK3/ DV_DATA6/TCLKB	SSISCK3	Connected to the IIS_BCK pin of the CD deck	CN7, pin 25	
		TCLKB	Connected to the through-hole (MH9)		
161	PF5/CS5#/CE1A#/SSIDATA2/ DV_DATA5/TCLKC/AUDATA3	AUDATA3	Connected to the H-UDI connector (J3)	CN7, pin 23	AUD
		TCLKC	Connected to the through-hole (MH10)		
		SSIDATA2	Connected to the SDTI pin of AK4353 (U12)		
162	PF4/ICIOWR#/AH#/SSIWS2/ DV_DATA4/TxD3/AUDATA2	AUDATA2	Connected to the H-UDI connector (J3)	CN7, pin 24	AUD
		SSIWS2	Connected to the LRCKI pin of AK4353 (U12)		
163	PF3/ICIORD#/SSISCK2/ DV_DATA3/RxD3/AUDATA1	AUDATA1	Connected to the H-UDI connector (J3)	CN7, pin 22	AUD
		SSISCK2	Connected to the BICK pin of AK4353 (U12)		
164	PF2/BACK#/SSIDATA1/DV_DAT A2/TxD2/DACK0/AUDATA0	AUDATA0	Connected to the H-UDI connector (J3)	CN7, pin 19	AUD
		SSIDATA1	Connected to the SDTI pin of AK4353 (U11)		
165	PVcc				
166	PF1/BREQ#/SSIWS1/DV_DATA1 /RxD2/DREQ0/AUDSYNC#	AUDSYNC #	Connected to the H-UDI connector (J3)	CN7, pin 20	AUD
		SSIWS1	Connected to the LRCKI pin of AK4353 (U11)		
167	Vss				
168	PF0/WAIT#/SSISCK1/DV_DATA0 /SCK2/TEND0/AUDCK	AUDCK	Connected to the H-UDI connector (J3)	CN7, pin 17	AUD
		SSISCK1	Connected to the BICKI pin of AK4353 (U11)		
169	Vcc				
170	PK7/PWM1H/SD_CD	PK7	Connected to DB7 pin of the character LCD	CN7, pin 15	JP2: 1-2
		SD_CD	Connected to the CD pin of the SD card slot		JP2: 2-3
171	PK6/PWM1G/SD_WP	PK6	Connected to DB6 pin of the character LCD	CN7, pin 16	JP2: 1-2
		SD_WP	Connected to the WP pin of the SD card slot		JP2: 2-3
172	PK5/PWM1F/SD_D1	PK5	Connected to DB5 pin of the character LCD	CN7, pin 13	JP2: 1-2
		SD_D1	Connected to DAT1 pin of the SD card slot		JP2: 2-3
173	PK4/PWM1E/SD_D0	PK4	Connected to DB4 pin of the character LCD	CN7, pin 14	JP2: 1-2
		SD_D0	Connected to DAT0 pin of the SD card slot		JP2: 2-3
174	PE5/SDA2/DV_HSYNC	SDA2	Connected to the external IIC connector (J11)	CN7, pin 12	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 3.2.6 SH7264 Pin Functions (6/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
175	PE4/SCL2/DV_VSYNC	SCL2	Connected to the external IIC connector (J11)	CN7, pin 9	
176	PE3/SDA1/IRQ3	SDA1	Connected to the EEPROM SDA pin	CN7, pin 10	JP9: 1-2
		SDA1	Connected to the SDA/CDTI pins of AK4353 (U11, and U12)		
177	PE2/SCL1/IRQ2	SCL1	Connected to the EEPROM SCL pin	CN7, pin 7	JP8:1 -2
		SCL1	Connected to the SCL/CCLKI pins of AK4353 (U11, and U12)		
178	PE1/SDA0/IOIS16#/IRQ1/ TCLKA/ADTRG#	IRQ1	Connected to the BLKCK pin of the CD deck	CN7, pin 8	
		TCLKA	Connected to the through-hole (MH8)		
179	PE0/SCL0/AUDIO_CLK/IRQ0	AUDIO_CLK	Connected to the external clock input socket (U8)	CN7, pin 5	
180	PK3/PWM1D/SD_CLK	PK3	Connected to DB3 pin of the character LCD	CN7, pin 3	JP2: 1-2
		SD_CLK	Connected to the CLK pin of the SD card slot		JP2: 2-3
181	PVcc				
182	Vss				
183	PK2/PWM1C/SD_CMD	PK2	Connected to DB2 pin of the character LCD	CN7, pin 4	JP2: 1-2
		SD_CMD	Connected to the CMD pin of the SD card slot		JP2: 2-3
184	PK1/PWM1B/SD_D3	PK1	Connected to DB1 pin of the character LCD	CN7, pin 1	JP2: 1-2
		SD_D3	Connected to DAT3 pin of the SD card slot		JP2: 2-3
185	PK0/PWM1A/SD_D2	PK0	Connected to DB0 pin of the character LCD	CN7, pin 2	JP2: 1-2
		SD_D2	Connected to DAT2 pin of the SD card slot		JP2: 2-3
186	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 1	
187	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 3	
188	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 6	
189	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 8	
190	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 11	
191	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 13	
192	Vss				
193	PVcc				
194	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 16	
195	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 18	
196	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and the NAND flash memory WE# pin	CN8, pin 2	Auto-switch
197	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and the NAND flash memory ALE pin	CN8, pin 4	Auto-switch
198	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and the NAND flash memory CLE pin	CN8, pin 7	Auto-switch
199	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and the NAND flash memory RE# pin	CN8, pin 9	Auto-switch
200	PD3/D3/PWM1D	D3	Data bus	CN8, pin 12	
201	Vcc				
202	PD2/D2/PWM1C	D2	Data bus	CN8, pin 14	
203	Vss				
204	PD1/D1/PWM1B	D1	Data bus	CN8, pin 17	
205	PVcc				
206	PD0/D0/PWM1A	D0	Data bus	CN8, pin 19	
207	PC0/CS0#	CS0#	Connected to the NOR flash memory CE# pin	CN6, pin 5	
208	PC1/RD#	RD#	Connected to the NOR flash memory OE# pin	CN6, pin 6	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

3.2.3 M3A-HS64G01 Module Availability

The following table shows which combination of modules can/cannot be used.

Table 3.2.7 M3A-HS64G01 Module Availability

				M3A-HS64												M3A-HS64+M3A-HS64G01												
	SH7264 Peripheral Function	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memo	EEPROM	Serial flash memor	USB	H-UDI (14-pin)	H-UDI (36-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	Character LCD	SD card	Audio codec	D/A converter 1	D/A converter 2	CD deck	UART	IIC	LCD	IEBus™	CAN 0	CAN 1	Key input switch
M3A-HS64	BSC	U6	NOR flash memory	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	BSC	U10	SDRAM	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	FLCTL	U7	NAND flash memor	Y	Y	\	Y	*2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*2	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	RSPI	U9	Serial flash memory	Y	Y	*2	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*2	Y	Y	Y	Y	Y	Y
	USB	J1, and J2	USB	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	H-UDI, AUD	J3	H-UDI (36-pin)	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	**N**	**N**	Y	Y	Y	Y	Y	Y	Y
	I/O ports	LED2, and LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	*1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*6	Y
	I/O port	SW5, and SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	*1	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	*4	*4	Y	Y
M3A-HS64+M3A-HS64G01	I/O ports	J1	Character LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	*3	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	SDHI	J2	SD card	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*3	\	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	SSIF, RSPI	U6	Audio codec	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y	Y
	SSIF, IIC3	U11	D/A converter 1	Y	Y	Y	Y	Y	Y	**N**	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y	Y
	SSIF, IIC3	U12	D/A converter 2	Y	Y	Y	Y	Y	Y	**N**	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y	Y
	ROMDEC	J9	CD deck	Y	Y	*2	Y	*2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y	Y
	SCIF	J10	UART	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y	Y
	IIC3	J11	IIC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	Y	Y
	VDC3	J12 to J14	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	Y	Y	*7	Y
	IEB	J15	IEBus™	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*4	Y	Y	Y	Y	Y	Y	Y	Y	Y	\	*5	Y	Y
	RCAN	J16	CAN 0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*4	Y	Y	Y	Y	Y	Y	Y	Y	Y	*5	\	Y	Y
	RCAN	J17	CAN 1	Y	Y	Y	Y	Y	Y	Y	Y	Y	*6	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*7	Y	Y	\	Y
	I/O ports	SW2 to SW17	Key input switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	\

Y: Yes N: No

Notes:
1: When using LED2, and LED3, SW5-1, SW5-2, and SW5-3 on the M3A-HS64 cannot be used.
2: PF9, and 10 are multiplex pins. When setting SW5-5, and SW5-6 on the M3A-HS64, only one module can be used at these intersections.
3: When changing JP2 setting on the M3A-HS64G01, either an SD card or a character LCD can be used.
4: When changing JP4, and JP5 settings on the M3A-HS64, only one module can be used at these intersections.
5: When changing JP5, and JP9 settings on the M3A-HS64G01, either CAN 0 or an IEBus can be used.
6: When changing JP6 setting on the M3A-HS64, either CAN 1 or IRQ1 switch can be used.
7: PJ2 is a multiplex pin. When using the signal LCD_M_DISP, CAN1 cannot be used. When using CAN 1, the signal LCD_M_DISP cannot be used.

3.2.4 SH7264 Multiplex Pins Used on the M3A-HS64G01

Table 3.2.8 to Table 3.2.20 list SH7264 multiplex pin functions used on the M3A-HS64G01.

These multiplex pins are set as port input pins by default. Set the MD bit in the port control register to use the SH7264 peripheral functions (except I/O ports).

Table 3.2.8 SH7264 Multiplex Pin Functions (BSC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
BSC	CS0#	PCCR0	PC0MD0 = B'1	PC0/CS0# (1)
	CS3#	PCCR2	PC8MD[1:0] = B'01	PC8/CS3#/TIOC4D/IRQ7
	RD#	PCCR0	PC1MD0 = B'1	PC1/RD# (1)
	WE0#/DQML	PCCR0	PC3MD0 = B'1	PC3/WE0#/DQML
	WE1#/DQMU/WE#	PCCR1	PC4MD0 = B'1	PC4/WE1#/DQMU/WE#
	RAS#	PCCR1	PC5MD[1:0] = B'01	PC5/RAS#/TIOC4A/IRQ4
	CAS#	PCCR1	PC6MD[1:0] = B'01	PC6/CAS#/TIOC4B/IRQ5
	CKE	PCCR1	PC7MD[1:0] = B'01	PC7/CKE/TIOC4C/IRQ6
	RD/WR#	PCCR0	PC2MD0 = B'1	PC2/RD/WR#
	A21	PBCR5	PB21MD0 = B'1	PB21/A21
	D15	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H (1)
	D14	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G (1)
	D13	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F (1)
	D12	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E (1)
	D11	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D (1)
	D10	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C (1)
	D9	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B (1)
	D8	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A (1)
	D7	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H (1)
	D6	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G (1)
	D5	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F (1)
	D4	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E (1)
	D3	PDCR0	PD3MD[1:0] = B'01	PD3/D3/PWM1D (1)
	D2	PDCR0	PD2MD[1:0] = B'01	PD2/D2/PWM1C (1)
	D1	PDCR0	PD1MD[1:0] = B'01	PD1/D1/PWM1B (1)
	D0	PDCR0	PD0MD[1:0] = B'01	PD0/D0/PWM1A (1)

Note 1: For boot modes 1 to 3

Table 3.2.9 SH7264 Multiplex Pin Functions (INTC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
INTC	IRQ1	PJCR0	PJ3MD[1:0] = B'11	PJ3/CRx1/CRx0&CRx1/IRQ1
	IRQ1	PECR0	PE1MD[2:0] = B'011	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#

Table 3.2.10 SH7264 Multiplex Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SCIF	RTS3#	PJCR2	PJ8MD[1:0] = B'10	PJ8/PWM2E/RTS3#
	CTS3#	PJCR1	PJ7MD[1:0] = B'10	PJ7/TIOC1B/CTS3#
	SCK3	PJCR1	PJ6MD[1:0] = B'10	PJ6/TIOC1A/SCK3
	TxD3	PJCR1	PJ5MD[1:0] = B'10	PJ5/IERxD/TxD3
	RxD3	PJCR1	PJ4MD[1:0] = B'10	PJ4/IETxD/RxD3
	RxD0	PJCR0	PJ1MD[2:0] = B'100	PJ1/CRx0/IERxD/IRQ0/RxD0
	TxD0	PJCR0	PJ0MD[2:0] = B'100	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 3.2.11 SH7264 Multiplex Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
IIC3	SDA2	PECR1	PE5MD[1:0] = B'01	PE5/SDA2/DV_HSYNC
	SCL2	PECR1	PE4MD[1:0] = B'01	PE4/SCL2/DV_VSYNC
	SDA1	PECR0	PE3MD[1:0] = B'01	PE3/SDA1/IRQ3
	SCL1	PECR0	PE2MD[1:0] = B'01	PE2/SCL1/IRQ2

Table 3.2.12 SH7264 Multiplex Pin Functions (RCAN-TL1)

Peripheral Function	Pin Nname	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
RCAN-TL1	CRx1	PJCR0	PJ3MD[1:0] = B'01	PJ3/CRx1/CRx0&CRx1/IRQ1
	CTx1	PJCR0	PJ2MD[2:0] = B'001	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP
	CRx0	PJCR0	PJ1MD[2:0] = B'001	PJ1/CRx0/IERxD/IRQ0/RxD0
	CTx0	PJCR0	PJ0MD[2:0] = B'001	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 3.2.13 SH7264 Multiplex Pin Functions (IEB)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
IEB	IERxD	PJCR0	PJ1MD[2:0] = B'010	PJ1/CRx0/IERxD/IRQ0/RxD0
	IETxD	PJCR0	PJ0MD[2:0] = B'010	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 3.2.14 SH7264 Multiplex Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E
	FCE#	PFCR2	PF10MD[2:0] = B'101	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	FRB	PFCR2	PF9MD[2:0] = B'101	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 3.2.15 SH7264 Multiplex Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SDHI	SD_CD	PKCR1	PK7MD[1:0] = B'10	PK7/PWM1H/SD_CD
	SD_WP	PKCR1	PK6MD[1:0] = B'10	PK6/PWM1G/SD_WP
	SD_D1	PKCR1	PK5MD[1:0] = B'10	PK5/PWM1F/SD_D1
	SD_D0	PKCR1	PK4MD[1:0] = B'10	PK4/PWM1E/SD_D0
	SD_CLK	PKCR0	PK3MD[1:0] = B'10	PK3/PWM1D/SD_CLK
	SD_CMD	PKCR0	PK2MD[1:0] = B'10	PK2/PWM1C/SD_CMD
	SD_D3	PKCR0	PK1MD[1:0] = B'10	PK1/PWM1B/SD_D3
	SD_D2	PKCR0	PK0MD[1:0] = B'10	PK0/PWM1A/SD_D2

Table 3.2.16 SH7264 Multiplex Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
RSPI	MOSI1	PGCR5	PG23MD[1:0] = B'01	PG23/MOSI1/TIOC0C
	SSL10	PGCR5	PG22MD[1:0] = B'01	PG22/SSL10/TIOC0B
	RSPCK1	PGCR5	PG21MD[1:0] = B'01	PG21/RSPCK1/TIOC0A
	MISO0	PFCR3	PF12MD[2:0] = B'011	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
	MOSI0	PFCR2	PF11MD[2:0] = B'011	PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN
	SSL00	PFCR2	PF10MD[2:0] = B'011	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	RSPCK0	PFCR2	PF9MD[2:0] = B'011	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 3.2.17 SH7264 Multiplex Pin Functions (SSIF)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SSIF	SSIDATA3	PFCR2	PF8MD[1:0] = B'10	PF8/CE2B#/SSIDATA3/DV_CLK
	SSIWS3	PFCR1	PF7MD[2:0] = B'010	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
	SSISCK3	PFCR1	PF6MD[2:0] = B'010	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/TCLKB
	SSIDATA2	PFCR1	PF5MD[2:0] = B'010	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5/TCLKC/AUDATA3
	SSIWS2	PFCR1	PF4MD[2:0] = B'010	PF4/ICIOWR#/AH#/SSIWS2/DV_DATA4/TxD3/AUDATA2
	SSISCK2	PFCR0	PF3MD[2:0] = B'010	PF3/ICIORD#/SSISCK2/DV_DATA3/RxD3/AUDATA1
	SSIDATA1	PFCR0	PF2MD[2:0] = B'010	PF2/BACK#/SSIDATA1/DV_DATA2/TxD2/DACK0/AUDATA0
	SSIWS1	PFCR0	PF1MD[2:0] = B'010	PF1/BREQ#/SSIWS1/DV_DATA1/RxD2/DREQ0/AUDSYNC#
	SSISCK1	PFCR0	PF0MD[2:0] = B'010	PF0/WAIT#/SSISCK1/DV_DATA0/SCK2/TEND0/AUDCK
	SSITxD0	PKCR2	PK11MD[1:0] = B'10	PK11/PWM2D/SSITxD0
	SSIRxD0	PKCR2	PK10MD[1:0] = B'10	PK10/PWM2C/SSIRxD0
	SSIWS0	PKCR2	PK9MD[1:0] = B'10	PK9/PWM2B/SSIWS0
	SSISCK0	PKCR2	PK8MD[1:0] = B'10	PK8/PWM2A/SSISCK0
	AUDIO_CLK	PECR0	PE0MD[1:0] = B'10	PE0/SCL0/AUDIO_CLK/IRQ0

Table 3.2.18 SH7264 Multiplex Pin Functions (ADC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
ADC	AN7	PHCR1	PH7MD0 = B'1	PH7/AN7
	AN3	PHCR0	PH3MD0 = B'1	PH3/AN3
	AN2	PHCR0	PH2MD0 = B'1	PH2/AN2
	AN1	PHCR0	PH1MD0 = B'1	PH1/AN1
	AN0	PHCR0	PH0MD0 = B'1	PH0/AN0

Table 3.2.19 SH7264 Multiplex Pin Functions (VDC3)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
VDC3	LCD_EXTCLK	PGCR5	PG20MD[2:0] = B'001	PG20/LCD_EXTCLK/MISO1/TxD7
	LCD_CLK	PGCR4	PG19MD[2:0] = B'001	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7
	LCD_DE	PGCR4	PG18MD[2:0] = B'001	PG18/LCD_DE/TIOC2A/SSL10/TxD6
	LCD_HSYNC	PGCR4	PG17MD[2:0] = B'001	PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6
	LCD_VSYNC	PGCR4	PG16MD[2:0] = B'001	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#
	LCD_DATA15	PGCR3	PG15MD[2:0] = B'001	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
	LCD_DATA14	PGCR3	PG14MD[2:0] = B'001	PG14/LCD_DATA14/TIOC0C/SCK1
	LCD_DATA13	PGCR3	PG13MD[2:0] = B'001	PG13/LCD_DATA13/TIOC0B/TxD1
	LCD_DATA12	PGCR3	PG12MD[2:0] = B'001	PG12/LCD_DATA12/TIOC0A/RxD1
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'001	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/SIOFTxD
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'001	PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/SIOFRxD
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'001	PG9/LCD_DATA9/SSIWS0/TxD4/SIOFSYNC
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'001	PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK
	LCD_DATA7	PGCR1	PG7MD[1:0] = B'01	PG7/LCD_DATA7/SD_CD/PINT7
	LCD_DATA6	PGCR1	PG6MD[1:0] = B'01	PG6/LCD_DATA6/SD_WP/PINT6
	LCD_DATA5	PGCR1	PG5MD[1:0] = B'01	PG5/LCD_DATA5/SD_D1/PINT5
	LCD_DATA4	PGCR1	PG4MD[1:0] = B'01	PG4/LCD_DATA4/SD_D0/PINT4
	LCD_DATA3	PGCR0	PG3MD[1:0] = B'01	PG3/LCD_DATA3/SD_CLK/PINT3
	LCD_DATA2	PGCR0	PG2MD[1:0] = B'01	PG2/LCD_DATA2/SD_CMD/PINT2
	LCD_DATA1	PGCR0	PG1MD[1:0] = B'01	PG1/LCD_DATA1/SD_D3/PINT1
	LCD_DATA0	PGCR7	PG0MD[2:0] = B'001	PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#
	LCD_M_DISP	PJCR0	PJ2MD[2:0] = B'101	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP

Table 3.2.20 SH7264 Multiplex Pin Functions (PORT)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
PORT	PG24	PGCR6	PG24MD[1:0] = B'00	PG24/MISO1/TIOC0D
	PJ10	PJCR2	PJ10MD[1:0] = B'00	PJ10/PWM2G/DREQ1
	PJ9	PJCR2	PJ9MD[1:0] = B'00	PJ9/PWM2F/TEND1
	PK7	PKCR1	PK7MD[1:0] = B'00	PK7/PWM1H/SD_CD
	PK6	PKCR1	PK6MD[1:0] = B'00	PK6/PWM1G/SD_WP
	PK5	PKCR1	PK5MD[1:0] = B'00	PK5/PWM1F/SD_D1
	PK4	PKCR1	PK4MD[1:0] = B'00	PK4/PWM1E/SD_D0
	PK3	PKCR0	PK3MD[1:0] = B'00	PK3/PWM1D/SD_CLK
	PK2	PKCR0	PK2MD[1:0] = B'00	PK2/PWM1C/SD_CMD
	PK1	PKCR0	PK1MD[1:0] = B'00	PK1/PWM1B/SD_D3
	PK0	PKCR0	PK0MD[1:0] = B'00	PK0/PWM1A/SD_D2
	PC10	PCCR2	PC10MD0 = B'0	PC10/TIOC2B
	PC9	PCCR2	PC9MD0 = B'0	PC9/TIOC2A
	PB22	PBCR5	PB22MD[1:0] = B'00	PB22/A22/CS4#

3.3 LCD Module Interface

3.3.1 LCD Module Interface

The M3A-HS64G01 includes two flexible connectors and one MIL-spec connector for connecting LCD modules. The SH7264 on-chip VDC3 controls the LCD modules.

The following figure shows the LCD module interface block diagram.

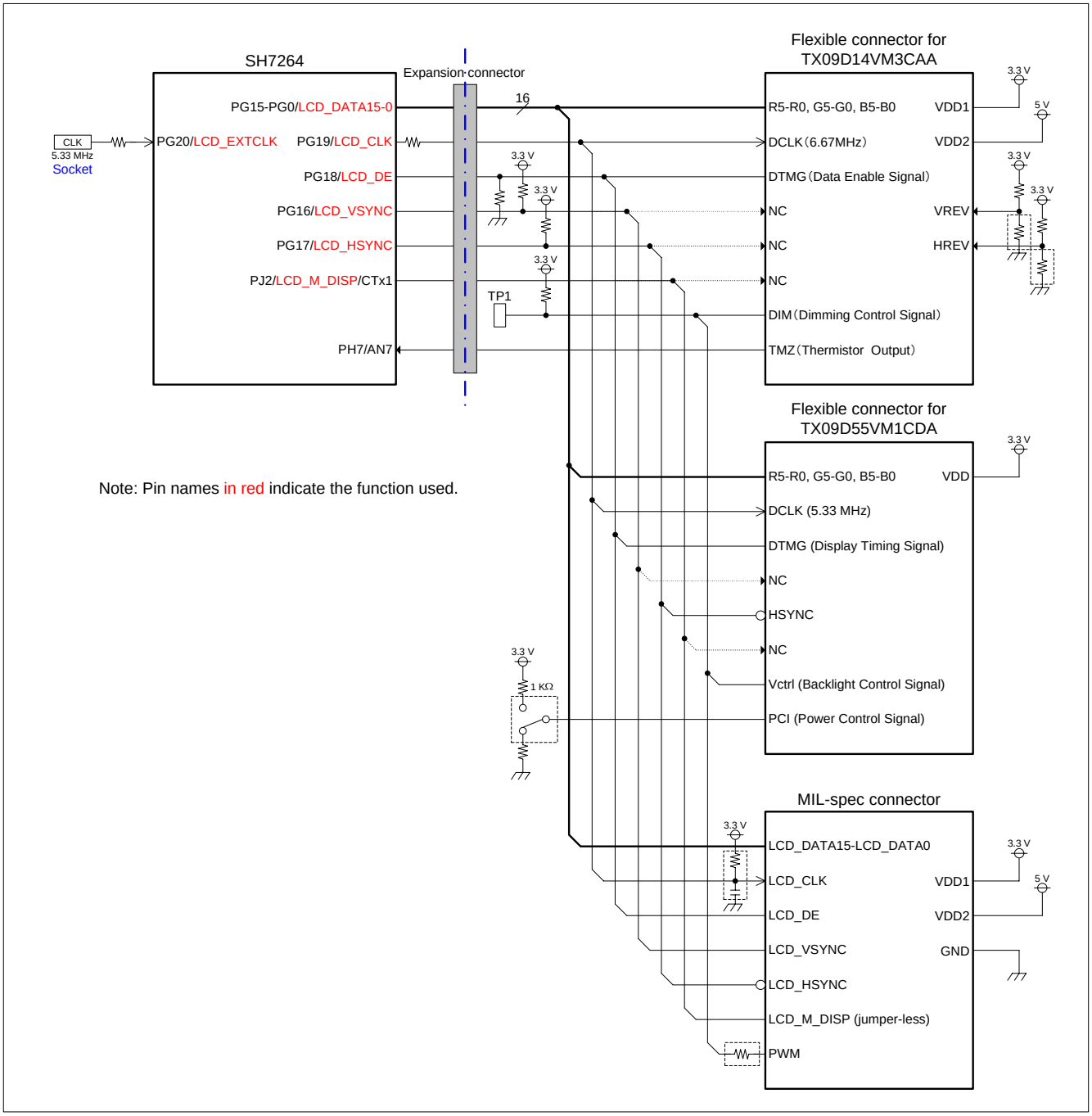

Figure 3.3.1 LCD Module Interface Block Diagram

3.3.2 Character LCD Module with LED Backlight

The M3A-HS64G01 includes a connector for 16 x 2 semi-transmissive character LCD module (SD1602H, SUNLIKE). The SH7264 general-purpose port output controls the character LCD module. The M3A-HS64G01 is intended only for writing from the SH7264 to the character LCD modules. Therefore, the character LCD module R/W signal is fixed low.

The M3A-HS64G01 also includes a variable resistor (VR1) for the LCD driver voltage adjustment to control the LCD contrast and a variable resistor (VR2) for LCD backlight adjustment.

SH7264 PK7 to PK0 pins are also used as SDHI pins. When using the character LCD module, SDHI cannot be used. The figure below shows the character LCD module block diagram. The table below lists the jumper setting (JP2).

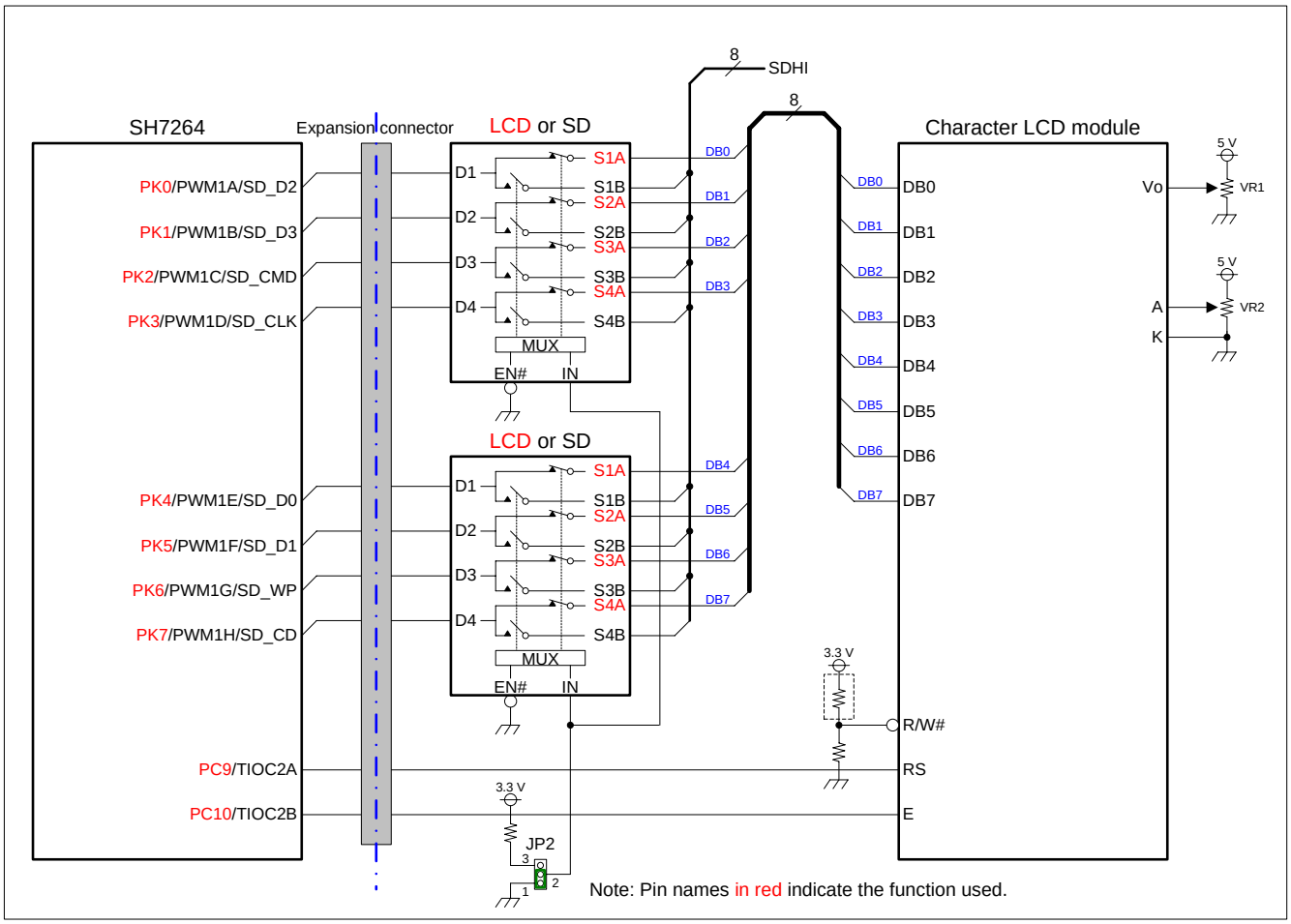

Figure 3.3.2 Character LCD Module Block Diagram

Table 3.3.1 Jumper Setting (JP2)

Number	1-2 (Low)	2-3 (High)
JP2	Connected to the character LCD interface (default)	Connected to the SDHI

3.4 Audio Modules

The M3A-HS64G01 includes two 96 kHz, 24-bit D/A converters with DIT (AK4353, Asahi Kasei EMD Corporation), and one 24-bit stereo codec with IPGA (AK4524).

➢ AK4353, D/A Converter

SH7264 IIC3, SSIF, and I/O ports control AK4353.

- SH7264 IIC3 (Channel 1): Accesses the AK4353 registers to initialize AK4353, format data, and configure the attenuator
- SH7264 SSIF (Channels 2, and 1): Outputs the audio data
- SH7264 I/O port (PG24): Powers down AK4353 at low
  Powers up AK4353 at high

Note: M3A-HS64 allows for selecting 12.2880 MHz or 11.2896 MHz as the AK4353 system clock.

Figure 3.4.1 shows the D/A converter block diagram, and Table 3.4.1 lists the jumper setting (JP7).

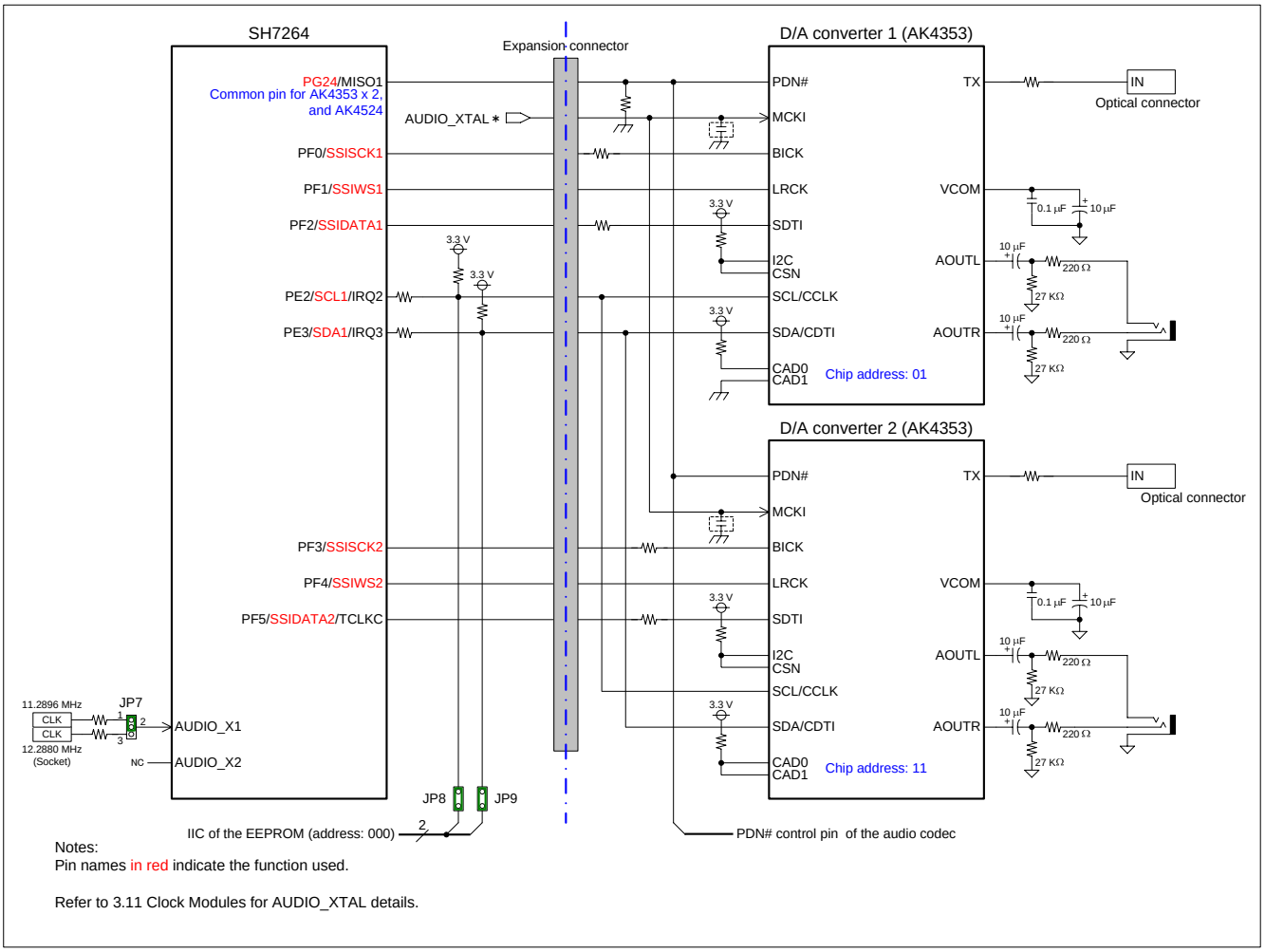

Figure 3.4.1 D/A Converter Block Diagram

Table 3.4.1 Jumper Setting (JP7)

Number	1-2	2-3
JP7	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

➢ AK4524 audio codec

RSPI, SSIF, and I/O ports on the SH7264 control the audio codec.

- SH7264 RSPI (Channel 1): Accesses the AK4524 registers to initialize AK4524, and format data
- SH7264 SSIF (Channel 0): Inputs/Outputs the audio data
- SH7264 I/O port (PG24): Powers down AK4524 at low
  Powers up AK4524 at high

Note: M3A-HS64 allows selecting either 12.2880 MHz or 11.2896 MHz as the AK4524 system clock.

The figure below shows the audio codec block diagram. Refer to Table 3.4.1 for the jumper setting (JP7).
The plug-in power microphone can be connected when JP3 is shorted.

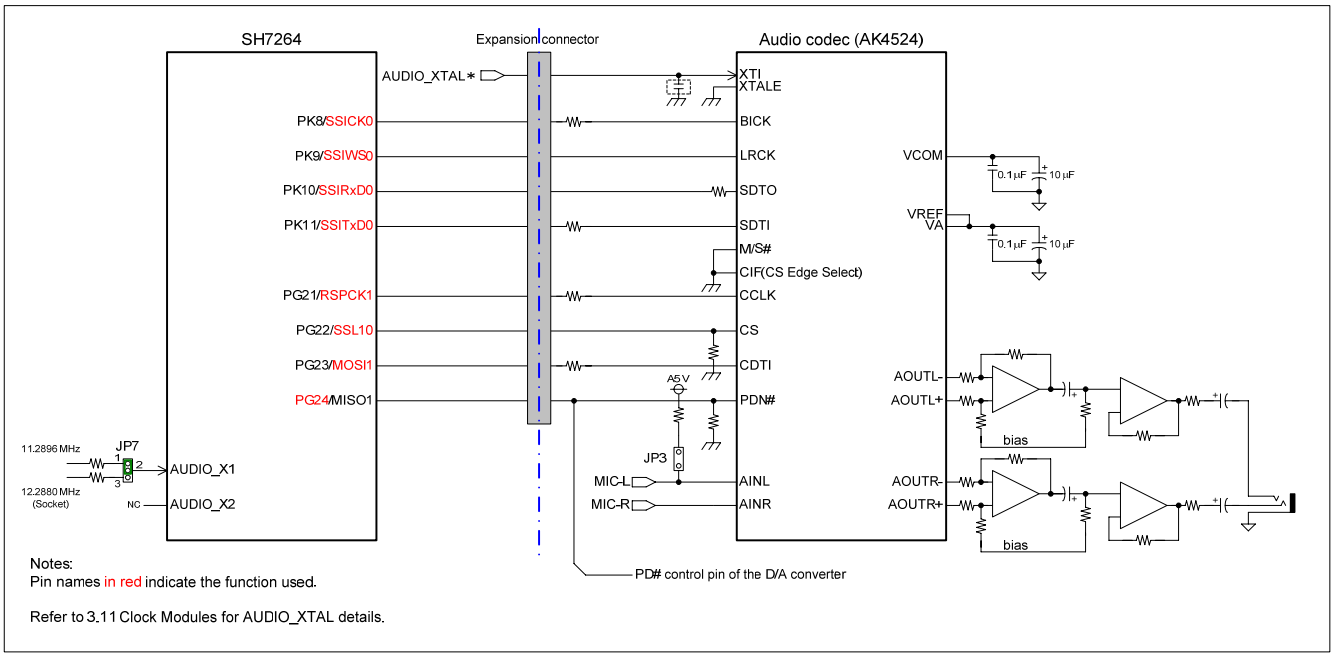

Figure 3.4.2 Audio Codec Block Diagram

Table 3.4.2 Jumper Setting (JP3)

Number	1-2	None (Open)
JP3	Plug-in power microphone available	Typical microphone available (default)

3.5 CD Deck Interface

The M3A-HS64G01 includes a CD deck interface connector. The SH7264 on-chip SSIF (Serial Sound Interface with FIFO) and RSPI (Renesas Peripheral Interface) control the CD deck.

The RSPI channel 0 pin is also used as the NAND flash memory controller (FLCTL) pin. When connecting it with the CD deck interface, set SW5-5 and SW5-6 to ON.

The following figure shows the CD deck interface block diagram. Table 3.5.1 lists the DIP switches setting (SW5-5, and SW5-6).

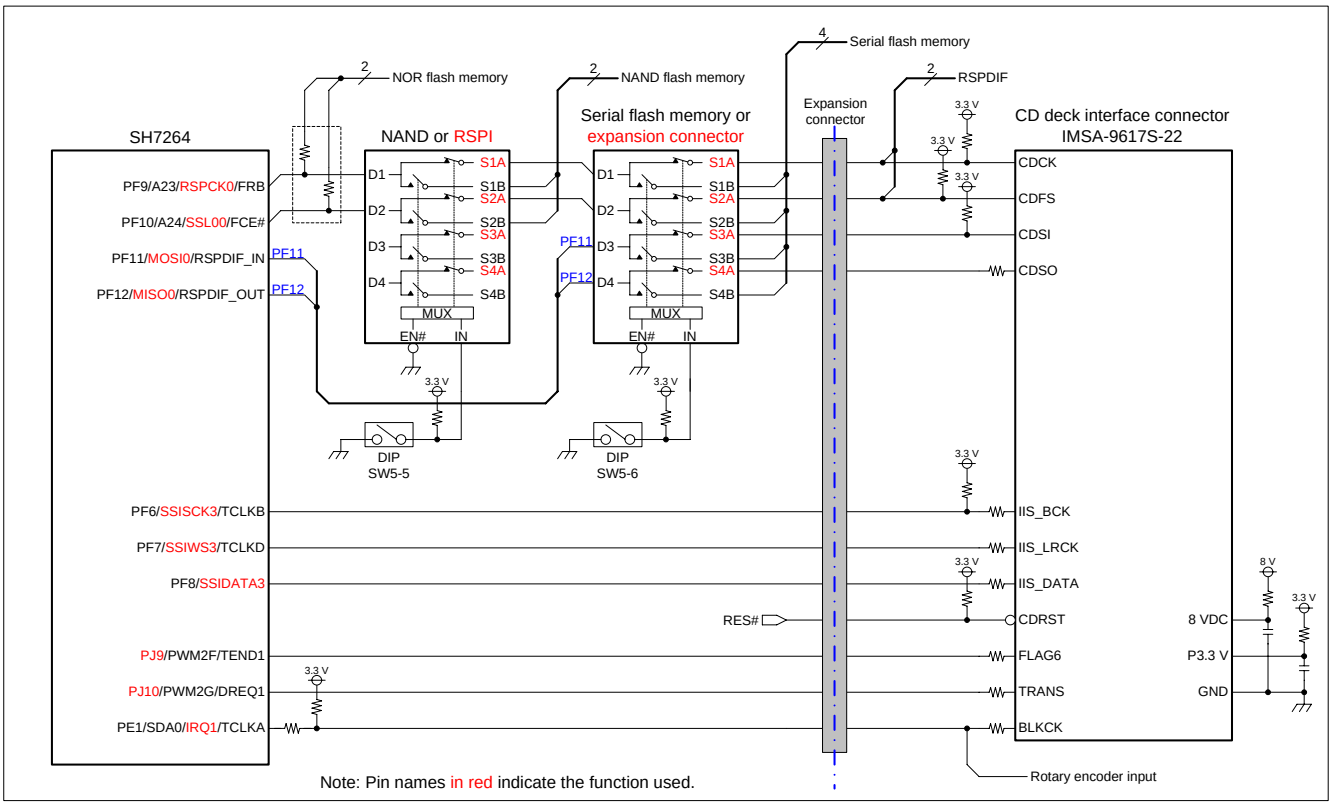

Figure 3.5.1 CD Deck Interface Block Diagram

Table 3.5.1 DIP Switches Setting (SW5)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI (default)
SW5-6	Connected to the serial flash memory	Connected to the expansion connector (CD deck/RSPDIF/MTU2 - default)

3.6 SD Card Interface

The M3A-HS64G01 includes an SD card slot. The SD card slot is connected to the SD Host Interface (SDHI) and the SD card slot built in the SH7264. The figure below shows the SD card interface block diagram.

The SDHI pin is also used as PK7 to PK0 pins to control the character LCD module. When using the SDHI, do not use the character LCD module (Remove the character LCD module).

Table 3.6.1 lists the jumper setting (JP2).

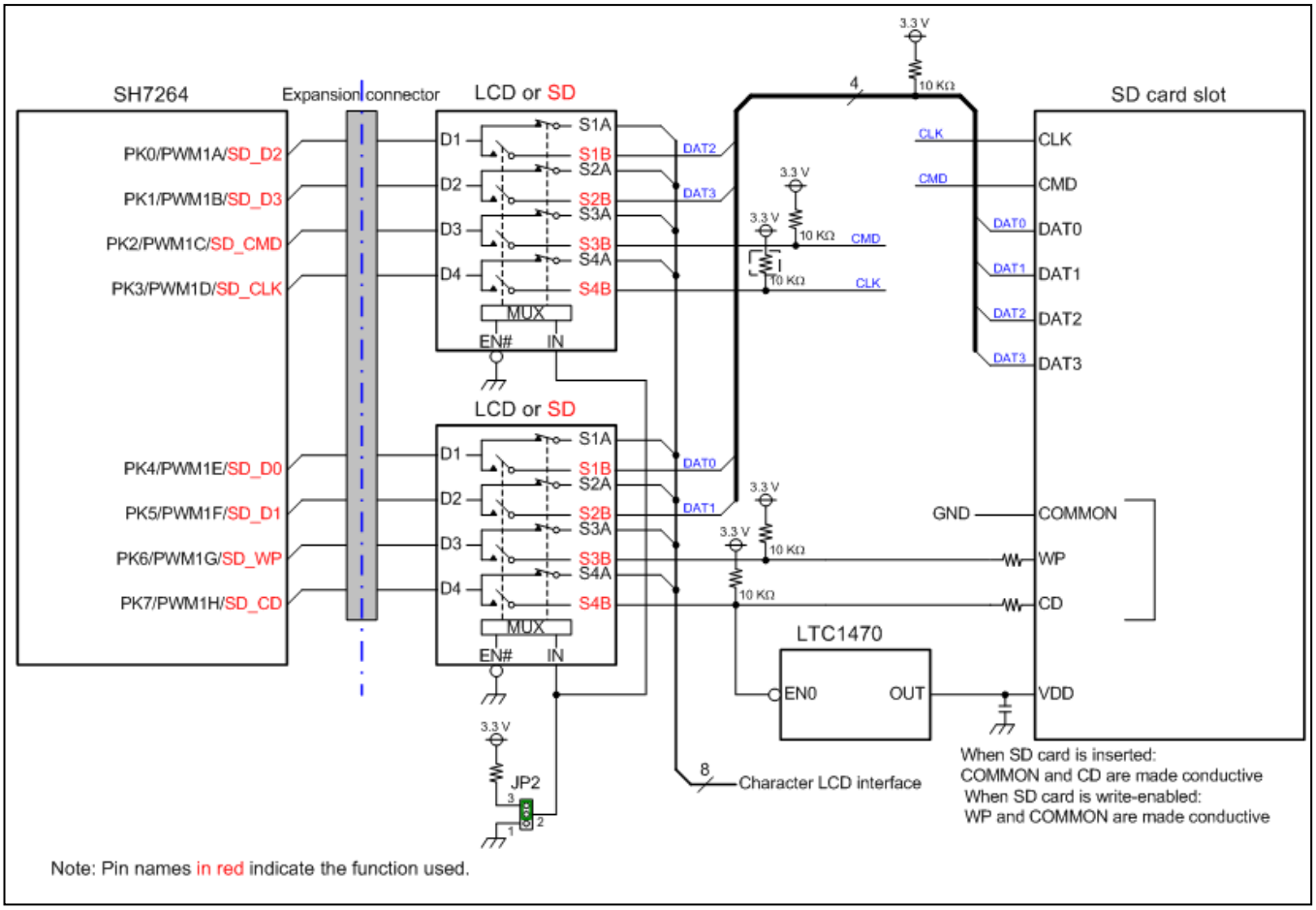

Figure 3.6.1 SD Card Interface Block Diagram

Table 3.6.1 Jumper Setting (JP2)

Number	1-2 (Low)	2-3 (High)
JP2	Connected to the character LCD interface (default)	Connected to the SDHI

3.7 UART Interface

The SH7264 has a Serial Communication Interface with FIFO (SCIF). The SCIF channel 3 pin is connected to the UART connector (7-pin, 2.5 mm pitch) on the M3A-HS64G01, at TTL level.

The figure below shows the UART interface block diagram, and the table below lists the jumpers setting (JP4, and JP5).

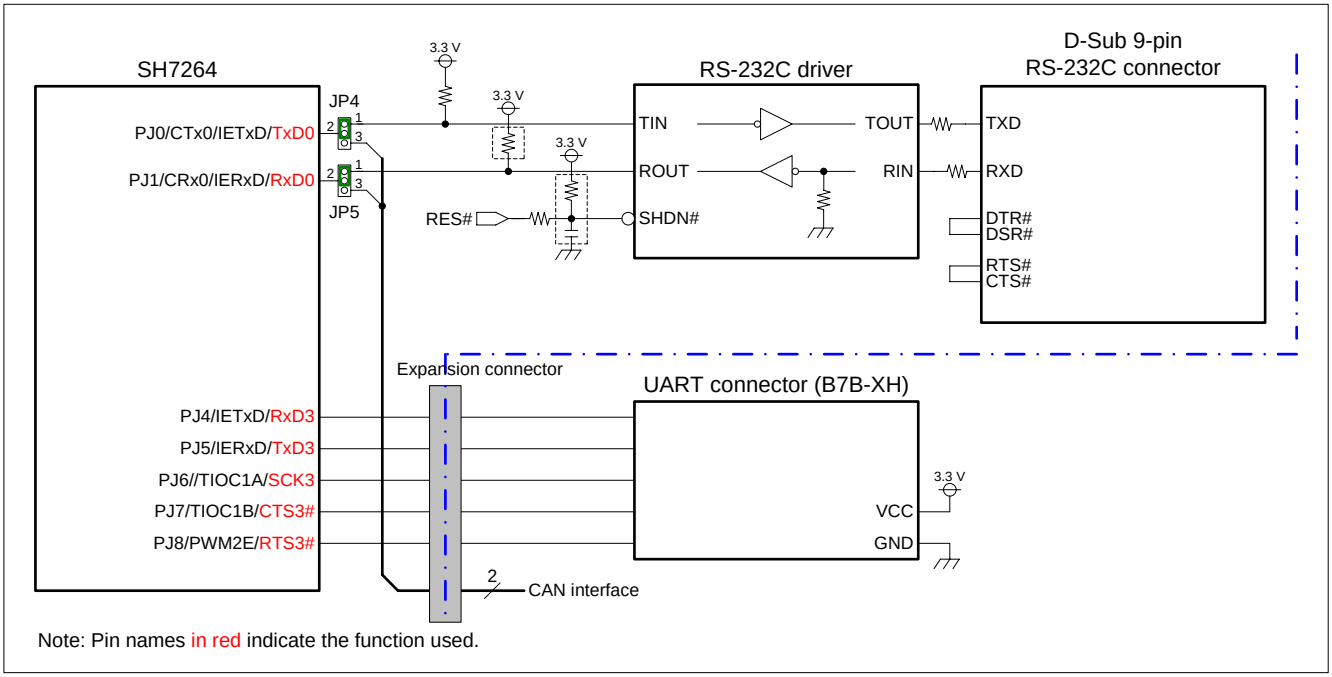

Figure 3.7.1 UART Interface Block Diagram

Table 3.7.1 Jumpers Setting (JP4, and JP5)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins

3.8 CAN Interface

The SH7264 includes RCAN-TL1 (Renesas CAN Time Trigger Level 1), the controller area network. SH7264 RCAN-TL1 channels 0 and 1 are connected to the CAN connector (3-pin, 2.5 mm pitch) on the M3A-HS64G01 via the voltage level shifter and the CAN driver IC.

The RCAN-TL1 channel 0 pin is also used as the SCIF channel 0 pin, and the IEBus™ controller (IEB) pin.

The figure below shows the CAN interface block diagram. Table 3.8.1 lists the jumpers setting (JP4 to JP6 on the M3A-HS64). Table 3.8.2 and Table 3.8.3 list the jumpers setting (JP4, JP5, JP8, and JP9).

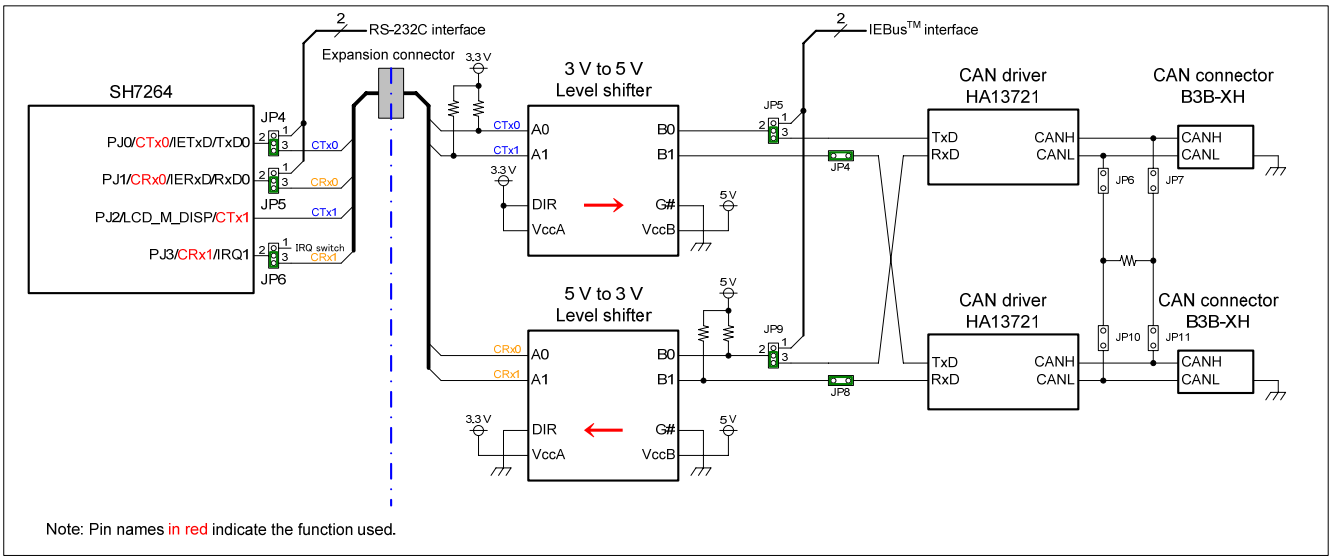

Figure 3.8.1 CAN Interface Block Diagram

Table 3.8.1 Jumpers Setting (JP4 to JP6 on the M3A-HS64)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins
JP6	Selects the IRQ1 switch	Selects the CRx1 (RCAN-TL1) pin

Table 3.8.2 Jumpers Setting (JP5, and JP9)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

Table 3.8.3 Jumper Setting (JP4, and JP8)

Number	1-2	None (Open)
JP4	Normal mode (Connects the CTx1 pin) - default	Debug mode (Leaves the CTx1 pin disconnected)
JP8	Normal mode (Connects the CRx1 pin) - default	Debug mode (Leaves the CRx1 pin disconnected)

3.9 IEBus™ Interface

The SH7264 includes an IEBus™ controller (IEB). The IEBus™ (Inter Equipment Bus™) is the bus for digital data transfer system on a small scale. The SH7264 IEB pin is connected to the IEBus connector (4-pin, 2.5 mm pitch) via the voltage level shifter and the IEBus™ driver IC on the M3A-HS64G01.

The IEB pin is also used as the SCIF channel 0 pin and the RCAN-TL1 channel 0 pin.

The figure below shows the IEBus™ interface block diagram. Table 3.9.1 lists the jumpers setting (JP4, and JP5 on the M3A-HS64). Table 3.9.2 lists the jumpers setting (JP5, and JP9).

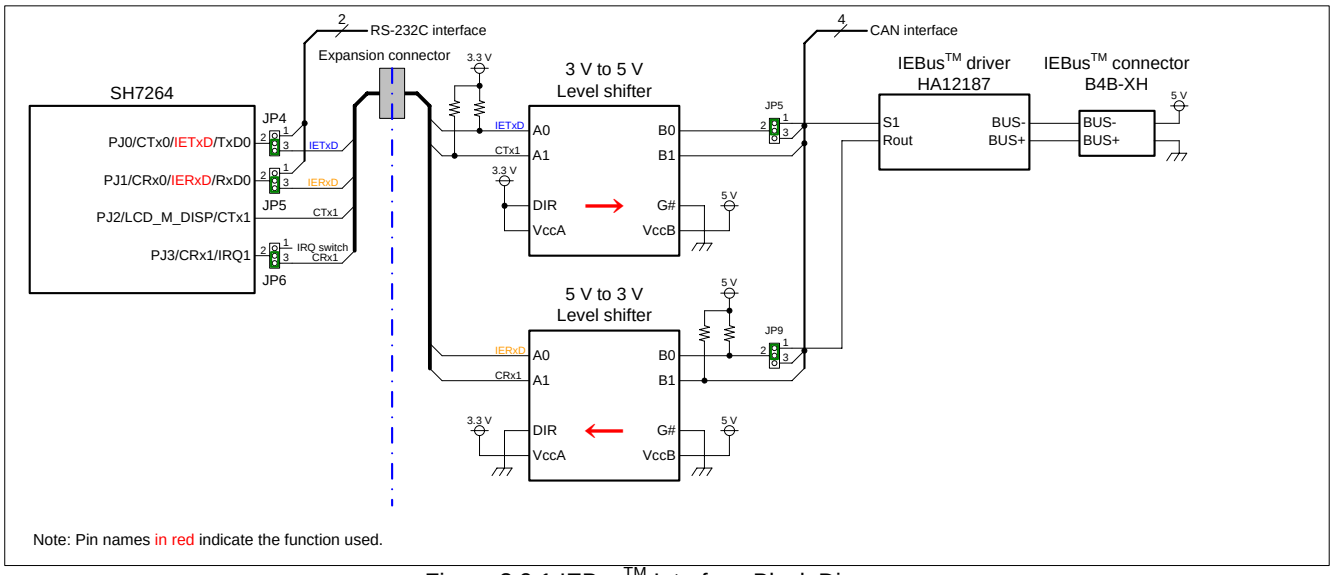

Figure 3.9.1 IEBus™ Interface Block Diagram

Table 3.9.1 Jumpers Setting (JP4, and JP5 on the M3A-HS64)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins

Table 3.9.2 Jumpers Setting (JP5, and JP9)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

3.10 I/O Ports

SH7264 I/O ports are connected to switches and LEDs on the M3A-HS64G01.

To use ports PH3 to PH0 as key input switches (4 switches x 4 inputs) via an A/D converter (ADC), set the ports as analog input pins (AN3 to AN0).

Port A can be used as a user interface by setting PB22 pin to high output.

The figure below shows the I/O ports block diagram. Table 3.10.1 lists the jumper setting (JP14 on the M3A-HS64). Table 3.10.2 lists the port A function switching.

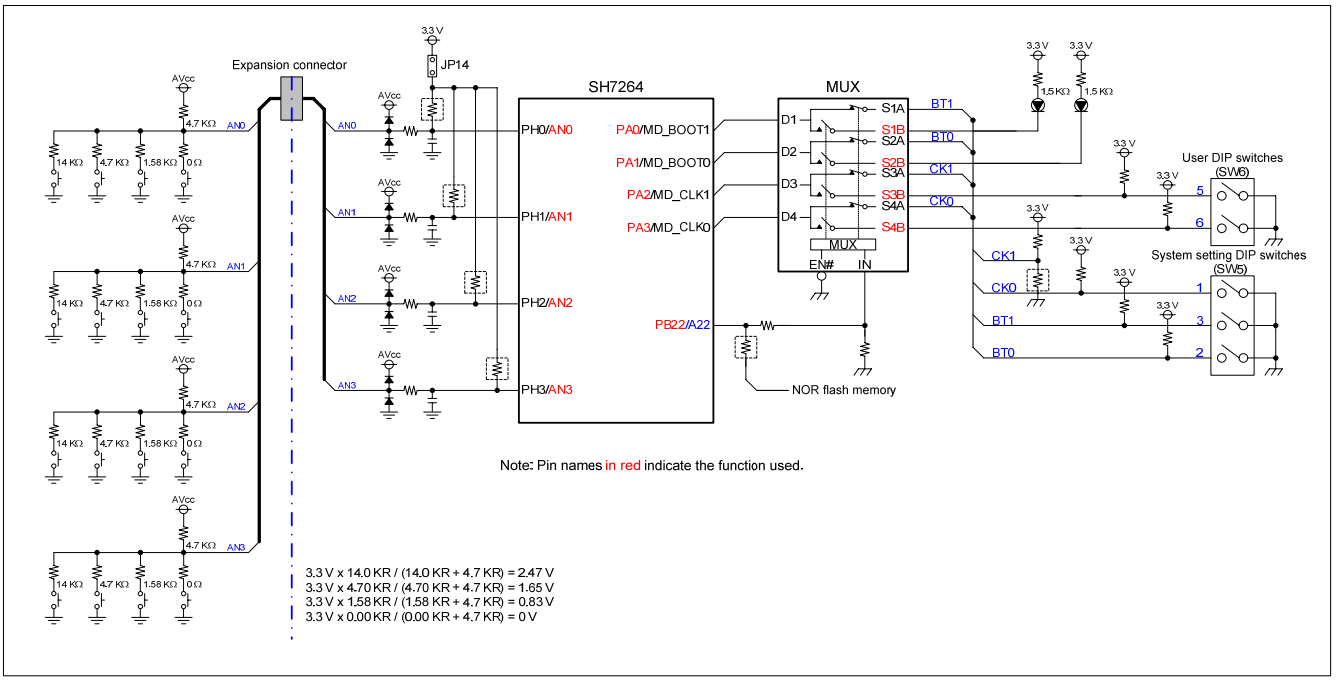

Figure 3.10.1 I/O Ports Block Diagram

Table 3.10.1 Jumper Setting (JP14 on the M3A-HS64)

Number	1-2	None (Open)
JP14	Uses PH[0:3] as an input port (default) (1)	Uses PH[0:3] as an analog input pin

Note 1: Mount R10 to R13 when using PH [0:3] as an input port.

Table 3.10.2 Port A Function Switching

Number	High output	Low output
PB22	Uses Port A as a user interface	Mode sampling (At power-up)

3.11 Clock Modules

Provide following clocks with the SH7264 on the M3A-HS64.

- SH7264 input clock: 18 MHz
- SH7264 RTC clock: 32.768 kHz
- SH7264 audio clock: 12.2880 MHz, and 11.2896 MHz (default)
- SH7264 USB clock: 48.00 MHz
- SH7264 LCD clock: 5.33 MHz

➢ How to select the system clock frequency of AK4353 (D/A converter), and AK4524 (audio codec)

SH7264 audio clock provides either 12.2880 MHz or 11.2896 MHz of the clock frequency with AK4353 and AK4524 by switching jumpers. The figure below shows the clock module block diagram of the M3A-HS64 and M3A-HS64G01.

Table 3.11.1 lists the audio clock switching.

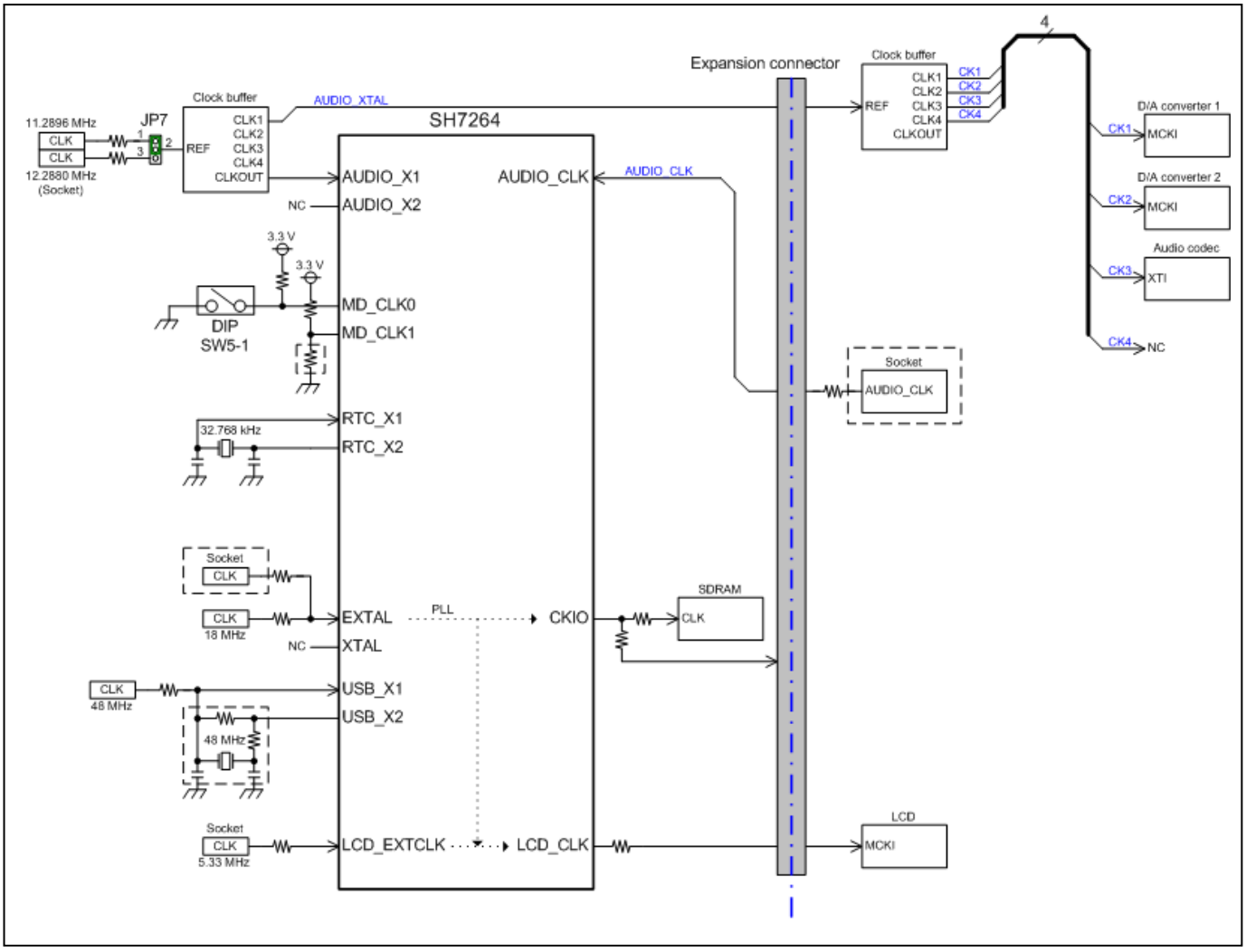

Figure 3.11.1 Clock Module Block Diagram

Table 3.11.1 Audio Clock Switching

Number	1-2	2-3
JP7	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

3.12 Reset Module

A reset IC controls reset signals connected to the SH7264, flash memory and peripheral I/Os on the M3A-HS64 and M3A-HS64G01. There are two system reset options: power-on reset, and reset by switch. The following figure shows the reset module block diagram.

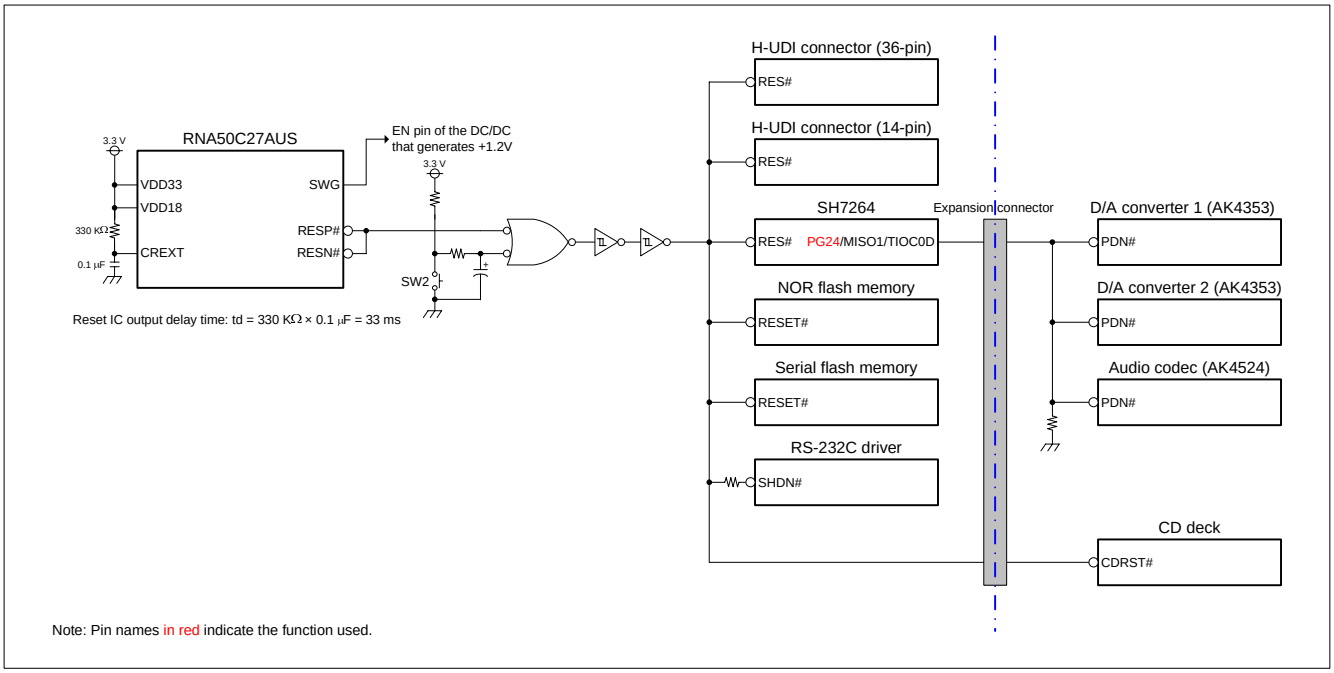

Figure 3.12.1 Reset Module Block Diagram

3.13 Power Supply Module

The M3A-HS64G01 is supplied 12 V power and the voltage regulator on the M3A-HS64G01 generates 8 V, and 5 V voltage.
5 V is supplied to the M3A-HS64, and the voltage regulator on the M3A-HS64 generates digital voltage (3.3 V, 3VCC) and analog voltage (3.3 V, AVcc).
The following figure shows the power supply module block diagram.

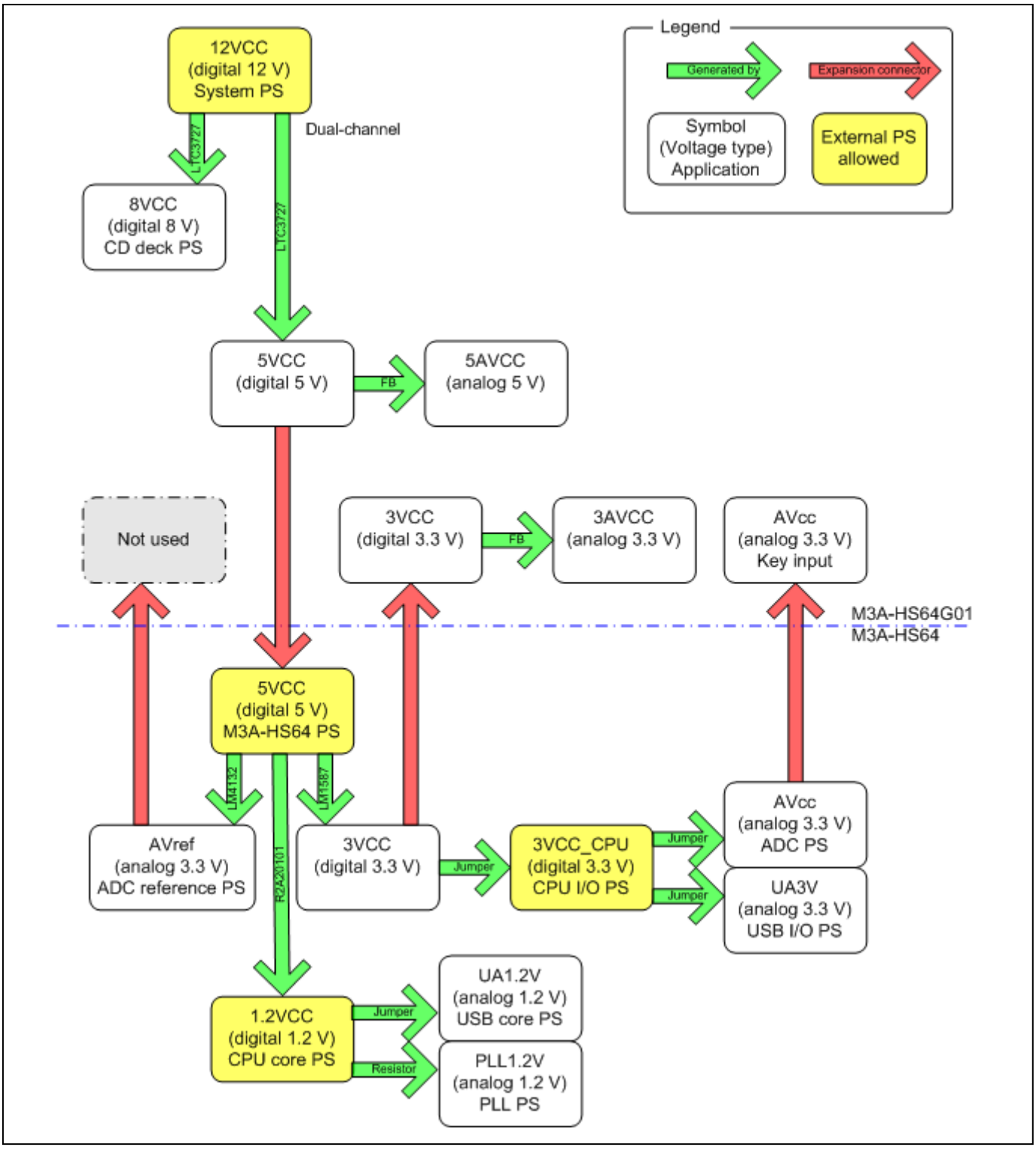

Figure 3.13.1 Power Supply Module Block Diagram

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Chapter 4
M3A-HS64G02 Functions

4.1 Overview of Functions

M3A-HS64G02 includes the functional modules listed in the following table.

Table 4.1.1 M3A-HS64G02 Function Modules

Section	Function	Description
4.2	CPU	• SH7264
4.3	LCD Module Interface	• LCD module interface - Connects the SH7264 Video Display Controller 3 (VDC3) and LCD module connectors - Flexible connectors for LCD module are included • Character LCD module with LED backlight
4.4	Audio Module	• Connects the SH7264, and a D/A converter - 96 kHz 24-bit D/A converter: 1
4.5	Video Signal Input Module	• Connects the SH7264 Video Display Controller (VDC3) and a video decoder IC
4.6	SD Card Interface	• Connects the SH7264 SD Host Interface (SDHI), and an SD card slot
4.7	UART Interface	• Connects the SH7264 Serial Communication Interface with FIFO (SCIF) and a UART connector
4.8	CAN Interface	• Connects the SH7264 Controller Area Network (RCAN-TL1) and a CAN connector
4.9	IEBus™ Interface	• Connects the SH7264 IEBus™ controller (IEB) and IEBus™ connector
4.10	PWM Interface	• Connects the SH7264 Motor Control PWM Timer (PWM) and a 20-pin MIL-spec connector
4.11	MTU2 Interface	• Connects the SH7264 Multi Function Timer Pulse Unit 2 (MTU2) and a 20-pin MIL-spec connector
4.12	I/O Ports	• Connect the SH7264 I/O ports, LEDs, and DIP switches
4.13	Interrupt Switches	• Connects the SH7264 IRQ2 pin, IRQ3 pin, and push-button switches
4.14	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
4.15	Reset Module	• Resets devices on the M3A-HS64G02
4.16	Power Supply Module	• Controls the M3A-HS64G02 system power supply
-	Operating Specifications	• Connectors, switches, and LEDs Refer to Chapter 7 for details.

4.2 CPU

4.2.1 SH7264 Overview

The M3A-HS64 includes the SH7264, the 32-bit RISC MCU that operates with a maximum frequency of 144 MHz.

4.2.2 SH7264 Pin Functions Used on the M3A-HS64G02

Table 4.2.1 to Table 4.2.6 list the SH7264 pin functions used on the M3A-HS64G02.

Table 4.2.1 SH7264 Pin Functions (1/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
1	PC2/RD/WR#	RD/WR#	Connected to the SDRAM #WE pin	CN6, pin 7	
2	PC3/WE0#/DQML	WE0#	Connected to the NOR flash memory #WE pin	CN6, pin 8	
		DQML	Connected to the SDRAM DQML pin		
3	Vss				
4	PC4/WE1#/DQMU/WE#	DQMU	Connected to the SDRAM DQMU pin	CN6, pin 9	
5	PVcc				
6	PC9/TIOC2A	PC9	Connected to the RS pin of the character LCD	CN6, pin 12	
		TIOC2A	Connected to the MTU2 connector (J16)		
7	PC10/TIOC2B	PC10	Connected to the E pin of the character LCD	CN6, pin 13	
		TIOC2B	Connected to the MTU2 connector (J16)		
8	PC5/RAS#/TIOC4A/IRQ4	RAS#	Connected to the SDRAM RAS# pin	-	SW5-4: OFF
		TIOC4A	Connected to the MTU2 connector (J16)	CN6, pin 14	SW5-4: ON
9	PC6/CAS#/TIOC4B/IRQ5	CAS#	Connected to the SDRAM CAS# pin	-	SW5-4: OFF
		TIOC4B	Connected to the MTU2 connector (J16)	CN6, pin 15	SW5-4: ON
10	Vcc				
11	PC7/CKE/TIOC4C/IRQ6	CKE	Connected to the SDRAM CKE pin	-	SW5-4: OFF
		TIOC4C	Connected to the MTU2 connector (J16)	CN6, pin 16	SW5-4: ON
12	Vss				
13	PC8/CS3#/TIOC4D/IRQ7	CS3#	Connected to the SDRAM CS# pin	-	SW5-4: OFF
		TIOC4D	Connected to the MTU2 connector (J16)	CN6,pin 17	SW5-4: ON
14	PVcc				
15	PB1/A1	A1	Address bus	CN4, pin 1	
16	PB2/A2	A2	Address bus	CN4, pin 2	
17	PB3/A3	A3	Address bus	CN4, pin 3	
18	PB4/A4/TIOC0A	A4	Address bus	CN4, pin 4	
19	PB5/A5/TIOC0B	A5	Address bus	CN4, pin 5	
20	PB6/A6/TIOC0C	A6	Address bus	CN4, pin 6	
21	PB7/A7/TIOC0D	A7	Address bus	CN4, pin 9	
22	Vcc				
23	PB8/A8/TIOC1A	A8	Address bus	CN4, pin 10	
24	Vss				
25	PB9/A9/TIOC1B	A9	Address bus	CN4, pin 11	
26	PVcc				
27	PB10/A10/TIOC2A	A10	Address bus	CN4, pin12	
28	PB11/A11/TIOC2B	A11	Address bus	CN4, pin 13	
29	PB12/A12/TIOC3A	A12	Address bus	CN4, pin 14	
30	PB13/A13/TIOC3B	A13	Address bus	CN4, pin 17	
31	PB14/A14/TIOC3C	A14	Address bus	CN4, pin 18	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 4.2.2 SH7264 Pin Functions (2/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
32	PB15/A15/TIOC3D	A15	Address bus	CN4, pin 19	
33	Vcc				
34	PB16/A16/TIOC4A	A16	Address bus	CN4, pin 20	
35	Vss				
36	CKIO	CKIO	Connected to the SDRAM CLK pin	CN6, pin 20	
37	PVcc				
38	PB17/A17/TIOC4B	A17	Address bus	CN4, pin 21	
39	PB18/A18/TIOC4C	A18	Address bus	CN4, pin 22	
40	PB19/A19/TIOC4D	A19	Address bus	CN4, pin 25	
41	PB20/A20	A20	Address bus	CN4, pin 26	
42	PB21/A21	A21	Address bus	CN4, pin 27	
43	PB22/A22/CS4#	PB22	Switches the system setting/user interface	CN4, pin 28	Low: MD Hi: IO
44	PJ11/PWM2H/DACK1	PWM2H	Connected to the PWM connector (J5)	CN1, pin 1	JP3: 1-2
45	Vcc				
46	PJ10/PWM2G/DREQ1	PWM2G	Connected to the PWM connector (J5)	CN1, pin 2	JP3: 1-2
47	Vss				
48	PJ9/PWM2F/TEND1	PWM2F	Connected to the PWM connector (J5)	CN1, pin 4	JP3: 1-2
49	PVcc				
50	PJ8/PWM2E/RTS3#	PWM2E	Connected to the PWM connector (J5)	CN1, pin 5	JP3: 1-2
51	RES#	RES#	Reset input	CN7, pin 6	
52	NMI	NMI	Non-maskable interrupt	-	
53	PLLVcc				
54	PA3/MD_CLK0	PA3	Connected to SW6-6 as a user input port	CN1, pin 7	PB22: High
		MD_CLK0	Connected to SW5-1 as the clock mode input 0		PB22: Low
55	PLLVss				
56	PA2/MD_CLK1	PA21	Connected to SW6-5 as a user input port	CN1, pin 8	PB22: High
		MD_CLK1	Fixed high as the clock mode input 1		PB22: Low
57	EXTAL	EXTAL	Connects the system external clock to MCU	-	18 MHz
58	XTAL	XTAL	Open	-	
59	PA1/MD_BOOT0	PA1	Connected to LED3 as a user output port	CN1, pin 9	PB22: High
		MD_BOOT0	Connected to SW5-2 as the boot mode input 0		PB22: Low
60	PA0/MD_BOOT1	PA0	Connected to LED2 as a user output port	CN1, pin 10	PB22: High
		MD_BOOT1	Connected to SW5-3 as the boot mode input 1		PB22: Low
61	PJ7/TIOC1B/CTS3#	TIOC1B	Connected to the MTU2 connector (J16)	CN1, pin 12	
62	PJ6/TIOC1A/SCK3	TIOC1A	Connected to the MTU2 connector (J16)	CN1, pin 13	
63	PJ5/IERxD/TxD3	TxD3	Connected to the UART connector (J2)	CN1, pin 14	TTL level
64	Vss				
65	PJ4/IETxD/RxD3	RxD3	Connected to the UART connector (J2)	CN1, pin 15	TTL level
66	PVcc				
67	RTC_X1	RTC_X1	Connects a real-time clock resonator to MCU	-	32.768 kHz
68	RTC_X2	RTC_X2		-	
69	Vss				
70	PJ3/CRx1/CRx0/CRx1/IRQ1	IRQ1	IRQ1 switch	CN1, pin 17	JP6: 1-2
		CRx1	Connected to the CAN driver IC (U15)		JP6: 2-3
71	PJ2/CTx1/CTx0&CTx1/CS2#/ SCK0/LCD_M_DISP	CTx1	Connected to the CAN driver IC (U15)	CN1, pin 18	
		LCD_M_DISP	LCD AC control signal		
72	Vcc				
73	PJ1/CRx0/IERxD/IRQ0/RxD0	RxD0	Connected to the RS-232C connector (J10)	CN1, pin 19	JP5: 1-2
		CRx0	Connected to the CAN driver IC (U13)		JP5: 2-3
		IERxD	Connected to the IEBus™ driver IC		
74	Vss				

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 4.2.3 SH7264 Pin Functions (3/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
75	PJ0/CTx0/IETxD/CS1#/ TxD0/A0	TxD0	Connected to the RS-232C connector (J10)	CN1, pin 20	JP4: 1-2
		CTx0	Connected to the CAN driver IC (U13)		JP4: 2-3
		IETxD	Connected to the IEBus™ driver IC		
76	PVcc				
77	USB_X1	USB_X1	Connects the USB external clock to MCU	-	48 MHz
78	USB_X2	USB_X2	Open	-	
79	ASEMD#	ASEMD#	ASE mode select	-	H-UDI
80	USBDPVcc				
81	USBDPVss				
82	DM	DM	USB differential signal D- data	-	
83	DP	DP	USB differential signal D+ data	-	
84	VBUS	VBUS	VBUS input	-	
85	USBDVcc				
86	USBDVss				
87	REFRIN	REFRIN	Reference input	-	Connects a 5.6 k(((1% resistor
88	USBAPVcc				
89	USBAPVss				
90	USBAVcc				
91	USBAVss				
92	USBUVcc				
93	USBUVss				
94	PH0/AN0	AN0	Connected to the push-botton switch as key input	CN3, pin 4	
95	PH1/AN1	AN1	Connected to the push-botton switch as key input	CN3, pin 3	
96	PH2/AN2	AN2	Connected to the push-botton switch as key input	CN3, pin 8	
97	PH3/AN3	AN3	Connected to the push-botton switch as key input	CN3, pin 7	
98	PH4/AN4	-	-	CN3, pin 12	
99	PH5/AN5	-	-	CN3, pin 11	
100	AVss				
101	PH6/AN6	-	-	CN3, pin 16	
102	AVref				
103	PH7/AN7	AN7	Connected to the TMZ pin of the LCD module	CN3, pin 15	
104	AVcc				
105	TRST#	TRST#	Initialization-signal input pin	-	H-UDI
106	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Brake mode acknowledge	-	H-UDI
		ASEBRK#	Brake request		
107	TDO	TDO	Test data output	-	H-UDI
108	TDI	TDI	Test data input	-	H-UDI
109	TMS	TMS	Test mode select	-	H-UDI
110	TCK	TCK	Test clock	-	H-UDI
111	PG24/MISO1/TIOC0D	PG24	Connected to the PDN# pin of AK4524 and AK4353	CN9, pin 29	
		TIOC0D	Connected to the MTU2 connector (J16)		
112	PG23/MOSI1/TIOC0C	TIOC0C	Connected to the MTU2 connector (J16)	CN9, pin 30	
113	PVcc				
114	PG22/SSL10/TIOC0B	TIOC0B	Connected to the MTU2 connector (J16)	CN9, pin 27	
115	Vss				
116	PG21/RSPCK1/TIOC0A	TIOC0A	Connected to the MTU2 connector (J16)	CN9, pin 28	
117	Vcc				
118	PG20/LCD_EXTCLK/ MISO1/TxD7	LCD_EXTCLK	Connects the LCD module external clock to MCU	CN9, pin 26	Default: 5.33 MHz
119	PG19/LCD_CLK/ TIOC2B/MOSI1/RxD7	LCD_CLK	Connected to the CLK pin of the LCD module	CN9, pin 23	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 4.2.4 SH7264 Pin Functions (4/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
120	PG18/LCD_DE/TIOC2A/SSL10/ TxD6	LCD_DE	Connected to the EN pin of the LCD module	CN9, pin 24	
121	PG17/LCD_HSYNC/TIOC1B/ RSPCK1/RxD6	LCD_HSYNC	Connected to the HSYNC pin of the LCD module	CN9, pin 21	
122	PG16/LCD_VSYNC/TIOC1A/ TxD3/CTS1#	LCD_VSYNC	Connected to the VSYNC pin of the LCD module	CN9, pin 19	
123	PG15/LCD_DATA15/TIOC0D/ RxD3/RTS1#	LCD_DATA15	Connected to the D15 pin of the LCD module	CN9, pin 20	R5
124	PG14/LCD_DATA14/TIOC0C/ SCK1	LCD_DATA14	Connected to the D14 pin of the LCD module	CN9, pin 17	R4
125	PG13/LCD_DATA13/TIOC0B/ TxD1	LCD_DATA13	Connected to the D13 pin of the LCD module	CN9, pin 18	R3
126	PVcc				
127	PG12/LCD_DATA12/TIOC0A/ RxD1	LCD_DATA12	Connected to the D12 pin of the LCD module	CN9, pin 16	R2
128	Vss				
129	PG11/LCD_DATA11/SSITxD0/ IRQ3/TxD5/SIOFTxD	LCD_DATA11	Connected to the D11 pin of the LCD module	CN9, pin 13	R1, R0
130	Vcc				
131	PG10/LCD_DATA10/SSIRxD0/ IRQ2/RxD5/SIOFRxD	LCD_DATA10	Connected to the D10 pin of the LCD module	CN9, pin 14	G5
132	PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC	LCD_DATA9	Connected to the D9 pin of the LCD module	CN9, pin 11	G4
133	PG8/LCD_DATA8/SSISCK0/ RxD4/SIOFSCK	LCD_DATA8	Connected to the D8 pin of the LCD module	CN9, pin 12	G3
134	PG7/LCD_DATA7/SD_CD/PINT7	LCD_DATA7	Connected to the D7 pin of the LCD module	CN9, pin 9	G2
135	PG6/LCD_DATA6/SD_WP/PINT6	LCD_DATA6	Connected to the D6 pin of the LCD module	CN9, pin 7	G1
136	PG5/LCD_DATA5/SD_D1/PINT5	LCD_DATA5	Connected to the D5 pin of the LCD module	CN9, pin 8	G0
137	PG4/LCD_DATA4/SD_D0/PINT4	LCD_DATA4	Connected to the D4 pin of the LCD module	CN9, pin 6	B5
138	PVcc				
139	PG3/LCD_DATA3/SD_CLK/ PINT3	LCD_DATA3	Connected to the D3 pin of the LCD module	CN9, pin 3	B4
140	Vss				
141	PG2/LCD_DATA2/SD_CMD/ PINT2	LCD_DATA2	Connected to the D2 pin of the LCD module	CN9, pin 4	B3
142	Vcc				
143	PG1/LCD_DATA1/SD_D3/PINT1	LCD_DATA1	Connected to the D1 pin of the LCD module	CN9, pin 1	B2
144	PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#	LCD_DATA0	Connected to the D0 pin of the LCD module	CN9, pin 2	B1, B0
145	PK11/PWM2D/SSITxD0	SSITxD0	Connected to the SDTI pin of AK4353	CN7, pin 37	JP3: 2-3
		PWM2D	Connected to the PWM connector (J5)		JP3: 1-2
146	PK10/PWM2C/SSIRxD0	PK10	Connected to the PDN# pin of AK4353	CN7, pin 38	JP3: 2-3
		PWM2C	Connected to the PWM connector (J5)		JP3: 1-2
147	PK9/PWM2B/SSIWS0	SSIWS0	Connected to the LRCK pin of AK4353	CN7, pin 35	JP3: 2-3
		PWM2B	Connected to the PWM connector (J5)		JP3: 1-2
148	PK8/PWM2A/SSISCK0	SSISCK0	Connected to the BICK pin of AK4353	CN7, pin 36	JP3: 2-3
		PWM2A	Connected to the PWM connector (J5)		JP3: 1-2
149	AUDIO_X2	AUDIO_X2	Open	-	
150	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	-	Switched by JP7
151	PF12/BS#/MISO0/TIOC3D/ SPDIF_OUT	MISO0	Connected to the serial flash memory SO pin	-	SW5-6: OFF
		TIOC3D	Connected to the MTU2 connector (J16)	CN7, pin 33	SW5-6: ON
		SPDIF_OUT	Connected to the through-hole (MH2)		
152	PVcc				

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 4.2.5 SH7264 Pin Functions (5/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
153	PF11/A25/SSIDATA3/MOSI0/ TIOC3C/SPDIF_IN	MOSI0	Connected to the serial flash memory SI pin	-	SW5-6: OFF
		TIOC3C	Connected to the MTU2 connector (J16)	CN7, pin 31	SW5-6: ON
154	Vss				
155	PF10/A24/SSIWS3/SSL00/ TIOC3B/FCE#	SSL00	Connected to the serial flash memory CS# pin	-	SW5-5: ON SW5-6: OFF
		-	-	CN7, pin 32	SW5-5: ON SW5-6: ON
		FCE#	Connected to the NAND flash memory CE# pin	-	SW5-5: OFF
156	Vcc				
157	PF9/A23/SSISCK3/RSPCK0/ TIOC3A/FRB	RSPCK0	Connected to the serial flash memory SCK pin	-	SW5-5: OFF SW5-6: OFF
		-	-	CN7, pin 30	SW5-5: OFF SW5-6: ON
		FRB	Connected to the NAND flash memory R/B# pin	-	SW5-5: ON
158	PF8/CE2B#/SSIDATA3/DV_CLK	DV_CLK	Connected to the CLK_27MO pin of the video decoder IC	CN7, pin 27	
159	PF7/CE2A#/SSIWS3/ DV_DATA7/TCLKD	DV_DATA7	Connected to the D7 pin of the video decoder IC	CN7, pin 28	
160	PF6/CS6#/CE1B#/SSISCK3/ DV_DATA6/TCLKB	DV_DATA6	Connected to the D6 pin of the video decoder IC	CN7, pin 25	
161	PF5/CS5#/CE1A#/SSIDATA2/ DV_DATA5/TCLKC/AUDATA3	AUDATA3	Connected to the H-UDI connector (J3)	CN7, pin 23	AUD
		DV_DATA5	Connected to the D5 pin of the video decoder IC		
162	PF4/ICIOWR#/AH#/SSIWS2/ DV_DATA4/TxD3/AUDATA2	AUDATA2	Connected to the H-UDI connector (J3)	CN7, pin 24	AUD
		DV_DATA4	Connected to the D4 pin of the video decoder IC		
163	PF3/ICIORD#/SSISCK2/ DV_DATA3/RxD3/AUDATA1	AUDATA1	Connected to the H-UDI connector (J3)	CN7, pin 22	AUD
		DV_DATA3	Connected to the D3 pin of the video decoder IC		
164	PF2/BACK#/SSIDATA1/ DV_DATA2/TxD2/DACK0/ AUDATA0	AUDATA0	Connected to the H-UDI connector (J3)	CN7, pin 19	AUD
		DV_DATA2	Connected to the D2 pin of the video decoder IC		
165	PVcc				
166	PF1/BREQ#/SSIWS1/DV_DATA1 /RxD2/DREQ0/AUDSYNC#	AUDSYNC#	Connected to the H-UDI connector (J3)	CN7, pin 20	AUD
		DV_DATA1	Connected to the D1 pin of the video decoder IC		
167	Vss				
168	PF0/WAIT#/SSISCK1/DV_DATA0 /SCK2/TEND0/AUDCK	AUDCK	Connected to the H-UDI connector (J3)	CN7, pin 17	AUD
		DV_DATA0	Connected to the D0 pin of the video decoder IC		
169	Vcc				
170	PK7/PWM1H/SD_CD	PK7	Connected to the DB7 pin of the character LCD	CN7, pin 15	JP3: 1-2
		PWM1H	Connected to the PWM connector (J5)		
		SD_CD	Connected to the CD pin of the SD card slot		JP3: 2-3
171	PK6/PWM1G/SD_WP	PK6	Connected to the DB6 pin of the character LCD	CN7, pin 16	JP3: 1-2
		PWM1G	Connected to the PWM connector (J5)		
		SD_WP	Connected to the WP pin of the SD card slot		JP3: 2-3
172	PK5/PWM1F/SD_D1	PK5	Connected to the DB5 pin of the character LCD	CN7, pin 13	JP3: 1-2
		PWM1F	Connected to the PWM connector (J5)		
		SD_D1	Connected to the DAT1 pin of the SD card slot		JP3: 2-3
173	PK4/PWM1E/SD_D0	PK4	Connected to the DB4 pin of the character LCD	CN7, pin 14	JP3: 1-2
		PWM1E	Connected to the PWM connector (J5)		
		SD_D0	Connected to the DAT0 pin of the SD card slot		JP3: 2-3
174	PE5/SDA2/DV_HSYNC	DV_HSYNC	Connected to the HSYNC pin of the video decoder IC	CN7, pin 12	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

Table 4.2.6 SH7264 Pin Functions (6/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
175	PE4/SCL2/DV_VSYNC	DV_VSYNC	Connected to the VSYNC pin of the video decoder IC	CN7, pin 9	
176	PE3/SDA1/IRQ3	SDA1	Connected to the EEPROM SDA pin	CN7, pin 10	JP9: 1-2
		SDA1	Connected to the SDA/CDTI pin of AK4353		JP2: 1-2
		IRQ3	IRQ3 switch		JP2: 2-3
177	PE2/SCL1/IRQ2	SCL1	Connected to the EEPROM SCL pin	CN7, pin 7	JP8: 1-2
		SCL1	Connected to the SCL/CCLKI pin of AK4353		JP1: 1-2
		IRQ2	IRQ2 switch		JP1: 2-3
178	PE1/SDA0/IOIS16#/IRQ1/ TCLKA/ADTRG#	SDA0	Connected to the external IIC connector (J3)	CN7, pin 8	
		SDA0	Connected to the SDA pin of the video decoder IC		
179	PE0/SCL0/AUDIO_CLK/IRQ0	SCL0	Connected to the external IIC connector (J3)	CN7, pin 5	
		SCL0	Connected to the SCL pin of the video decoder IC		
180	PK3/PWM1D/SD_CLK	PK3	Connected to the DB3 pin of the character LCD	CN7, pin 3	JP3: 1-2
		PWM1D	Connected to the PWM connector (J5)		
		SD_CLK	Connected to the CLK pin of the SD card slot		JP3: 2-3
181	PVcc				
182	Vss				
183	PK2/PWM1C/SD_CMD	PK2	Connected to the DB2 pin of the character LCD	CN7, pin 4	JP3: 1-2
		PWM1C	Connected to the PWM connector (J5)		
		SD_CMD	Connected to the CMD pin of the SD card slot		JP3: 2-3
184	PK1/PWM1B/SD_D3	PK1	Connected to the DB1 pin of the character LCD	CN7, pin 1	JP3: 1-2
		PWM1B	Connected to the PWM connector (J5)		
		SD_D3	Connected to the DAT3 pin of the SD card slot		JP3: 2-3
185	PK0/PWM1A/SD_D2	PK0	Connected to the DB0 pin of the character LCD	CN7, pin 2	JP3: 1-2
		PWM1A	Connected to the PWM connector (J5)		
		SD_D2	Connected to the DAT2 pin of the SD card slot		JP3: 2-3
186	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 1	
187	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 3	
188	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 6	
189	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 8	
190	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 11	
191	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 13	
192	Vss				
193	PVcc				
194	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 16	
195	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 18	
196	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and the NAND flash memory WE# pin	CN8, pin 2	Auto-switch
197	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and the NAND flash memory ALE pin	CN8, pin 4	Auto-switch
198	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the NAND flash memory CLE pin	CN8, pin 7	Auto-switch
199	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the NAND flash memory RE# pin	CN8, pin 9	Auto-switch
200	PD3/D3/PWM1D	D3	Data bus	CN8, pin 12	
201	Vcc				
202	PD2/D2/PWM1C	D2	Data bus	CN8, pin 14	
203	Vss				
204	PD1/D1/PWM1B	D1	Data bus	CN8, pin 17	
205	PVcc				
206	PD0/D0/PWM1A	D0	Data bus	CN8, pin 19	
207	PC0/CS0#	CS0#	Connected to the NOR flash memory CE# pin	CN6, pin 5	
208	PC1/RD#	RD#	Connected to the NOR flash memory OE# pin	CN6, pin 6	

Legend: : 3.3 V power supply, : 1.2 V power supply, : GND

4.2.3 M3A-HS64G02 Module Availability

The following table shows which combination of modules can/cannot be used.

Table 4.2.7 M3A-HS64G02 Module Availability

				M3A-HS64												M3A-HS64+M3A-HS64G02																	
	SH7264 Peripheral Function	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory	USB	H-UDI (14-pin)	H-UDI (36-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	Character LCD	SD card	D/A converter	UART	IIC	LCD	IEBus™	CAN 0	CAN 1	Key input switch	IRQ2 switch	IRQ3 switch	PWM	Video decoder	MTU2
M3A-HS64	BSC	U6	NOR flash memory		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	BSC	U10	SDRAM	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*9
	FLCTL	U7	NAND flash memory	Y	Y		Y	*2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	RSPI	U9	Serial flash memory	Y	Y	*2	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*10
	USB	J1, and J2	USB	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	H-UDI, AUD	J3	H-UDI (36-pin)	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	**N**	Y
	I/O ports	LED2, and LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	*1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*5	Y	Y	Y	Y	Y	Y	Y
	I/O ports	SW5, and SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	*1	Y	Y			Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y			Y	Y	Y	Y	Y	Y	*3	*3	Y	Y	Y	Y	Y	Y	Y	Y
M3A-HS64+M3A-HS64G02	I/O ports	J1	Character LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	**N**
	SDHI	J4	SD card	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*6	Y	Y
	SSIF, IIC3	U10	D/A converter	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	*4	*4	*6	Y	Y
	SCIF	J2	UART	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	IIC3	J3	IIC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	VDC3	J10 to J12	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	*8	Y	Y	Y	Y	Y	*11
	IEBus	J13	IEBus™	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*3	Y	Y	Y	Y	Y	Y		*7	Y	Y	Y	Y	Y	Y	Y	Y
	RCAN	J14	CAN 0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*3	Y	Y	Y	Y	Y	Y	*7		Y	Y	Y	Y	Y	Y	Y	Y
	RCAN	J15	CAN 1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*5	Y	Y	Y	Y	Y	Y	Y	*8	Y	Y		Y	Y	Y	Y	Y	Y	Y
	I/O ports	SW4 to SW19	Key input switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y
	INTC	SW1	IRQ2 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*4	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y
	INTC	SW2	IRQ3 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*4	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y
	PWM	J5	PWM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	*6	*6	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y
	VDC3	U11	Video decoder	Y	Y	Y	Y	Y	Y	Y	**N**	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y
	MTU2	LED1 to LED14	MTU2	Y	*9	Y	Y	*10	Y	Y	Y	Y	Y	Y	Y	Y	**N**	Y	Y	Y	Y	*11	Y	Y	Y	Y	Y	Y	Y	Y	

Y: Yes N: No

Notes:
1: When using LED2, and LED3, SW5-1, SW5-2, and SW5-3 on the M3A-HS64 cannot be used.
2: PF9, and PF10 are multiplex pins. When setting SW5-5, and SW5-6 on the M3A-HS64, either serial or NAND can be used.
3: When changing JP4, and JP5 settings on the M3A-HS64, only one module can be used at these sections.
4: When changing JP1, and JP2 setting on the M3A-HS64G02, only one module can be used at these intersections.
5: When changing JP6 setting on the M3A-HS64, either CAN 1 or IRQ1 switch can be used.
6: When changing JP3 setting on the M3A-HS64G02, only one module can be used at these sections.
7: When changing JP5, and JP9 settings on the M3A-HS64G02, either CAN 0 or an IEBus can be used.
8: PJ2 is a multiplex pin. When using the signal LCD_M_DISP, CAN1 cannot be used. When using CAN 1, the signal LCD_M_DISP cannot be used.
9: PC5 to PC8 are multiplex pins. When setting SW5-4 on the M3A-HS64, either MTU2 or SDRAM can be used.
10: PF11, and PF12 are multiplex pins. When setting SW5-6 on the M3A-HS64, either MTU2 or serial can be used.
11: The PG21 pin is connected to both the LCD and MTU2 modules. Therefore, any operation to either module will result in both modules performing the same operation.

4.2.4 SH7264 Multiplex Pins Used on the M3A-HS64G02

Table 4.2.8 to Table 4.2.21 list SH7264 multiplex pin functions used on the M3A-HS64G02.

These multiplex pins are set as port input pins by default. Set the MD bit in the port control register to use the SH7264 peripheral functions (except I/O ports).

Table 4.2.8 SH7264 Multiplex Pin Functions (BSC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
BSC	CS0#	PCCR0	PC0MD0 = B'1	PC0/CS0# (1)
	CS3#	PCCR2	PC8MD[1:0] = B'01	PC8/CS3#/TIOC4D/IRQ7
	RD#	PCCR0	PC1MD0 = B'1	PC1/RD# (1)
	WE0#/DQML	PCCR0	PC3MD0 = B'1	PC3/WE0#/DQML
	WE1#/DQMU/WE#	PCCR1	PC4MD0 = B'1	PC4/WE1#/DQMU/WE#
	RAS#	PCCR1	PC5MD[1:0] = B'01	PC5/RAS#/TIOC4A/IRQ4
	CAS#	PCCR1	PC6MD[1:0] = B'01	PC6/CAS#/TIOC4B/IRQ5
	CKE	PCCR1	PC7MD[1:0] = B'01	PC7/CKE/TIOC4C/IRQ6
	RD/WR#	PCCR0	PC2MD0 = B'1	PC2/RD/WR#
	A21	PBCR5	PB21MD0 = B'1	PB21/A21
	D15	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H (1)
	D14	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G (1)
	D13	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F (1)
	D12	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E (1)
	D11	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D (1)
	D10	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C (1)
	D9	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B (1)
	D8	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A (1)
	D7	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H (1)
	D6	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G (1)
	D5	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F (1)
	D4	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E (1)
	D3	PDCR0	PD3MD[1:0] = B'01	PD3/D3/PWM1D (1)
	D2	PDCR0	PD2MD[1:0] = B'01	PD2/D2/PWM1C (1)
	D1	PDCR0	PD1MD[1:0] = B'01	PD1/D1/PWM1B (1)
	D0	PDCR0	PD0MD[1:0] = B'01	PD0/D0/PWM1A (1)

Note 1: For boot modes 1 to 3

Table 4.2.9 SH7264 Multiplex Pin Functions (INTC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
INTC	IRQ3	PECR0	PE3MD[1:0] = B'11	PE3/SDA1/IRQ3
	IRQ2	PECR0	PE2MD[1:0] = B'11	PE2/SCL1/IRQ2
	IRQ1	PJCR0	PJ3MD[1:0] = B'11	PJ3/CRx1/CRx0&CRx1/IRQ1

Table 4.2.10 SH7264 Multiplex Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SCIF	TxD3	PJCR1	PJ5MD[1:0] = B'10	PJ5/IERxD/TxD3
	RxD3	PJCR1	PJ4MD[1:0] = B'10	PJ4/IETxD/RxD3
	RxD0	PJCR0	PJ1MD[2:0] = B'100	PJ1/CRx0/IERxD/IRQ0/RxD0
	TxD0	PJCR0	PJ0MD[2:0] = B'100	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 4.2.11 SH7264 Multiplex Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
IIC3	SDA1	PECR0	PE3MD[1:0] = B'01	PE3/SDA1/IRQ3
	SCL1	PECR0	PE2MD[1:0] = B'01	PE2/SCL1/IRQ2
	SDA0	PECR0	PE1MD[2:0] = B'001	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#
	SCL0	PECR0	PE0MD[1:0] = B'01	PE0/SCL0/AUDIO_CLK/IRQ0

Table4.2.12 SH7264 Multiplex Pin Functions (RCAN-TL1)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
RCAN-TL1	CRx1	PJCR0	PJ3MD[1:0] = B'01	PJ3/CRx1/CRx0&CRx1/IRQ1
	CTx1	PJCR0	PJ2MD[2:0] = B'001	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP
	CRx0	PJCR0	PJ1MD[2:0] = B'001	PJ1/CRx0/IERxD/IRQ0/RxD0
	CTx0	PJCR0	PJ0MD[2:0] = B'001	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 4.2.13 SH7264 Multiplex Pin Functions (IEB)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
IEB	IERxD	PJCR0	PJ1MD[2:0] = B'010	PJ1/CRx0/IERxD/IRQ0/RxD0
	IETxD	PJCR0	PJ0MD[2:0] = B'010	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 4.2.14 SH7264 Multiplex Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E
	FCE#	PFCR2	PF10MD[2:0] = B'101	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	FRB	PFCR2	PF9MD[2:0] = B'101	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 4.2.15 SH7264 Multiplex Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SDHI	SD_CD	PKCR1	PK7MD[1:0] = B'10	PK7/PWM1H/SD_CD
	SD_WP	PKCR1	PK6MD[1:0] = B'10	PK6/PWM1G/SD_WP
	SD_D1	PKCR1	PK5MD[1:0] = B'10	PK5/PWM1F/SD_D1
	SD_D0	PKCR1	PK4MD[1:0] = B'10	PK4/PWM1E/SD_D0
	SD_CLK	PKCR0	PK3MD[1:0] = B'10	PK3/PWM1D/SD_CLK
	SD_CMD	PKCR0	PK2MD[1:0] = B'10	PK2/PWM1C/SD_CMD
	SD_D3	PKCR0	PK1MD[1:0] = B'10	PK1/PWM1B/SD_D3
	SD_D2	PKCR0	PK0MD[1:0] = B'10	PK0/PWM1A/SD_D2

Table 4.2.16 SH7264 Multiplex Pin Functions (MTU2)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
MTU2	TIOC4D	PCCR2	PC8MD[1:0] = B'10	PC8/CS3#/TIOC4D/IRQ7
	TIOC4C	PCCR1	PC7MD[1:0] = B'10	PC7/CKE/TIOC4C/IRQ6
	TIOC4B	PCCR1	PC6MD[1:0] = B'10	PC6/CAS#/TIOC4B/IRQ5
	TIOC4A	PCCR1	PC5MD[1:0] = B'10	PC5/RAS#/TIOC4A/IRQ4
	TIOC3D	PFCR3	PF12MD[2:0] = B'100	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
	TIOC3C	PFCR2	PF11MD[2:0] = B'100	PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN
	TIOC2B	PCCR2	PC10MD0 = B'1	PC10/TIOC2B
	TIOC2A	PCCR2	PC9MD0 = B'1	PC9/TIOC2A
	TIOC1B	PJCR1	PJ7MD[1:0] = B'01	PJ7/TIOC1B/CTS3#
	TIOC1A	PJCR1	PJ6MD[1:0] = B'01	PJ6/TIOC1A/SCK3
	TIOC0D	PGCR6	PG24MD[1:0] = B'10	PG24/MISO1/TIOC0D
	TIOC0C	PGCR5	PG23MD[1:0] = B'10	PG23/MOSI1/TIOC0C
	TIOC0B	PGCR5	PG22MD[1:0] = B'10	PG22/SSL10/TIOC0B
	TIOC0A	PGCR5	PG21MD[1:0] = B'10	PG21/RSPCK1/TIOC0A
	TCLKD	PFCR1	PF7MD[2:0] = B'100	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
	TCLKC	PFCR1	PF5MD[2:0] = B'100	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5/TCLKC/ AUDATA3
	TCLKB	PFCR1	PF6MD[2:0] = B'100	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/TCLKB
	TCLKA	PECR0	PE1MD[2:0] = B'100	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#

Table4.2.17 SH7264 Multiplex Pin Functions (SSIF)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
SSIF	SSITxD0	PKCR2	PK11MD[1:0] = B'10	PK11/PWM2D/SSITxD0
	SSIWS0	PKCR2	PK9MD[1:0] = B'10	PK9/PWM2B/SSIWS0
	SSISCK0	PKCR2	PK8MD[1:0] = B'10	PK8/PWM2A/SSISCK0

Table 4.2.18 SH7264 Multiplex Pin Functions (ADC)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
ADC	AN7	PHCR1	PH7MD0 = B'1	PH7/AN7
	AN3	PHCR0	PH3MD0 = B'1	PH3/AN3
	AN2	PHCR0	PH2MD0 = B'1	PH2/AN2
	AN1	PHCR0	PH1MD0 = B'1	PH1/AN1
	AN0	PHCR0	PH0MD0 = B'1	PH0/AN0

Table 4.2.19 SH7264 Multiplex Pin Functions (VDC3)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
VDC3	DV_CLK	PFCR2	PF8MD[1:0] = B'11	PF8/CE2B#/SSIDATA3/DV_CLK
	DV_DATA7	PFCR1	PF7MD[2:0] = B'011	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
	DV_DATA6	PFCR1	PF6MD[2:0] = B'011	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/TCLKB
	DV_DATA5	PFCR1	PF5MD[2:0] = B'011	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5/TCLKC/AUDATA3
	DV_DATA4	PFCR1	PF4MD[2:0] = B'011	PF4/ICIOWR#/AH#/SSIWS2/DV_DATA4/TxD3/AUDATA2
	DV_DATA3	PFCR0	PF3MD[2:0] = B'011	PF3/ICIORD#/SSISCK2/DV_DATA3/RxD3/AUDATA1
	DV_DATA2	PFCR0	PF2MD[2:0] = B'011	PF2/BACK#/SSIDATA1/DV_DATA2/TxD2/DACK0/AUDATA0
	DV_DATA1	PFCR0	PF1MD[2:0] = B'011	PF1/BREQ#/SSIWS1/DV_DATA1/RxD2/DREQ0/AUDSYNC#
	DV_DATA0	PFCR0	PF0MD[2:0] = B'011	PF0/WAIT#/SSISCK1/DV_DATA0/SCK2/TEND0/AUDCK
	DV_HSYNC	PECR1	PE5MD[1:0] = B'11	PE5/SDA2/DV_HSYNC
	DV_VSYNC	PECR1	PE4MD[1:0] = B'11	PE4/SCL2/DV_VSYNC
	LCD_EXTCLK	PGCR5	PG20MD[2:0] = B'001	PG20/LCD_EXTCLK/MISO1/TxD7
	LCD_CLK	PGCR4	PG19MD[2:0] = B'001	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7
	LCD_DE	PGCR4	PG18MD[2:0] = B'001	PG18/LCD_DE/TIOC2A/SSL10/TxD6
	LCD_HSYNC	PGCR4	PG17MD[2:0] = B'001	PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6
	LCD_VSYNC	PGCR4	PG16MD[2:0] = B'001	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#
	LCD_DATA15	PGCR3	PG15MD[2:0] = B'001	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
	LCD_DATA14	PGCR3	PG14MD[2:0] = B'001	PG14/LCD_DATA14/TIOC0C/SCK1
	LCD_DATA13	PGCR3	PG13MD[2:0] = B'001	PG13/LCD_DATA13/TIOC0B/TxD1
	LCD_DATA12	PGCR3	PG12MD[2:0] = B'001	PG12/LCD_DATA12/TIOC0A/RxD1
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'001	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/SIOFTxD
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'001	PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/SIOFRxD
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'001	PG9/LCD_DATA9/SSIWS0/TxD4/SIOFSYNC
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'001	PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK
	LCD_DATA7	PGCR1	PG7MD[1:0] = B'01	PG7/LCD_DATA7/SD_CD/PINT7
	LCD_DATA6	PGCR1	PG6MD[1:0] = B'01	PG6/LCD_DATA6/SD_WP/PINT6
	LCD_DATA5	PGCR1	PG5MD[1:0] = B'01	PG5/LCD_DATA5/SD_D1/PINT5
	LCD_DATA4	PGCR1	PG4MD[1:0] = B'01	PG4/LCD_DATA4/SD_D0/PINT4
	LCD_DATA3	PGCR0	PG3MD[1:0] = B'01	PG3/LCD_DATA3/SD_CLK/PINT3
	LCD_DATA2	PGCR0	PG2MD[1:0] = B'01	PG2/LCD_DATA2/SD_CMD/PINT2
	LCD_DATA1	PGCR0	PG1MD[1:0] = B'01	PG1/LCD_DATA1/SD_D3/PINT1
	LCD_DATA0	PGCR7	PG0MD[2:0] = B'001	PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#
	LCD_M_DISP	PJCR0	PJ2MD[2:0] = B'101	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP

Table 4.2.20 SH7264 Multiplex Pin Functions (PWM)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
PWM	PWM2H	PJCR2	PJ11MD[1:0] = B'01	PJ11/PWM2H/DACK1
	PWM2G	PJCR2	PJ10MD[1:0] = B'01	PJ10/PWM2G/DREQ1
	PWM2F	PJCR2	PJ9MD[1:0] = B'01	PJ9/PWM2F/TEND1
	PWM2E	PJCR2	PJ8MD[1:0] = B'01	PJ8/PWM2E/RTS3#
	PWM2D	PKCR2	PK11MD[1:0] = B'01	PK11/PWM2D/SSITxD0
	PWM2C	PKCR2	PK10MD[1:0] = B'01	PK10/PWM2C/SSIRxD0
	PWM2B	PKCR2	PK9MD[1:0] = B'01	PK9/PWM2B/SSIWS0
	PWM2A	PKCR2	PK8MD[1:0] = B'01	PK8/PWM2A/SSISCK0
	PWM1H	PKCR1	PK7MD[1:0] = B'01	PK7/PWM1H/SD_CD
	PWM1G	PKCR1	PK6MD[1:0] = B'01	PK6/PWM1G/SD_WP
	PWM1F	PKCR1	PK5MD[1:0] = B'01	PK5/PWM1F/SD_D1
	PWM1E	PKCR1	PK4MD[1:0] = B'01	PK4/PWM1E/SD_D0
	PWM1D	PKCR0	PK3MD[1:0] = B'01	PK3/PWM1D/SD_CLK
	PWM1C	PKCR0	PK2MD[1:0] = B'01	PK2/PWM1C/SD_CMD
	PWM1B	PKCR0	PK1MD[1:0] = B'01	PK1/PWM1B/SD_D3
	PWM1A	PKCR0	PK0MD[1:0] = B'01	PK0/PWM1A/SD_D2

Table 4.2.21 SH7264 Multiplex Pin Functions (PORT)

Peripheral Function	Pin Name	SH7264 Port Control Register		SH7264 Multiplex Pin Name
		Register Name	MD bit Setting	
PORT	PK10	PKCR2	PK10MD[1:0] = B'00	PK10/PWM2C/SSIRxD0
	PK7	PKCR1	PK7MD[1:0] = B'00	PK7/PWM1H/SD_CD
	PK6	PKCR1	PK6MD[1:0] = B'00	PK6/PWM1G/SD_WP
	PK5	PKCR1	PK5MD[1:0] = B'00	PK5/PWM1F/SD_D1
	PK4	PKCR1	PK4MD[1:0] = B'00	PK4/PWM1E/SD_D0
	PK3	PKCR0	PK3MD[1:0] = B'00	PK3/PWM1D/SD_CLK
	PK2	PKCR0	PK2MD[1:0] = B'00	PK2/PWM1C/SD_CMD
	PK1	PKCR0	PK1MD[1:0] = B'00	PK1/PWM1B/SD_D3
	PK0	PKCR0	PK0MD[1:0] = B'00	PK0/PWM1A/SD_D2
	PC10	PCCR2	PC10MD0 = B'0	PC10/TIOC2B
	PC9	PCCR2	PC9MD0 = B'0	PC9/TIOC2A
	PB22	PBCR5	PB22MD[1:0] = B'00	PB22/A22/CS4#

4.3 LCD Module Interface

4.3.1 LCD Module Interface

The M3A-HS64G02 includes two flexible connectors and one MIL-spec connector for connecting LCD modules.

The SH7264 on-chip VDC3 controls the LCD modules.

The following figure shows the LCD module interface block diagram.

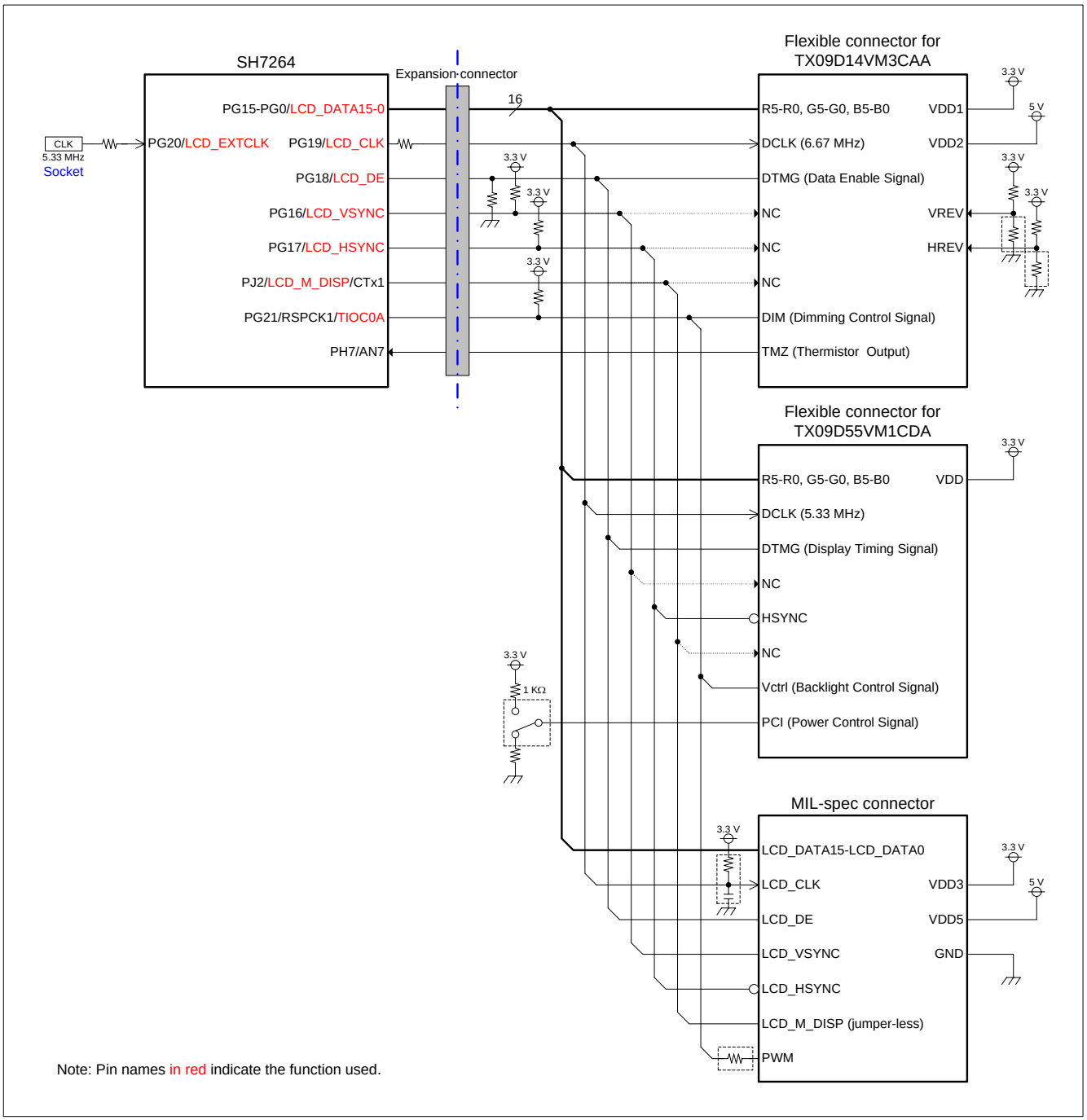


Figure 4.3.1 LCD Module Interface Block Diagram

4.3.2 Character LCD Module with LED Backlight

The M3A-HS64G02 includes a connector for 16 x 2 semi-transmissive character LCD module (SD1602H, SUNLIKE). The SH7264 general-purpose port output controls the character LCD module. The M3A-HS64G02 is intended only for writing from the SH7264 to the character LCD modules. Therefore, the character LCD module R/W signal is fixed low.

The M3A-HS64G02 also includes a variable resister (VR1) for the LCD driver voltage adjustment to control the LCD contrast and a variable resister (VR2) for LCD backlight adjustment.

SH7264 PK7 to PK0 pins are also used as SDHI pins. When using the character LCD module, SDHI cannot be used. The figure below shows the character LCD module block diagram The table below lists the jumper setting (JP3).

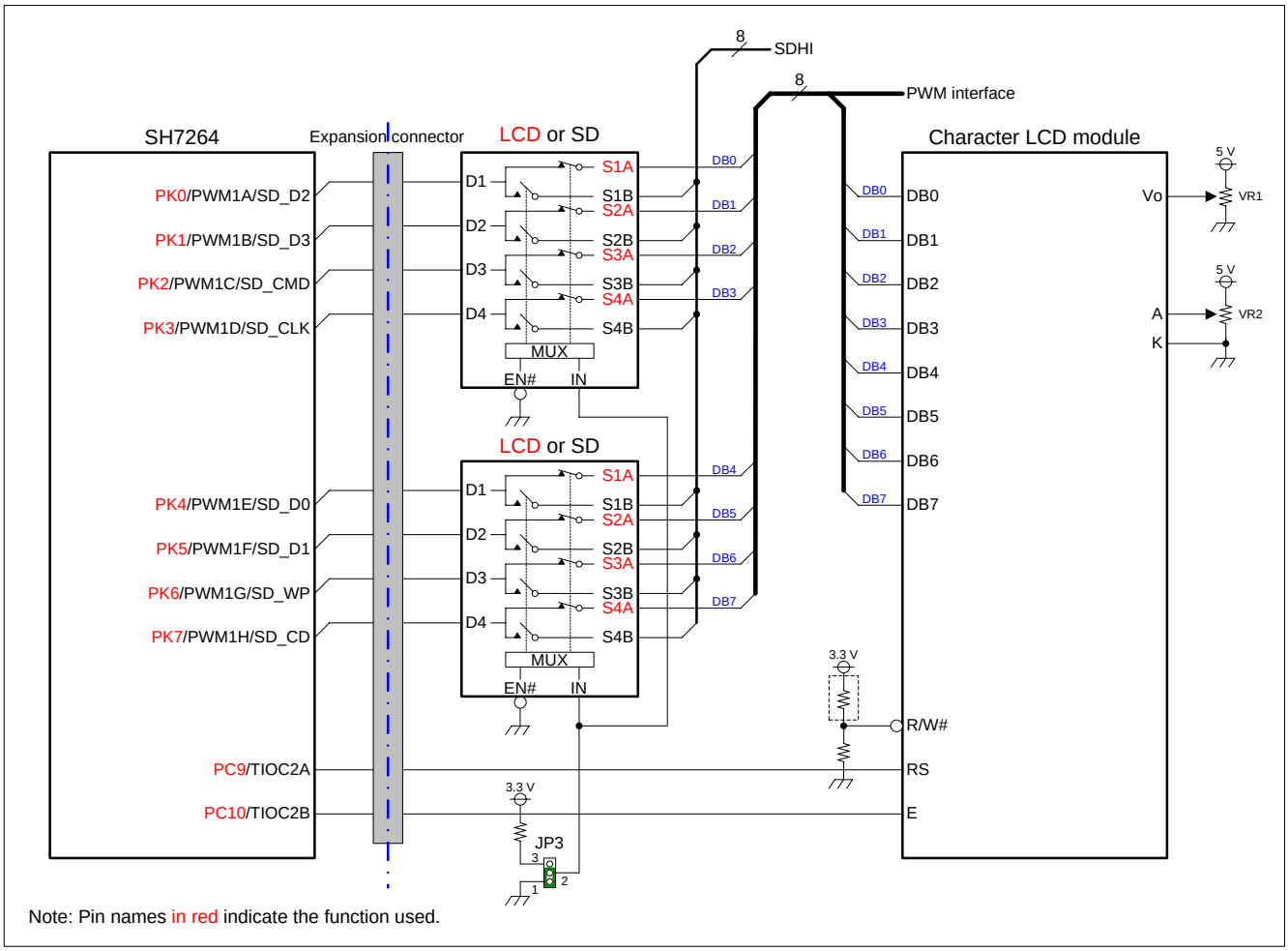


Figure 4.3.2 Character LCD Module Block Diagram

Table 4.3.1 Jumper Setting (JP3)

Number	1-2 (Low)	2-3 (High)
JP3	Connected to the character LCD interface	Connected to the SDHI (default)

4.4 Audio Module

The M3A-HS64G02 includes a 96 KHz 24-bit D/A converter with DIT (AK4353, Asahi Kasei EMD Corporation).

➢ AK4353, D/A Converter

SH7264 IIC3, SSIF, and I/O ports control AK4353.

- SH7264 IIC3 (Channel 1): Accesses the AK4353 registers to initialize AK4353, format data, and configure the attenuator
- SH7264 SSIF (Channel 0): Outputs the audio data
- SH7264 I/O ports (PK10): Powers down AK4353 at low

Powers up AK4353 at high

Note: The M3A-HS64 allows for selecting 12.2880 MHz or 11.2896 MHz as the AK4353 system clock.

The figure below shows the D/A converter block diagram. The table below lists the jumpers setting (JP1 to JP3, and JP7).

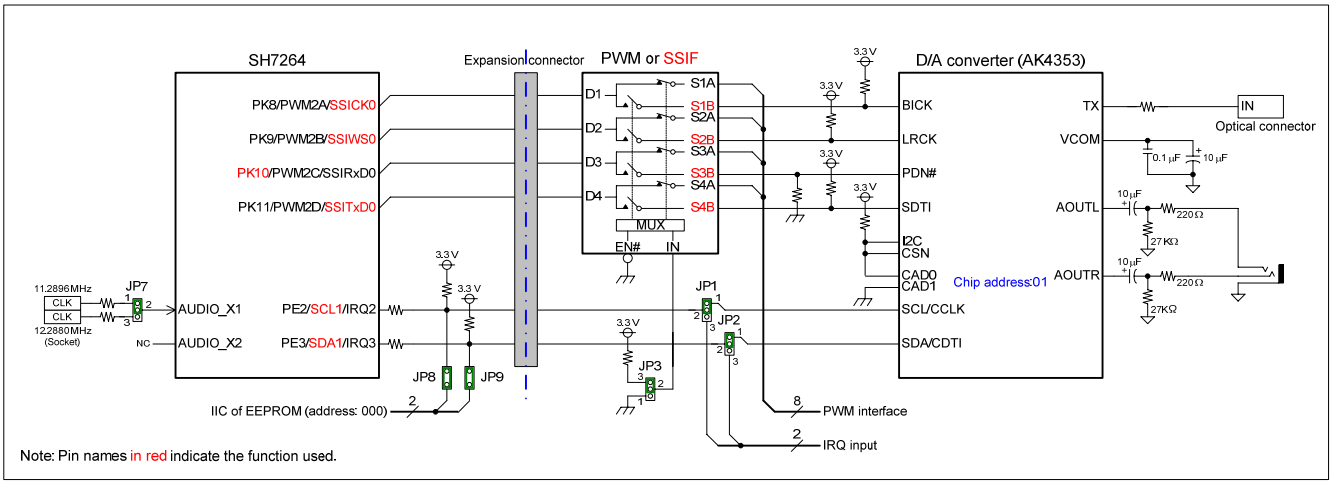


Figure 4.4.1 D/A Converter Block Diagram

Table 4.4.1 Jumpers Setting (JP1 to JP3, JP7)

Number	1-2	2-3
JP1	IIC3 mode (Sets the PE2 as the SCL1 output pin)	IRQ mode (Sets the PE2 as the IRQ2 input pin, default)
JP2	IIC3 mode (Sets the PE3 as the SDA1 I/O pin)	IRQ mode (Sets the PE3 as the IRQ3 input pin, default)
JP3	Connected to the PWM interface (Low, default)	Connected to the SSIF (High)
JP7	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

4.5 Video Signal Input Module

The M3A-HS64G02 includes a video decoder IC (AK8851, Asahi Kasei EMD Corporation). The M3A-HS64G02 also includes an RCA connector and an S-Video connector for NTSC and PAL video signal input as video signal input to input the digital signals to the SH7264 VDC3 module via the video decoder IC. The SH7264 on-chip IIC3 controls the video decoder.

The following figure shows the video signal input module block diagram.

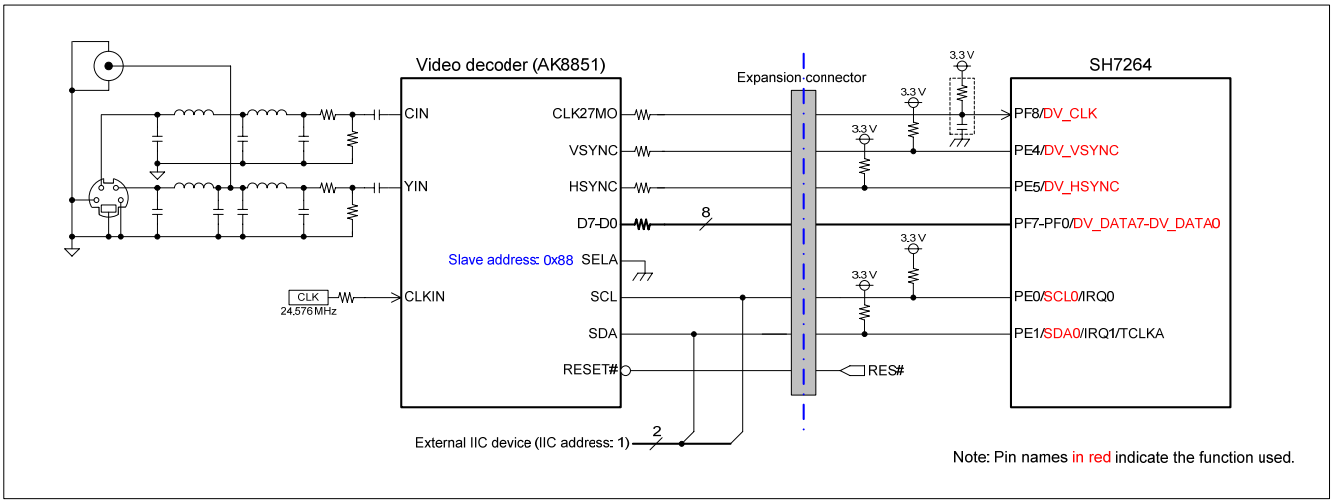


Figure 4.5.1 Video Signal Input Module Block Diagram

4.6 SD Card Interface

The M3A-HS64G02 includes an SD card slot to interface the SH7264 built-in SD Host Interface (SDHI) with the SD card slot. The figure below shows the SD card interface block diagram.

The SDHI pin is also used as PL7 to PK0 pins to control the character LCD module. When using the SDHI, the character LCD module cannot be used. The table below lists the jumper setting (JP3).

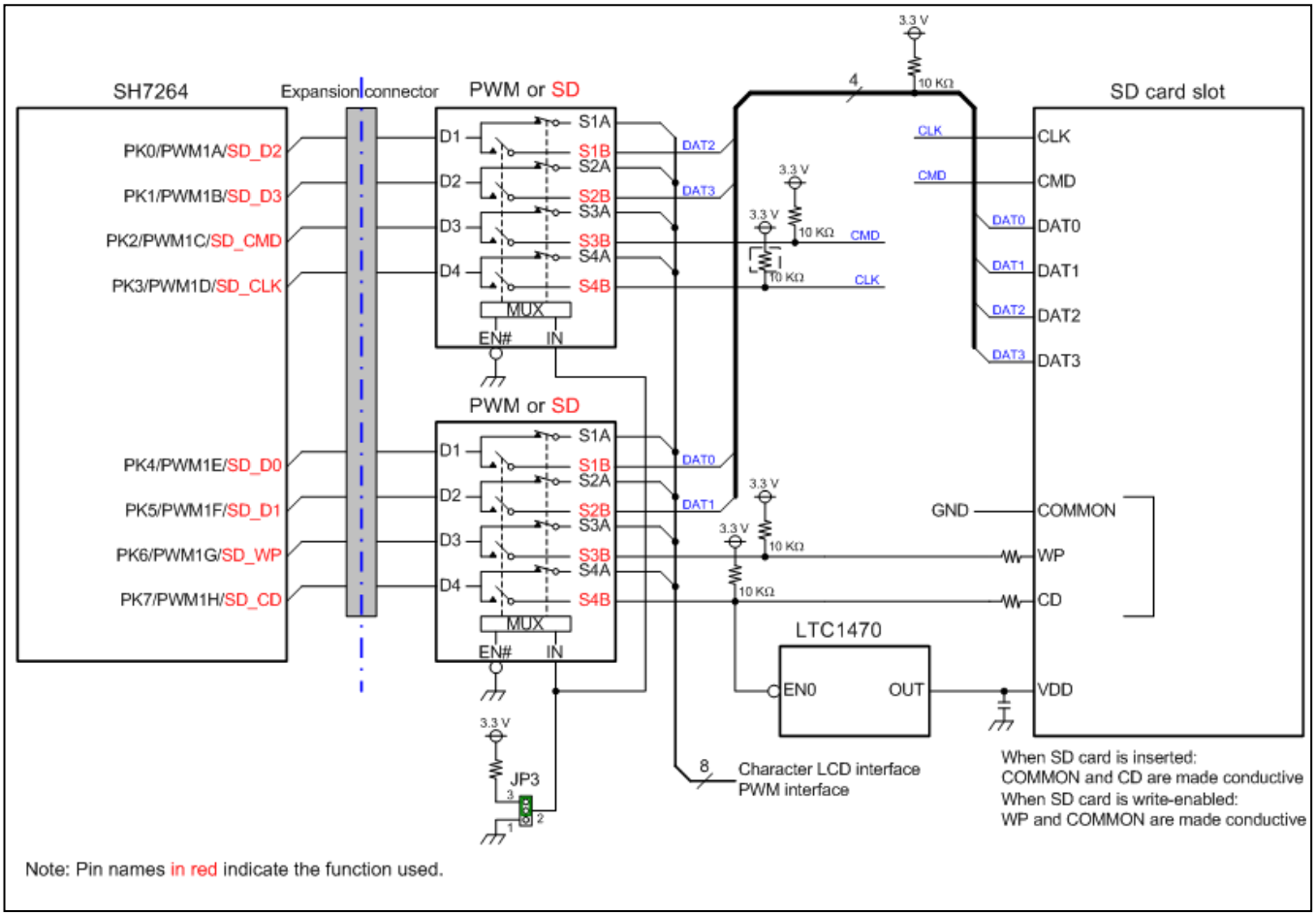


Figure 4.6.1 SD Card Interface Block Diagram

Table 4.6.1 Jumper Setting (JP3)

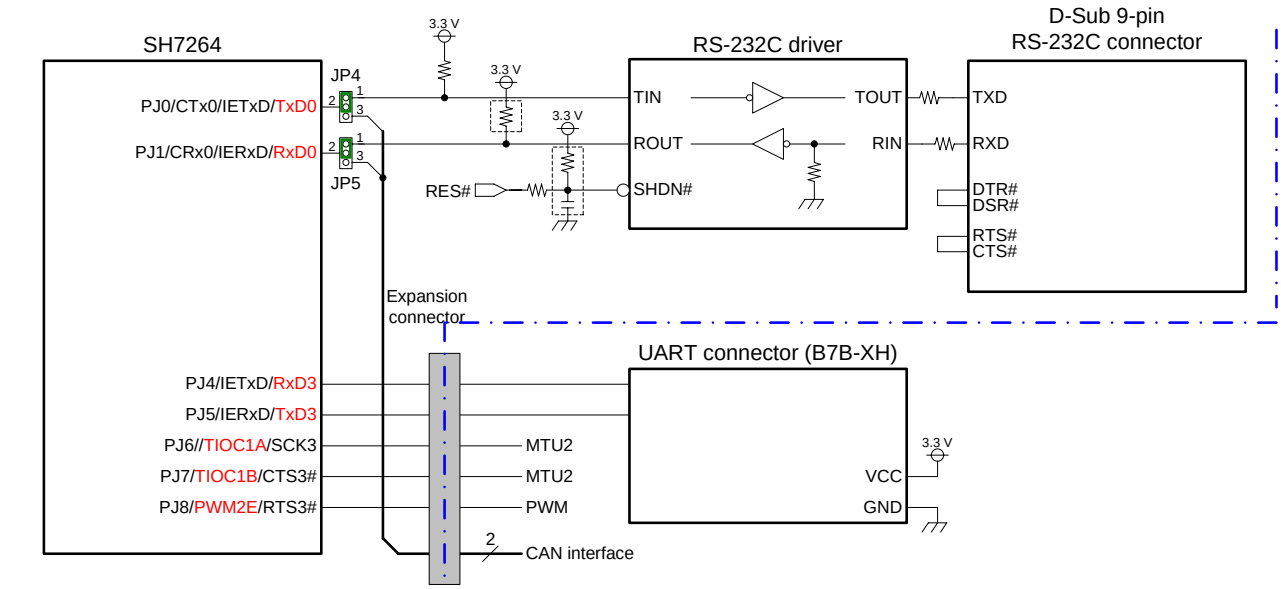
Number	1-2 (Low)	2-3 (High)
JP3	Connected to the PWM interface (default)	Connected to the SDHI

4.7 UART Interface

The SH7264 includes a Serial Communication Interface with FIFO (SCIF). SCIF channel 3 is connected to the UART connector (7-pin, 2.5 mm pitch) on the M3A-HS64G02, at TTL level.

The SH7264 SCIF channel 3 pin is also used as the Multi Function Timer Pulse Unit 2 (MTU2) pin and the Motor Control PWM Timer pin.

The figure below shows the UART interface block diagram. The table below lists the jumpers setting (JP4, and JP5).



Note: Pin names in red indicate the function used.

Figure 4.7.1 UART Interface Block Diagram

Table 4.7.1 Jumper Setting (JP4, and JP5 on the M3A-HS64)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins

4.8 CAN Interface

The SH7264 includes an RCAN-TL1 (Renesas CAN Time Trigger Level 1), the Controller Area Network. RCAN-TL1 channels 0 and 1 are connected to the CAN connector (3-pin, 2.5 mm pitch) on the M3A-HS64G02 via the voltage level shifter and the CAN driver IC.

The RCAN-TL1 channel 0 pin is also used as the SCIF channel 0 pin, and the IEBus™ controller (IEB) pin.

The figure below shows the CAN interface block diagram. Table 4.8.1 lists the jumpers setting (JP4 to JP6 on the M3A-HS64). Table 4.8.2 and Table 4.8.3 list jumpers setting (JP4, JP5, JP8, and JP9).

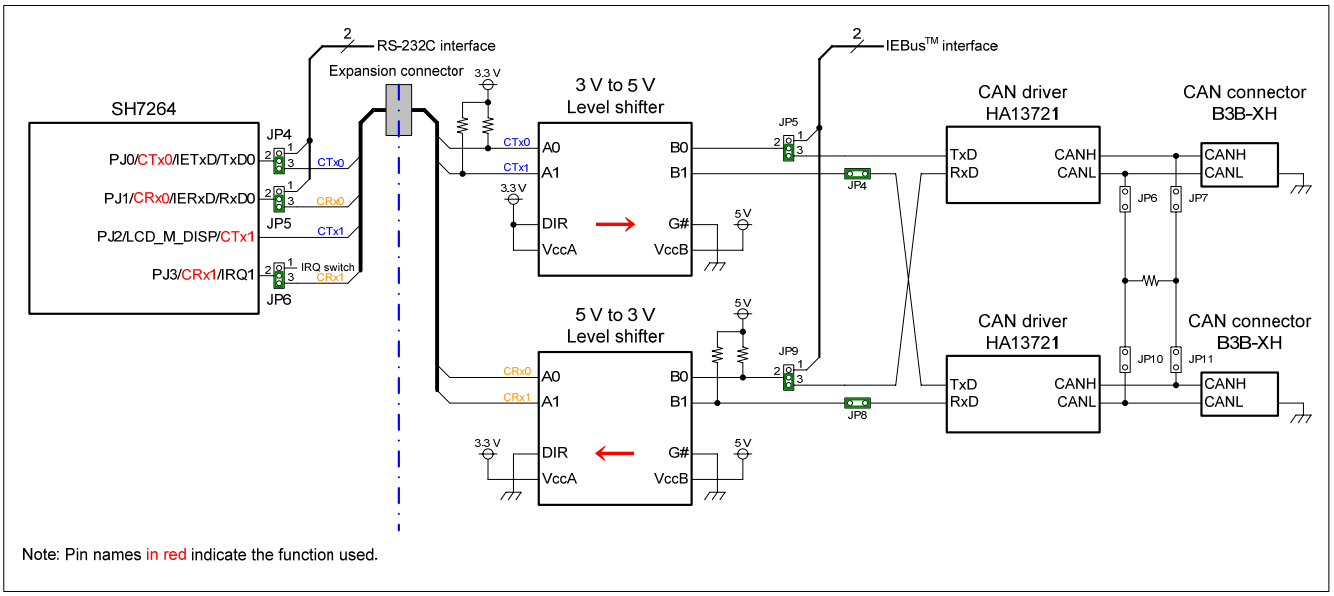


Figure 4.8.1 CAN Interface Block Diagram

Table 4.8.1 M3A-HS64 Jumpers Setting (JP4 to JP6)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins
JP6	Selects the IRQ1 switch	Selects the CRx1 (RCAN-TL1) pin

Table 4.8.2 Jumpers Setting (JP5, and JP9)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

Table 4.8.3 Jumpers Setting (JP4, and JP8)

Number	1-2	None (Open)
JP4	Normal mode (Connects the CTx1 pin) - default	Debug mode (Leaves the CTx1 pin disconnected)
JP8	Normal mode (Connects the CRx1 pin) - default	Debug mode (Leaves the CRx1 pin disconnected)

4.9 IEBus™ Interface

The SH7264 includes an IEBus™ controller (IEB). IEBus™ (Inter Equipment Bus™) is the bus for digital data transfer system on a small scale. The SH7264 IEB pin is connected to the IEBus connector (4-pin, 2.5 mm) via the voltage level shifter and the IEBus™ driver IC on the M3A-HS64G02.

The IEB pin is also used as the SCIF channel 0 pin and the RCAN-TL1 channel 0 pin.

The figure below shows the IEBus™ interface block diagram. Table 4.9.1 lists the jumpers setting (JP4, and JP5 on the M3A-HS64). Table 4.9.2 lists the jumpers setting (JP5, and JP9).

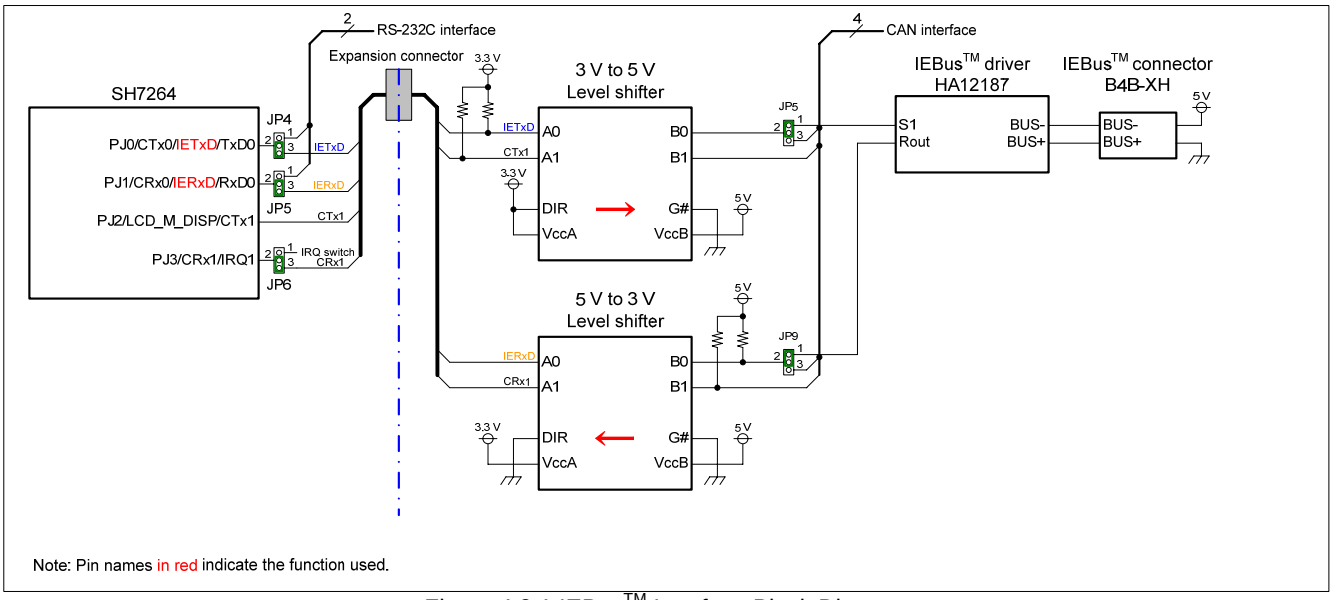


Figure 4.9.1 IEBus™ Interface Block Diagram

Table 4.9.1 Jumpers Setting (JP4, and JP5 on the M3A-HS64)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins

Table 4.9.2 Jumpers Setting (JP5, and JP9)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

4.10 PWM Interface

The SH7264 includes two channels of on-chip Motor Control Pulse Width Modulator (PWM) timer with a maximum of eight pulse outputs per channel. The SH7264 PWM output pin is connected to a 20-pin MIL-spec connector on the M3A-HS64G02 via the voltage level shifter. The PWM output pin is also used as the SDHI pin and SSIF channel 0 pin.

The figure below shows the PWM interface block diagram. The table below lists the jumper setting (JP3).

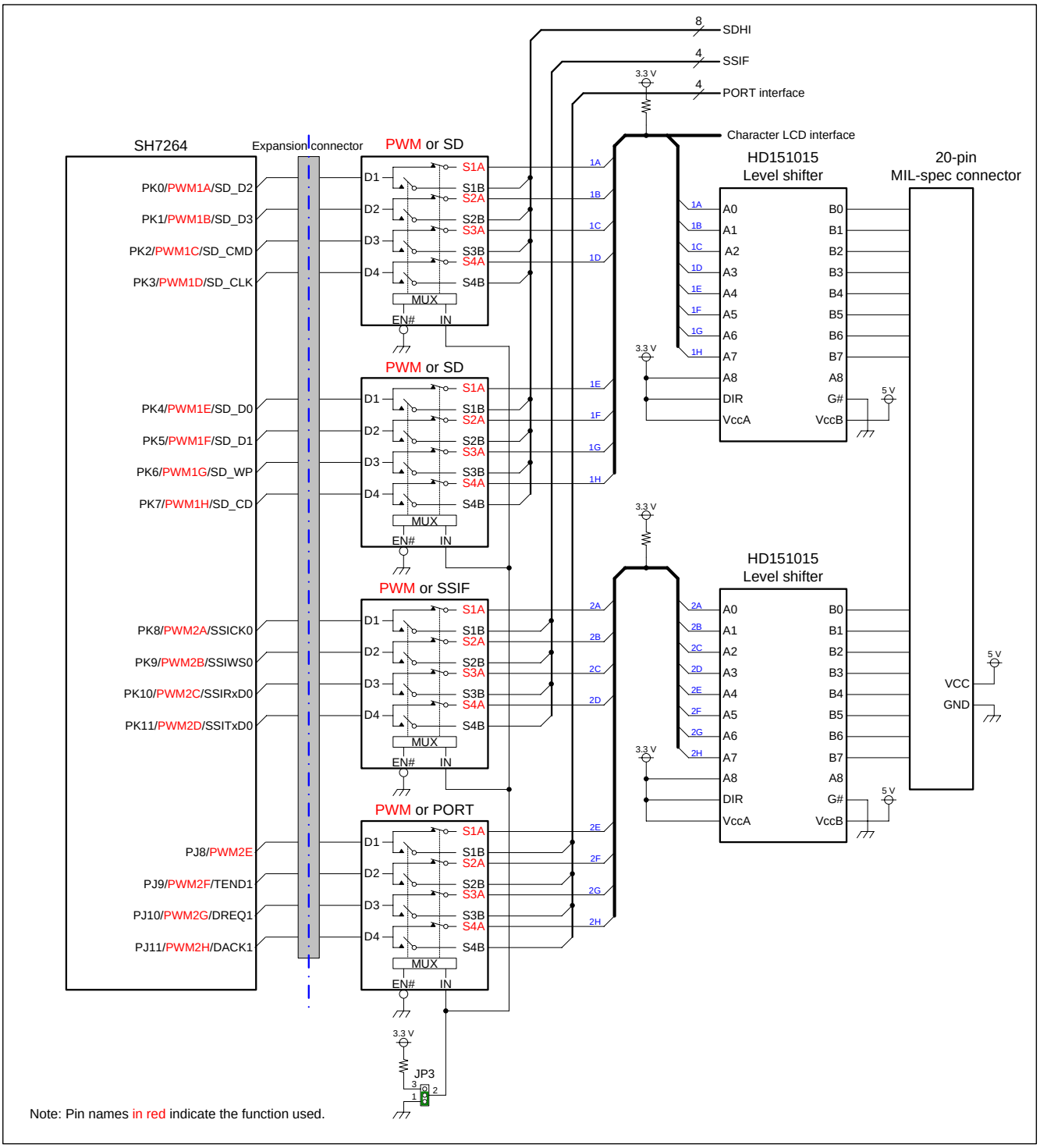


Figure 4.10.1 PWM Interface Block Diagram

Table 4.10.1 Jumper Setting (JP3)

Number	1-2 (Low)	2-3 (High)
JP3	Connected to the PWM interface (default)	Connected to the SDHI/SSIF/PORT interface

4.11 MTU2 Interface

The SH7264 includes a Multi Function Timer Pulse Unit 2 (MTU2) consists of five channels of 16-bit timer counter. LEDs are connected to MTU2 pins to control LED brightness on the M3A-HS64G02. MTU2 pins are also used as SDRAM control pins and RSPI (Renesas Peripheral Interface) channel 0 pin. The figure below shows the MTU2 interface block diagram. The table below lists the DIP switches setting (SW5 on the M3A-HS64).

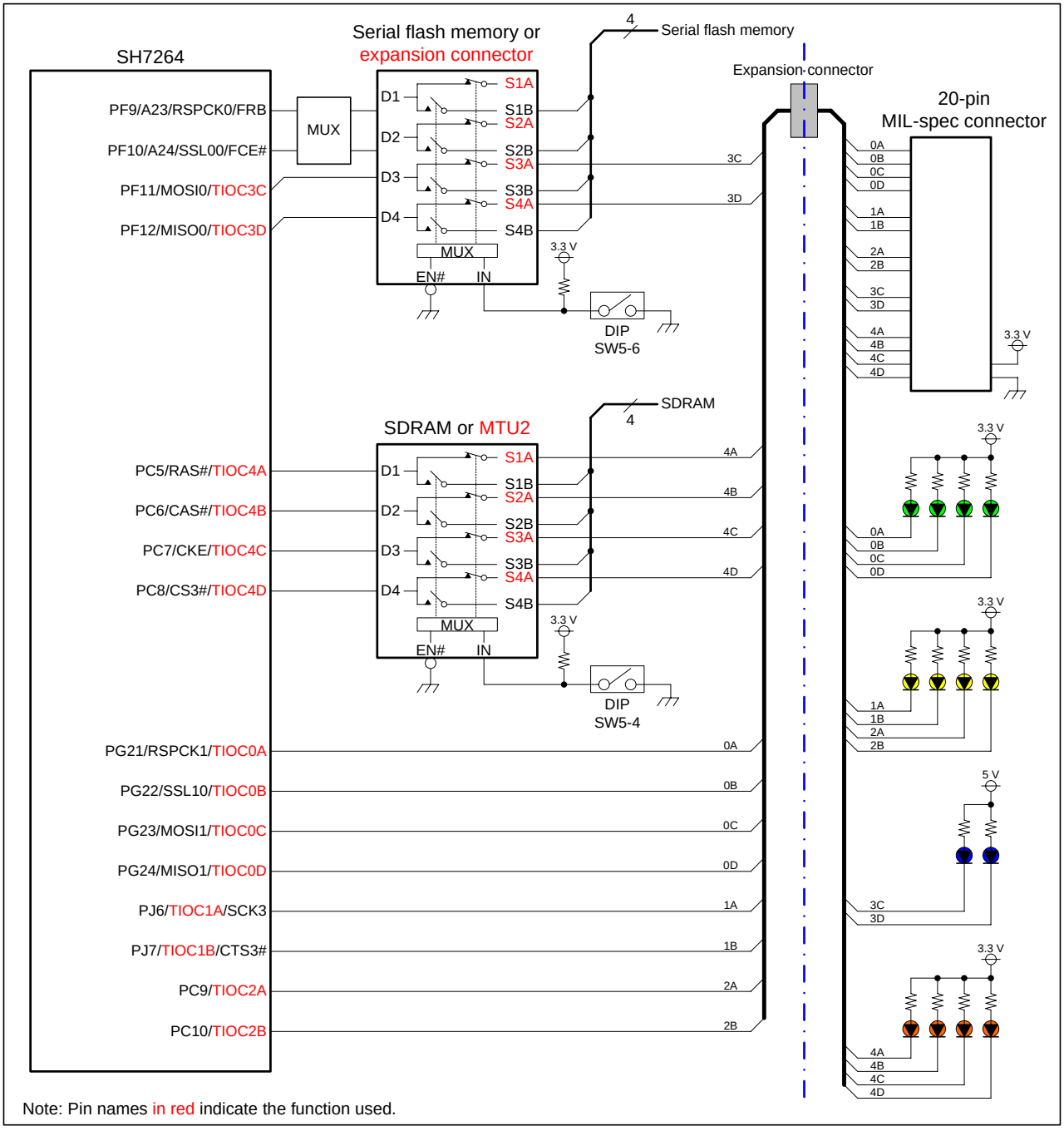


Figure 4.11.1 MTU2 Interface Block Diagram

Table 4.11.1 DIP Switches Setting (SW5)

Number	Function	
	OFF (High)	ON (Low)
SW5-4	Connected to the SDRAM (default)	Connected to the MTU2 interface
SW5-6	Connected to the serial flash memory	Connected to the expansion connector (CD deck/RSPDIF/MTU2 - default)

4.12 I/O Ports

SH7264 I/O ports are connected to switches and LEDs on the M3A-HS64G02.

To use ports PH3 to PH0 as key input switches (4 switches x 4 inputs) via an A/D converter (ADC), sets the ports as analog input pins (AN3 to AN0). Port A can be used as a user interface by setting PB22 pin to high output. The figure below shows the I/O ports block diagram. Table 4.12.1 lists the jumper setting (JP14 on the M3A-HS64). Table 4.12.2 lists the port A function switching.

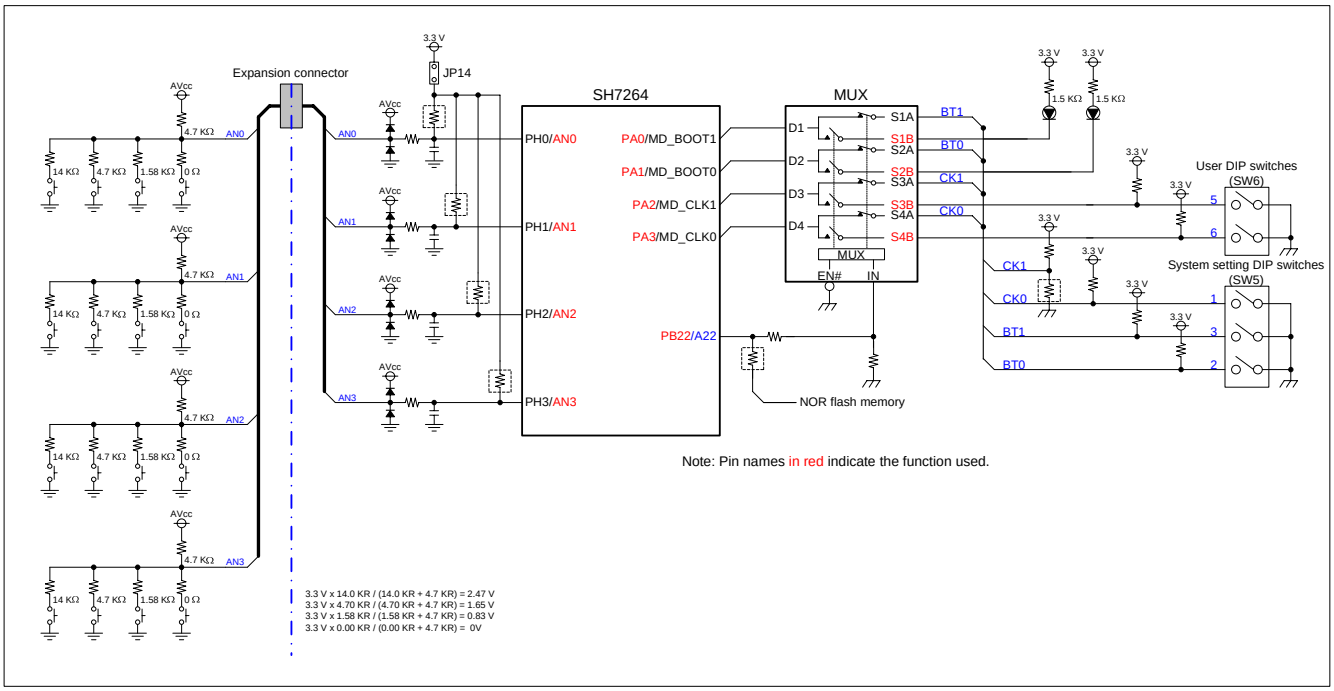


Figure 4.12.1 I/O Ports Block Diagram

Table 4.12.1 Jumper Setting (JP14 on the M3A-HS64)

Number	1-2	None (Open)
JP14	Uses PH[0:3] as an input port (default) (1)	Uses PH[0:3] as an analog input pin

Note 1: When using the PH [0:3] as the input port, mount R10 to R13.

Table 4.12.2 Port A Function Switching

Number	High output	Low output
PB22	Uses Port A as a user interface	Mode sampling (At power-up)

4.13 Interrupt Switches

The M3A-HS64G02 includes two push-button switches (IRQ2 switch and IRQ3 switch) for the IRQ2, and IRQ3 interrupt signals input from the SH7264.

Set JP8, and JP9 on the M3A-HS64, JP1, and JP2 on the M3A-HS64G02 to use these switches.

The figure below shows the interrupt switch block diagram. Table 4.13.1 lists the jumpers setting (JP8, and JP9 on the M3A-HS64). Table 4.13.2 lists the jumpers setting (JP1, and JP2).

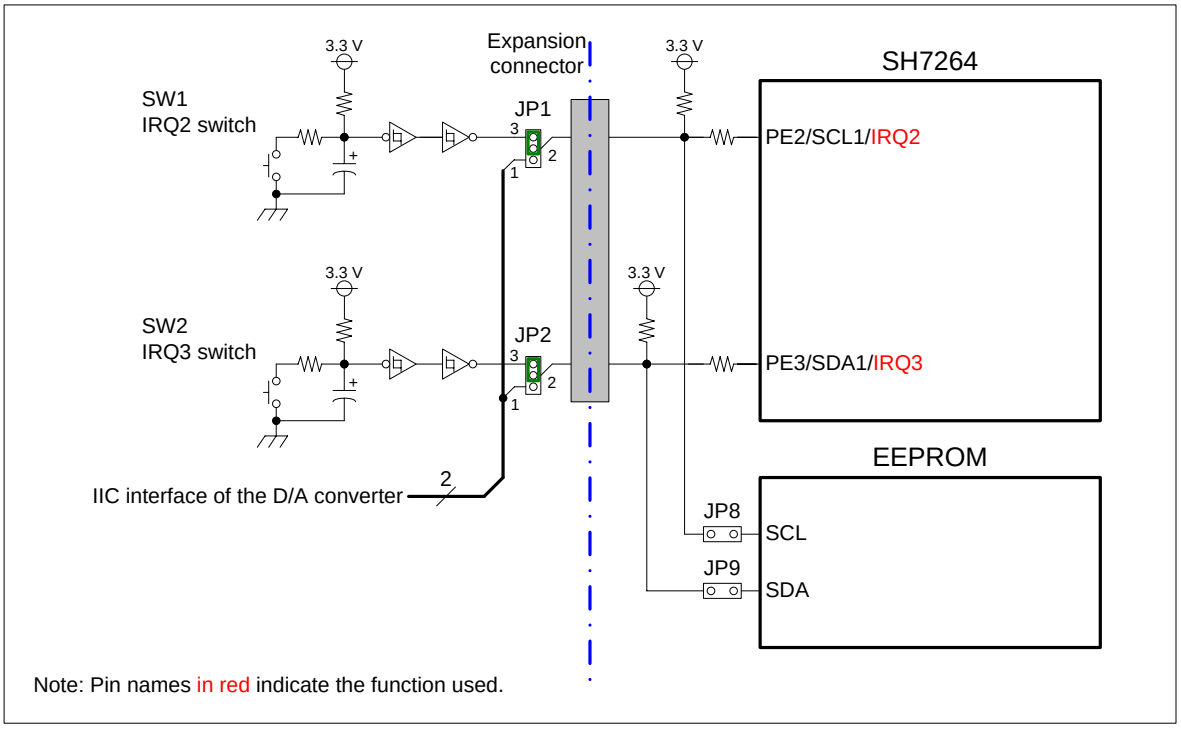


Figure 4.13.1 Interrupt Switch Block Diagram

Table 4.13.1 Jumper Setting (JP8, and JP9 on the M3A-HS64)

Number	1-2	None (Open)
JP8	IIC3 mode (Sets the PE2 as the SCL1 output pin, default)	IRQ mode (Sets the PE2 as the IRQ2 output pin)
JP9	IIC3 mode (Sets the PE3 as the SDA1 output pin, default)	IRQ mode (Sets the PE3 as the IRQ3 output pin)

Table 4.13.2 Jumper Setting (JP1, and JP2)

Number	1-2	2-3
JP1	IIC3 mode (Sets the PE2 as the SCL1 output pin)	IRQ mode (Sets the PE2 as the IRQ2 input pin, default)
JP2	IIC3 mode (Sets the PE3 as the SDA1 I/O pins)	IRQ mode (Sets the PE3 as the IRQ3 input pin, default)

4.14 Clock Modules

Provide following clocks with the SH7264 on the M3A-HS64.

- SH7264 input clock: 18 MHz
- SH7264 RTC clock: 32.768 kHz
- SH7264 audio clock: 12.2880 MHz, and 11.2896 MHz (default)
- SH7264 USB clock: 48.00 MHz
- SH7264 LCD clock : 5.33 MHz

➢ How to select the system clock frequency of AK4353 (D/A converter)

SH7264 audio clock provides either 12.2880 MHz or 11.2896 MHz of the clock frequency with AK4353 by switching jumpers. The figure below shows the clock module block diagram of the M3A-HS64 and M3A-HS64G02. The table below lists the audio clock switching.

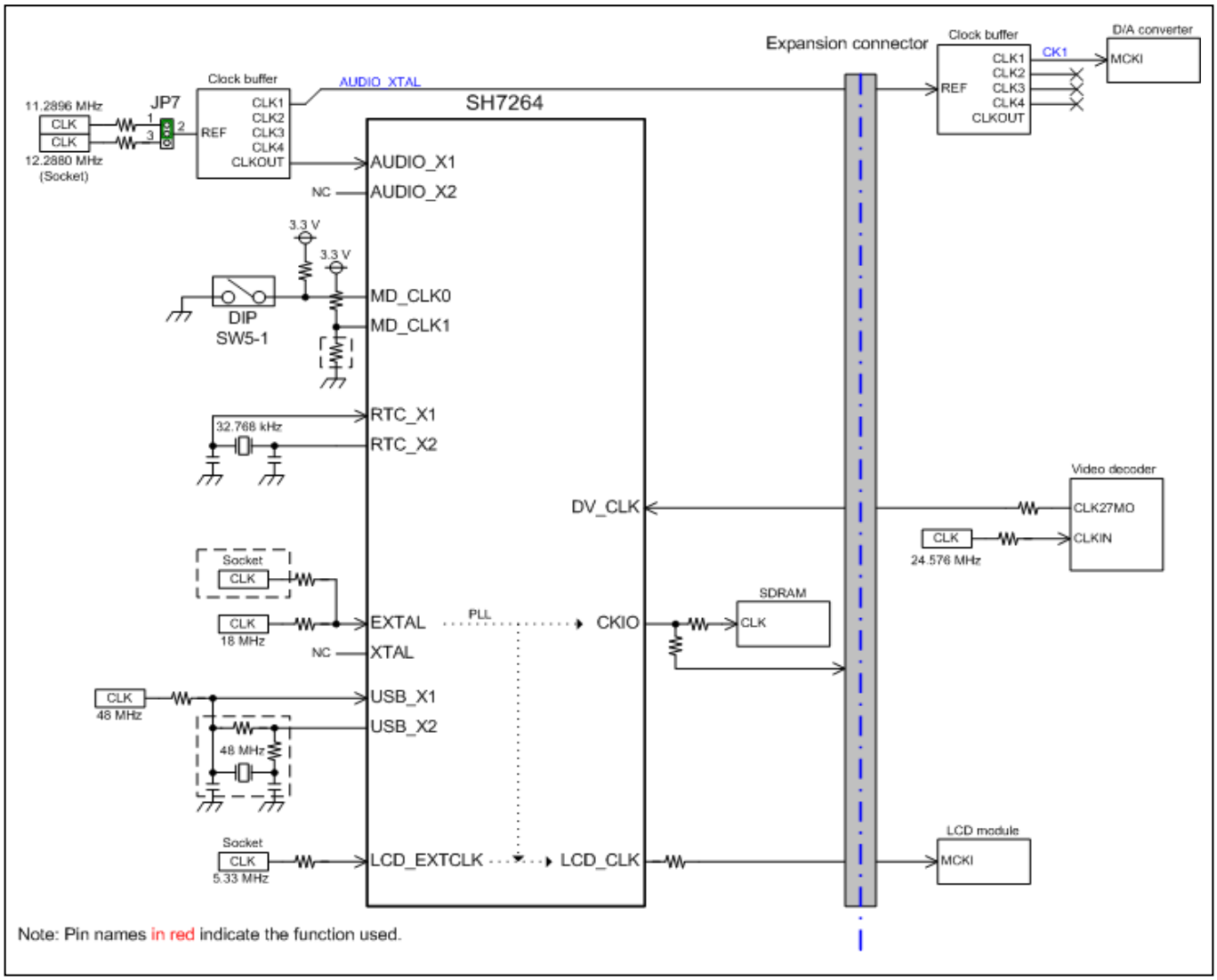


Figure 4.14.1 Clock Module Block Diagram

Table 4.14.1 Audio Clock Switching

Number	1-2	2-3
JP7	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

4.15 Reset Module

A reset IC controls reset signals connected to the SH7264, flash memory and peripheral I/Os on the M3A-HS64 and M3A-HS64G02.

There are two system reset options: power-on reset, and reset by switch. The following figure shows the reset module block diagram.

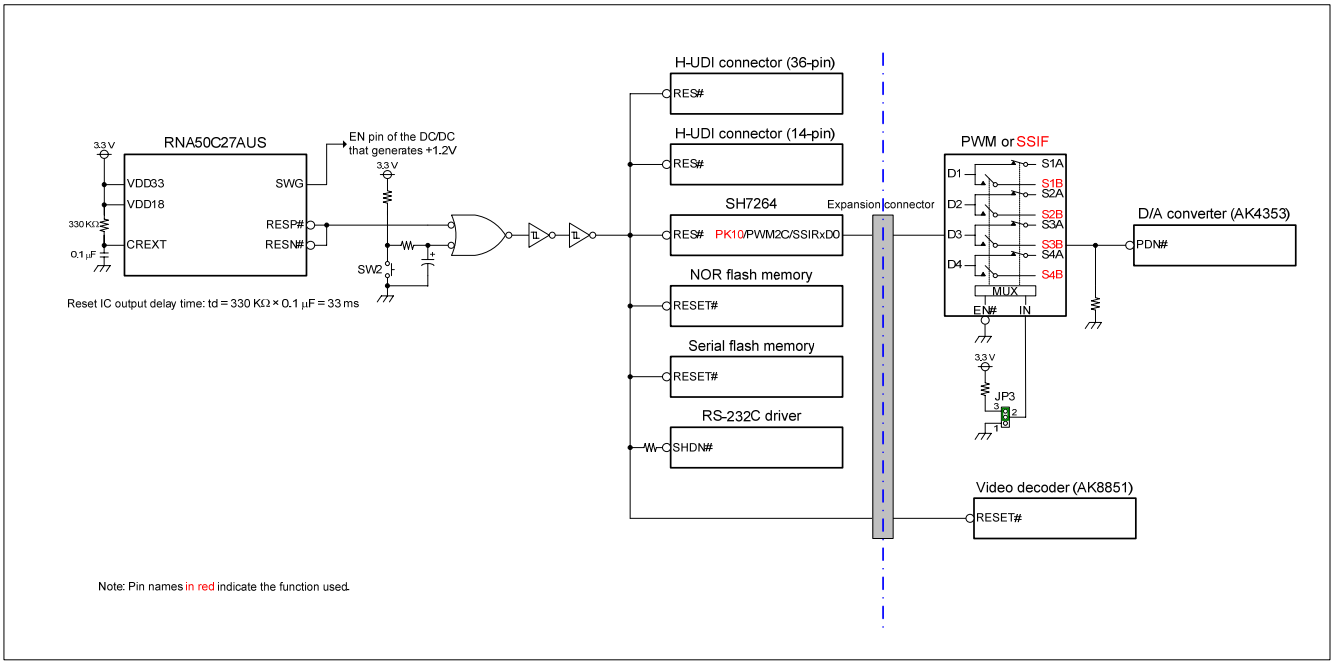


Figure 4.15.1 Reset Module Block Diagram

4.16 Power Supply Module

The M3A-HS64G02 is supplied 12 V power and the voltage regulator on the M3A-HS64G02 generates 8 V, and 5 V voltage. 5 V voltage is supplied to the M3A-HS64, and the voltage regulator on the M3A-HS64 generates digital voltage (3.3 V, 3VCC) and analog voltage (3.3 V, AVcc).

The figure below shows the power supply module block diagram. Refer to 7.2.1 Jumpers (JP1 to JP12) for details on jumpers.

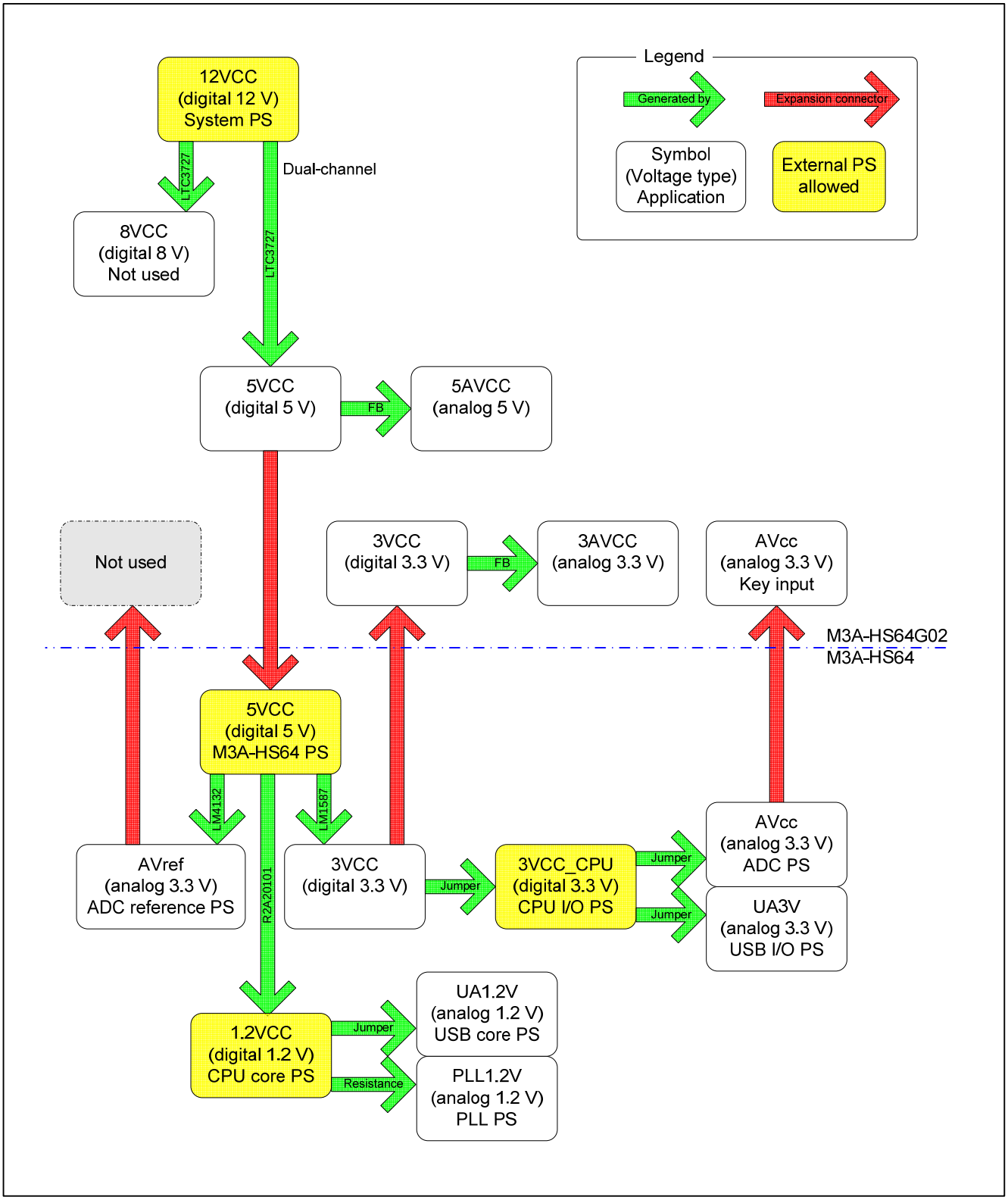


Figure 4.16.1 Power Supply Module Block Diagram

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Chapter 5
M3A-HS64 Operating Specifications

5.1 M3A-HS64 Connectors

Figure 5.1.1 and Figure 5.1.2 show the connector assignments for the M3A-HS64.

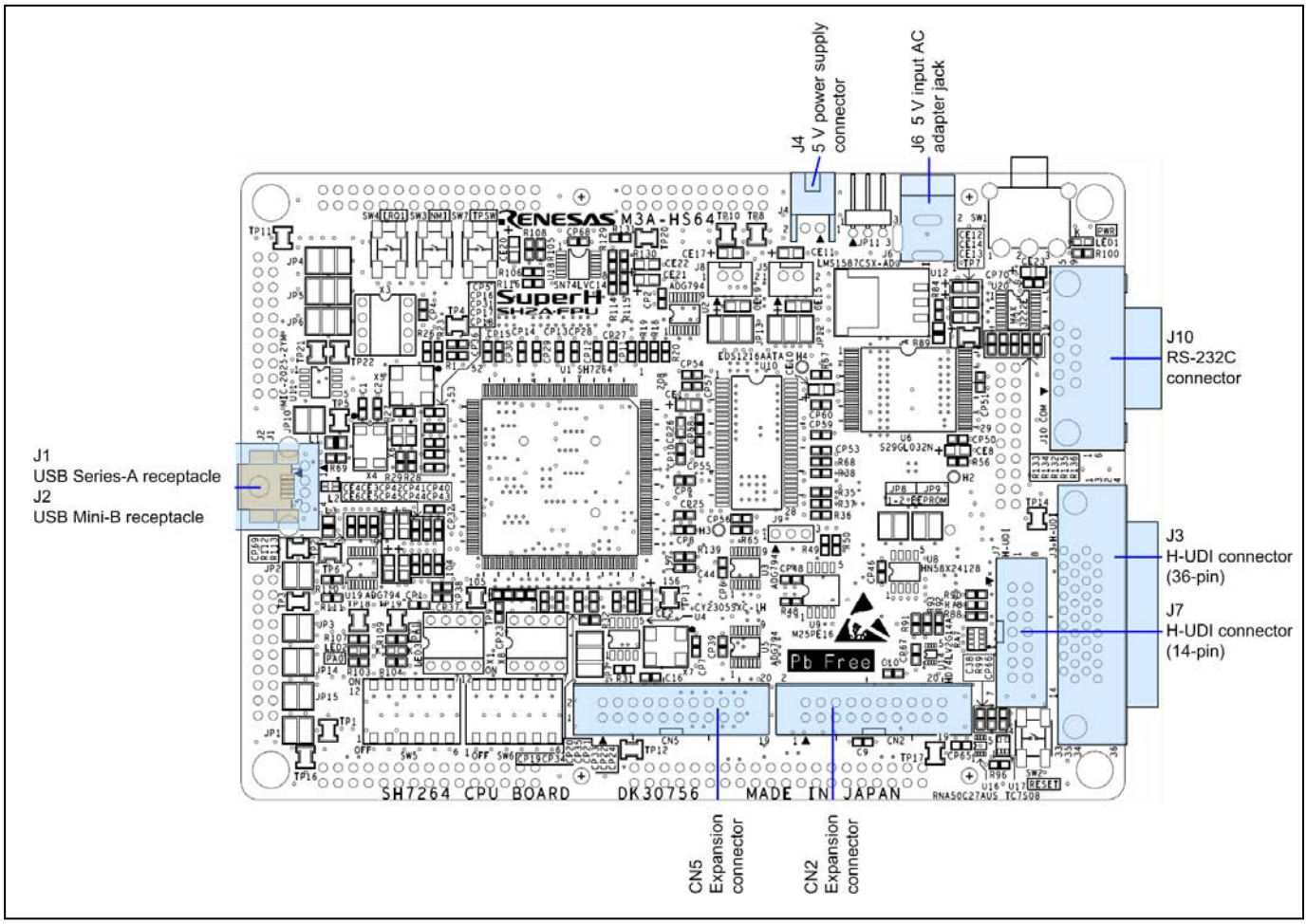


Figure 5.1.1 M3A-HS64 Connectors (Top View of the Component Side)

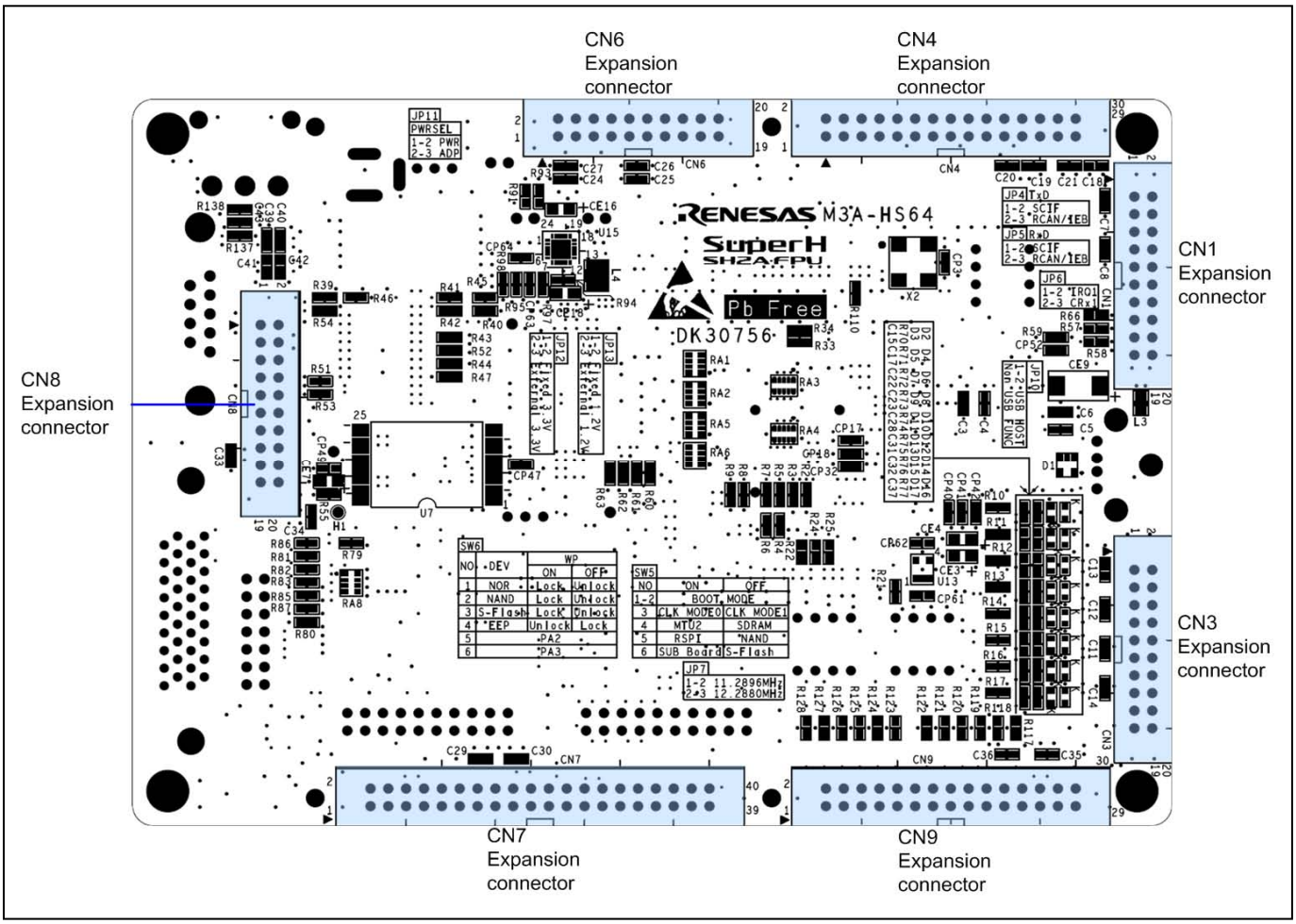


Figure 5.1.2 M3A-HS64 Connectors (Top View of the Solder Side)

5.1.1 USB Connectors (J1 and J2)

The M3A-HS64 includes a USB Series-A receptacle (J1).

Remove the series-A receptacle to connect a USB mini-B receptacle (J2). Refer to Table 1.6.2 in Chapter 1 for the USB mini-B receptacle allowed on the M3A-HS64.

The following figure shows the pin assignments for J1.

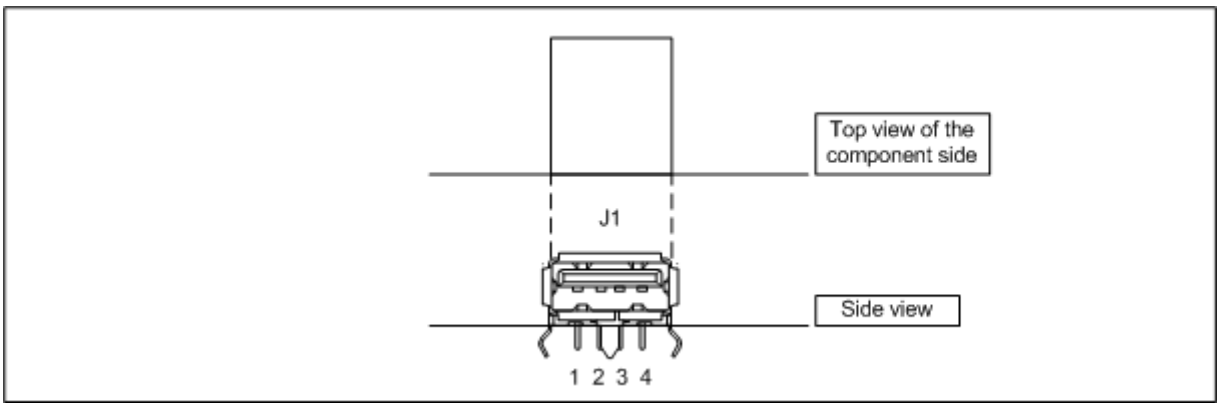


Figure 5.1.3 J1 Pin Assignments

The following figure shows the pin assignments for J2.

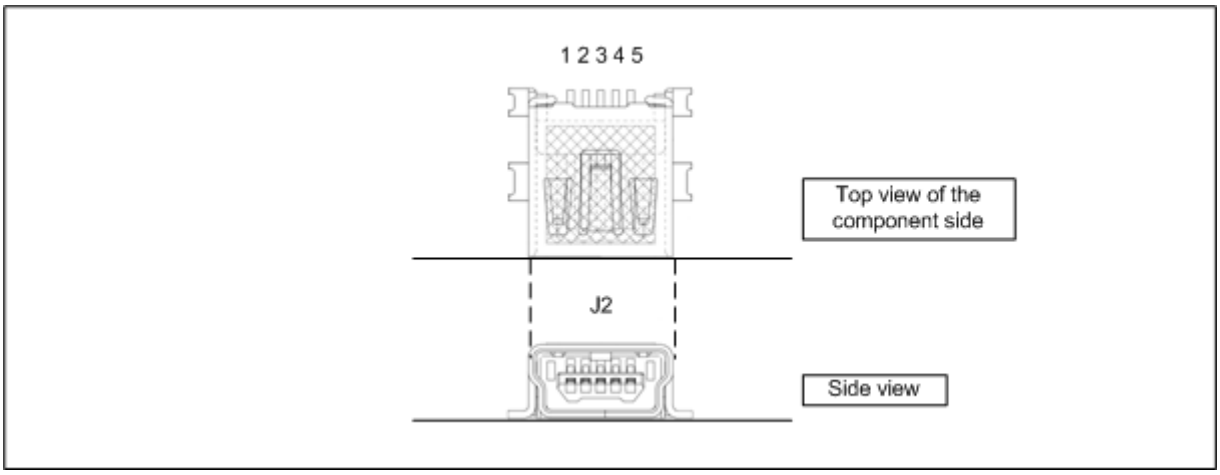


Figure 5.1.4 J2 Pin Assignments

The following table lists the pin descriptions for J1.

Table 5.1.1 J1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	VBUS	3	DP
2	DM	4	GND

The following table lists the pin descriptions for J2.

Table 5.1.2 J2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	VBUS	4	ID (Connected to a test pin)
2	DM	5	GND
3	DP	-	

5.1.2 H-UDI Connector (36-pin, J3)

The M3A-HS64 includes a 36-pin H-UDI connector (J3) to connect the board to an E10A-USB emulator.

The following figure shows the pin assignments for J3.

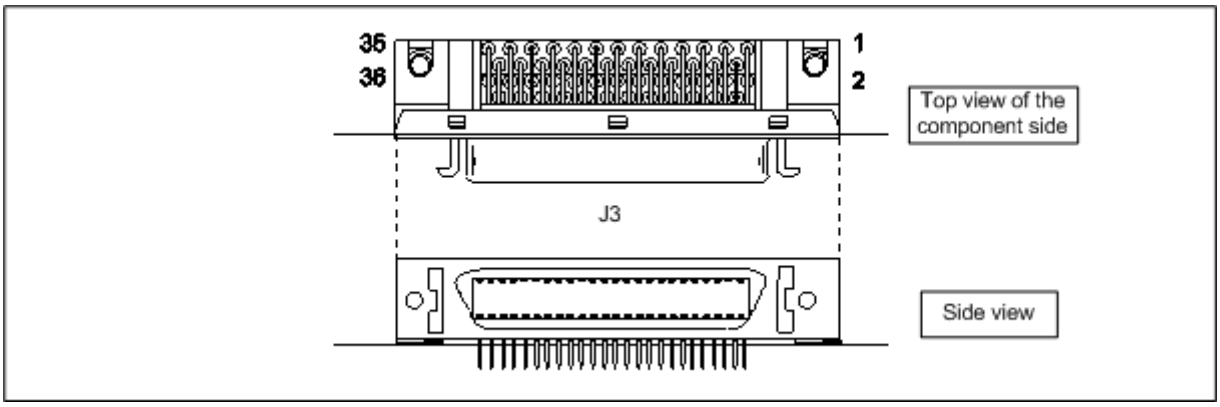


Figure 5.1.5 J3 Pin Assignments

The following table lists the pin descriptions for J3.

Table 5.1.3 J3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AUDCK	19	TMS
2	GND	20	GND
3	AUDATA0	21	TRST#
4	GND	22	ASEMD#
5	AUDATA1	23	TDI
6	GND	24	GND
7	AUDATA2	25	TDO
8	GND	26	GND
9	AUDATA3	27	ASEBRKAK#/ASEBRK#
10	GND	28	GND
11	AUDSYNC#	29	3.3 V
12	GND	30	GND
13	NC	31	RESET#
14	GND	32	GND
15	NC	33	GND
16	GND	34	GND
17	TCK	35	NC
18	GND	36	GND

5.1.3 5 V Power Supply Connector (J4)

The M3A-HS64 includes a system power supply connector.

The following figure shows the pin assignments for J4.

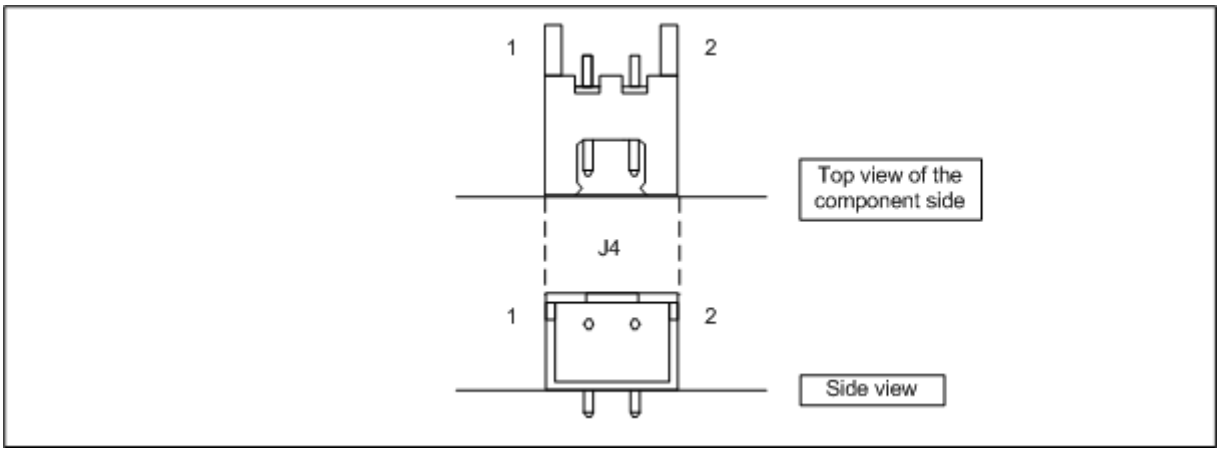


Figure 5.1.6 J4 Pin Assignments

The following table lists the pin descriptions for J4.

Table 5.1.4 J4 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	2	GND

5.1.4 5 V Input AC Adapter Jack (J6)

The M3A-HS64 includes an AC adapter jack (J6) for 5 V DC input.

The following figure shows the pin assignments for J6.

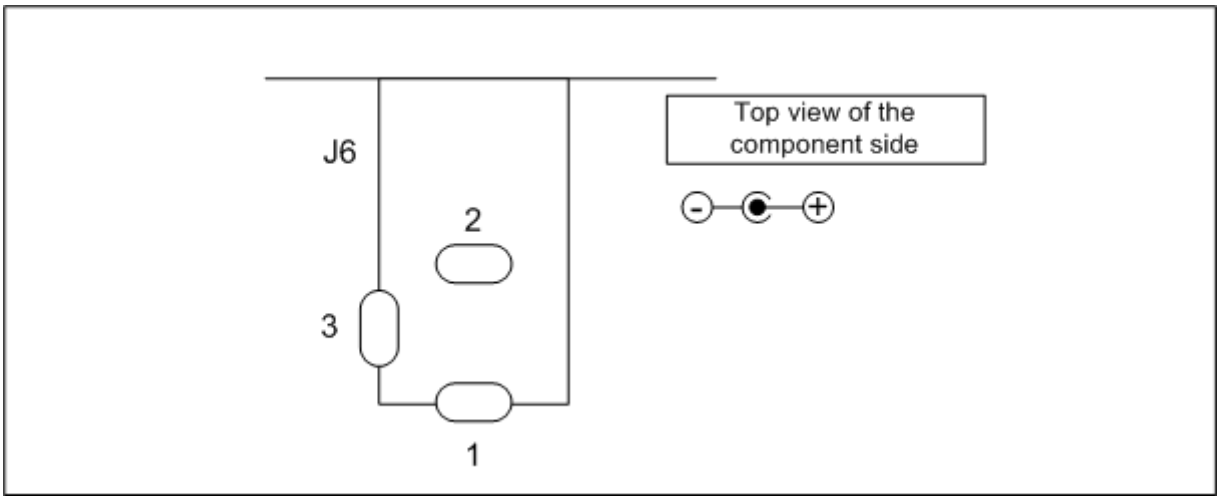


Figure 5.1.7 J6 Pin Assignments

The following table lists the pin descriptions for J6.

Table 5.1.5 J6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	2	GND
3	GND	-	

5.1.5 H-UDI Connector (14-pin, J7)

The M3A-HS64 includes a 14-pin H-UDI connector (J7) to connect the board to an E10A-USB emulator.

The following figure shows the pin assignments for J7.

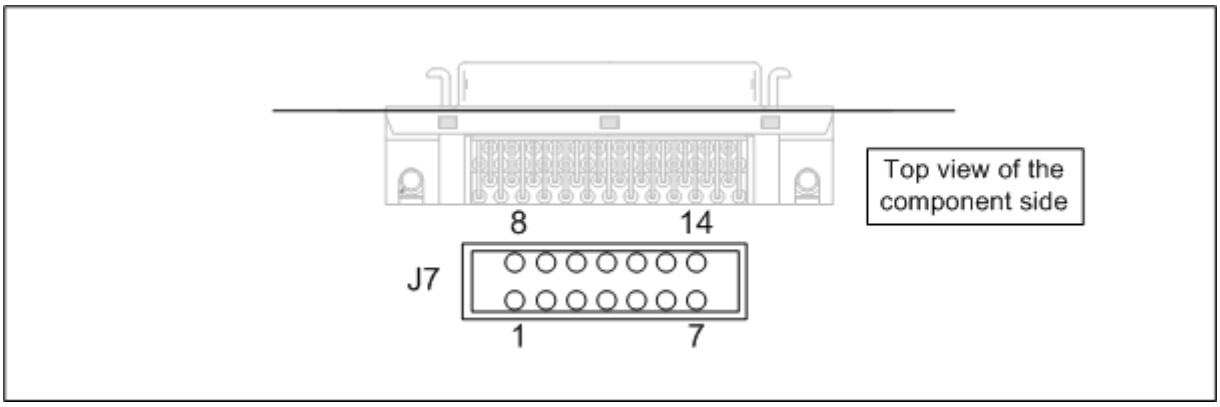


Figure 5.1.8 J7 Pin Assignments

The following table lists the pin descriptions for J7.

Table 5.1.6 J7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	TCK	8	NC
2	TRST#	9	ASEMD#
3	TDO	10	GND
4	ASEBRKAK#/ASEBRK#	11	3.3 V
5	TMS	12	GND
6	TDI	13	GND
7	RESET#	14	GND

5.1.6 RS-232C Connector (J10)

The M3A-HS64 includes an RS-232C connector (J10).

The following figure shows the pin assignments for J10.

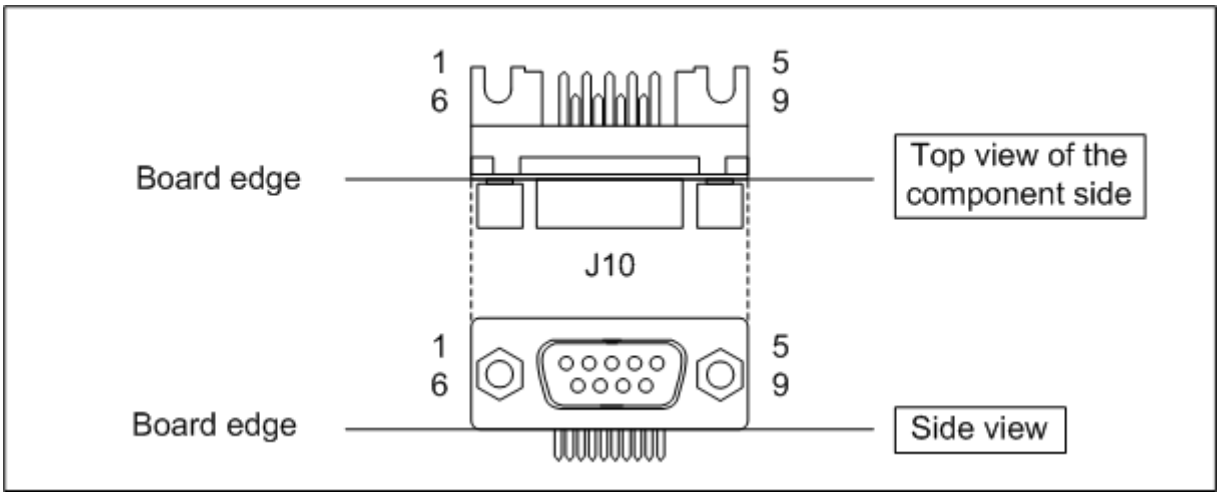


Figure 5.1.9 J10 Pin Assignments

The following table lists the pin descriptions for J10.

Table 5.1.7 J10 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	6	DSR#
2	RXD (PJ1/CRx0/IERxD/IRQ0/RxD0)	7	RTS#
3	TXD (PJ0/CTx0/IETxD/CS1#/TxD0/A0)	8	CTS#
4	DTR#	9	NC
5	GND	-	

Pins 4 to 6 and 7 to 8 are loopback-connected.

5.1.7 Expansion Connectors (CN1 to CN9)

The M3A-HS64 includes through-holes for mounting expansion connectors (CN1 to CN9).

The following figure shows the pin assignments for expansion connectors.

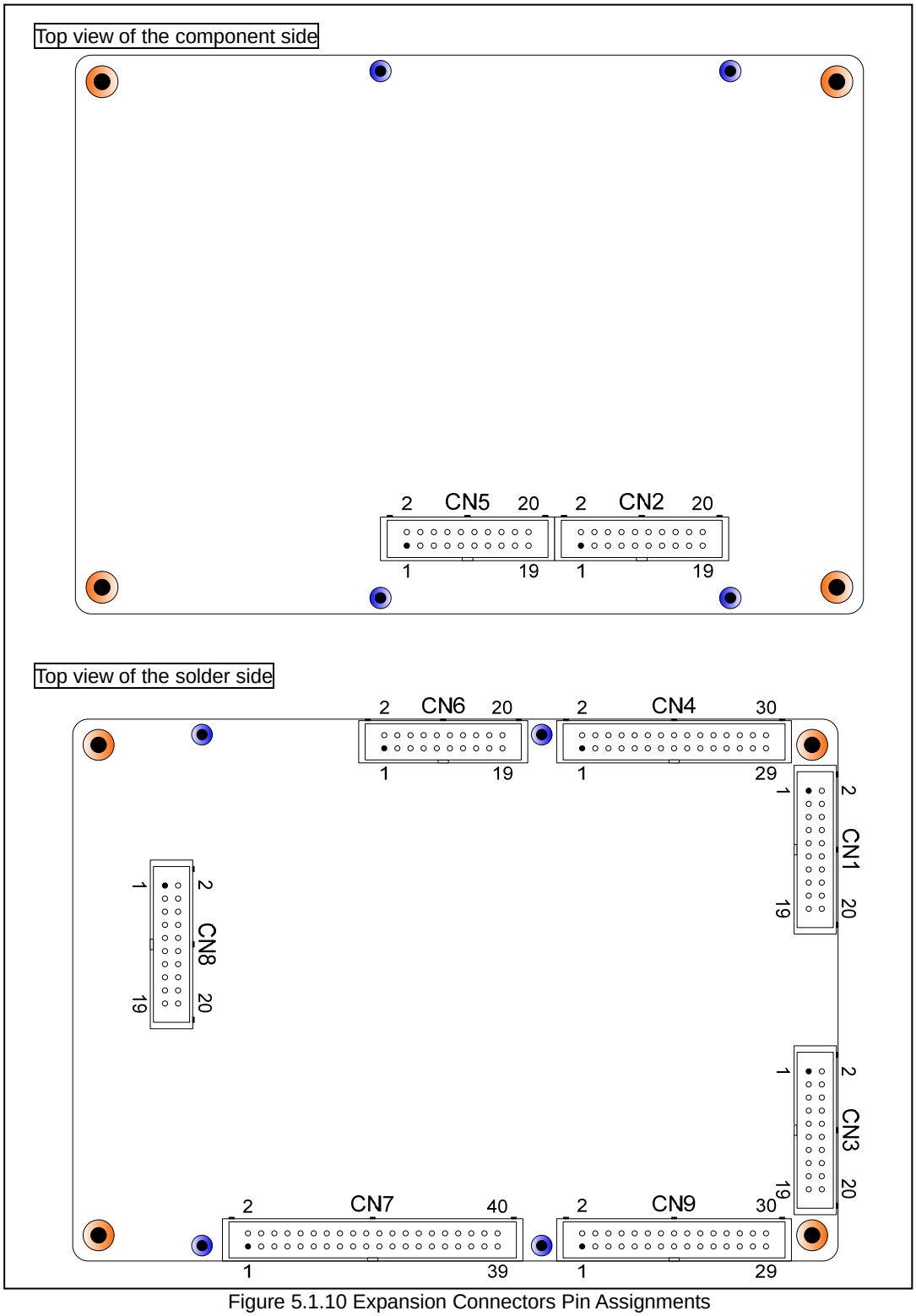


Figure 5.1.10 Expansion Connectors Pin Assignments

The following table lists the pin descriptions for CN1.

Table 5.1.8 CN1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PJ11/PWM2H/DACK1	2	PJ10/PWM2G/DREQ1
3	5 V	4	PJ9/PWM2F/TEND1
5	PJ8/PWM2E/RTS3#	6	3.3 V
7	PA3/MD_CLK0	8	PA2/MD_CLK1
9	PA1/MD_BOOT0	10	PA0/MD_BOOT1
11	GND	12	PJ7/TIOC1B/CTS3#
13	PJ6/TIOC1A/SCK3	14	PJ5/IERxD/TxD3
15	PJ4/IETxD/RxD3	16	GND
17	PJ3/CRx1/CRx0&CRx1/IRQ1	18	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP
19	PJ1/CRx0/IERxD/IRQ0/RxD0	20	PJ0/CTx0/IETxD/CS1#/TxD0/A0

The following table lists the pin descriptions for CN2.

Table 5.1.9 CN2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	GND
3	PK7/PWM1H/SD_CD	4	PK6/PWM1G/SD_WP
5	PK5/PWM1F/SD_D1	6	PK4/PWM1E/SD_D0
7	3.3 V	8	PE5/SDA2/DV_HSYNC
9	PE4/SCL2/DV_VSYNC	10	PE3/SDA1/IRQ3
11	PE2/SCL1/IRQ2	12	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#
13	PE0/SCL0/AUDIO_CLK/IRQ0	14	5 V
15	PK3/PWM1D/SD_CLK	16	PK2/PWM1C/SD_CMD
17	PK1/PWM1B/SD_D3	18	PK0/PWM1A/SD_D2
19	GND	20	GND

The following table lists the pin descriptions for CN3.

Table 5.1.10 CN3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AVref	2	AVref
3	PH1/AN1	4	PH0/AN0
5	AVref	6	AVref
7	PH3/AN3	8	PH2/AN2
9	AVcc	10	AVcc
11	PH5/AN5	12	PH4/AN4
13	AVcc	14	AVcc
15	PH7/AN7	16	PH6/AN6
17	AVss	18	AVss
19	AVss	20	AVss

The following table lists the pin descriptions for CN4.

Table 5.1.11 Pin Descriptions (CN4)

Pin Number	Signal Name	Pin Number	Signal Name
1	PB1/A1	2	PB2/A2
3	PB3/A3	4	PB4/A4/TIOC0A
5	PB5/A5/TIOC0B	6	PB6/A6/TIOC0C
7	GND	8	GND
9	PB7/A7/TIOC0D	10	PB8/A8/TIOC1A
11	PB9/A9/TIOC1B	12	PB10/A10/TIOC2A
13	PB11/A11/TIOC2B	14	PB12/A12/TIOC3A
15	GND	16	GND
17	PB13/A13/TIOC3B	18	PB14/A14/TIOC3C
19	PB15/A15/TIOC3D	20	PB16/A16/TIOC4A
21	PB17/A17/TIOC4B	22	PB18/A18/TIOC4C
23	3.3 V	24	3.3 V
25	PB19/A19/TIOC4D	26	PB20/A20
27	PB21/A21	28	PB22/A22/CS4#
29	5 V	30	5 V

The following table lists the pin descriptions for CN5.

Table 5.1.12 CN5 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PK11/PWM2D/SSITxD0	2	PK10/PWM2C/SSIRxD0
3	PK9/PWM2B/SSIWS0	4	PK8/PWM2A/SSISCK0
5	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT	6	5 V
7	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN	8	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
9	GND	10	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
11	PF8/CE2B#/SSIDATA3/DV_CLK	12	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
13	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/ TCLKB	14	GND
15	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5/ TCLKC/AUDATA3	16	PF4/ICIOWR#/AH#/SSIWS2/DV_DATA4/ TxD3/AUDATA2
17	PF3/ICIORD#/SSISCK2/DV_DATA3/RxD3/ AUDATA1	18	PF2/BACK#/SSIDATA1/DV_DATA2/TxD2/ DACK0/AUDATA0
19	PF1/BREQ#/SSIWS1/DV_DATA1/RxD2/ DREQ0/AUDSYNC#	20	PF0/WAIT#/SSISCK1/DV_DATA0/SCK2/ TEND0/AUDCK

The following table lists the pin descriptions for CN6.

Table 5.1.13 CN6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	2	5 V
3	5 V	4	5 V
5	PC0/CS0#	6	PC1/RD#
7	PC2/RDWR#	8	PC3/WE0#/DQML
9	PC4/WE1#/DQMU/WE#	10	3.3V
11	3.3V	12	PC9/TIOC2A
13	PC10/TIOC2B	14	PC5/RAS#/TIOC4A/IRQ4
15	PC6/CAS#/TIOC4B/IRQ5	16	PC7/CKE/TIOC4C/IRQ6
17	PC8/CS3#/TIOC4D/IRQ6	18	GND
19	GND	20	CKIO

The following table lists the pin descriptions for CN7.

Table 5.1.14 CN7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PK1/PWM1B/SD_D3	2	PK0/PWM1A/SD_D2
3	PK3/PWM1D/SD_CLK	4	PK2/PWM1C/SD_CMD
5	PE0/SCL0/AUDIO_CLK/IRQ0	6	RES#
7	PE2/SCL1/IRQ2	8	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#
9	PE4/SCL2/DV_VSYNC	10	PE3/SDA1/IRQ3
11	3.3 V	12	PE5/SDA2/DV_HSYNC
13	PK5/PWM1F/SD_D1	14	PK4/PWM1E/SD_D0
15	PK7/PWM1H/SD_CD	16	PK6/PWM1G/SD_WP
17	PF0/WAIT#/SSISCK1/DV_DATA0/SCK2/ TEND0/AUDCK	18	5 V
19	PF2/BACK#/SSIDATA1/DV_DATA2/TxD2/ DACK0/AUDATA0	20	PF1/BREQ#/SSIWS1/DV_DATA1/RxD2/ DREQ0/AUDSYNC#
21	GND	22	PF3/ICIORD#/SSISCK2/DV_DATA3/RxD3/ AUDATA1
23	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5/ TCLKC/AUDATA3	24	PF4/ICIOWR#/AH#/SSIWS2/DV_DATA4/ TxD3/AUDATA2
25	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/ TCLKB	26	GND
27	PF8/CE2B#/SSIDATA3/DV_CLK	28	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
29	GND	30	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
31	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN	32	PF10/A24/SSIWS3/SSL0/TIOC3B/FCE#
33	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT	34	GND
35	PK9/PWM2B/SSIWS0	36	PK8/PWM2A/SSISCK0
37	PK11/PWM2D/SSITxD0	38	PK10/PWM2C/SSIRxD0
39	GND	40	AUDIO_XTAL

The following table lists the pin descriptions for CN8.

Table 5.1.15 CN8 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PD15/D15/NAF7/PWM2H	2	PD7/D7/FWE#/PWM1H
3	PD14/D14/NAF6/PWM2G	4	PD6/D6/FALE/PWM1G
5	GND	6	PD13/D13/NAF5/PWM2F
7	PD5/D5/FCLE/PWM1F	8	PD12/D12/NAF4/PWM2E
9	PD4/D4/FRE#/PWM1E	10	GND
11	PD11/D11/NAF3/PWM2D	12	PD3/D3/PWM1D
13	PD10/D10/NAF2/PWM2C	14	PD2/D2/PWM1C
15	3.3 V	16	PD9/D9/NAF1/PWM2B
17	PD1/D1/PWM1B	18	PD8/D8/NAF0/PWM2A
19	PD0/D0/PWM1A	20	5 V

The following table lists the pin descriptions for CN9.

Table 5.1.16 CN9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PG1/LCD_DATA1/SD_D3/PINT1	2	PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#
3	PG3/LCD_DATA3/SD_CLK/PINT3	4	PG2/LCD_DATA2/SD_CMD/PINT2
5	GND	6	PG4/LCD_DATA4/SD_D0/PINT4
7	PG6/LCD_DATA6/SD_WP/PINT6	8	PG5/LCD_DATA5/SD_D1/PINT5
9	PG7/LCD_DATA7/SD_CD/PINT7	10	GND
11	PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC	12	PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK
13	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/ SIOFTxD	14	PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/ SIOFRxD
15	GND	16	PG12/LCD_DATA12/TIOC0A/RxD1
17	PG14/LCD_DATA14/TIOC0C/SCK1	18	PG13/LCD_DATA13/TIOC0B/TxD1
19	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#	20	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
21	PG17/LCD_HSYNC/TIOC1B/RSPCK1/ RxD6	22	5 V
23	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7	24	PG18/LCD_DE/TIOC2A/SSL1/TxD6
25	3.3 V	26	PG20/LCD_EXTCLK/MISO1/TxD7
27	PG22/SSL1/TIOC0B	28	PG21/RSPCK1/TIOC0A
29	PG24/MISO1/TIOC0D	30	PG23/MOSI1/TIOC0C

5.2 M3A-HS64 Operating Components

The following figure shows the assignments of the M3A-HS64 operating components.

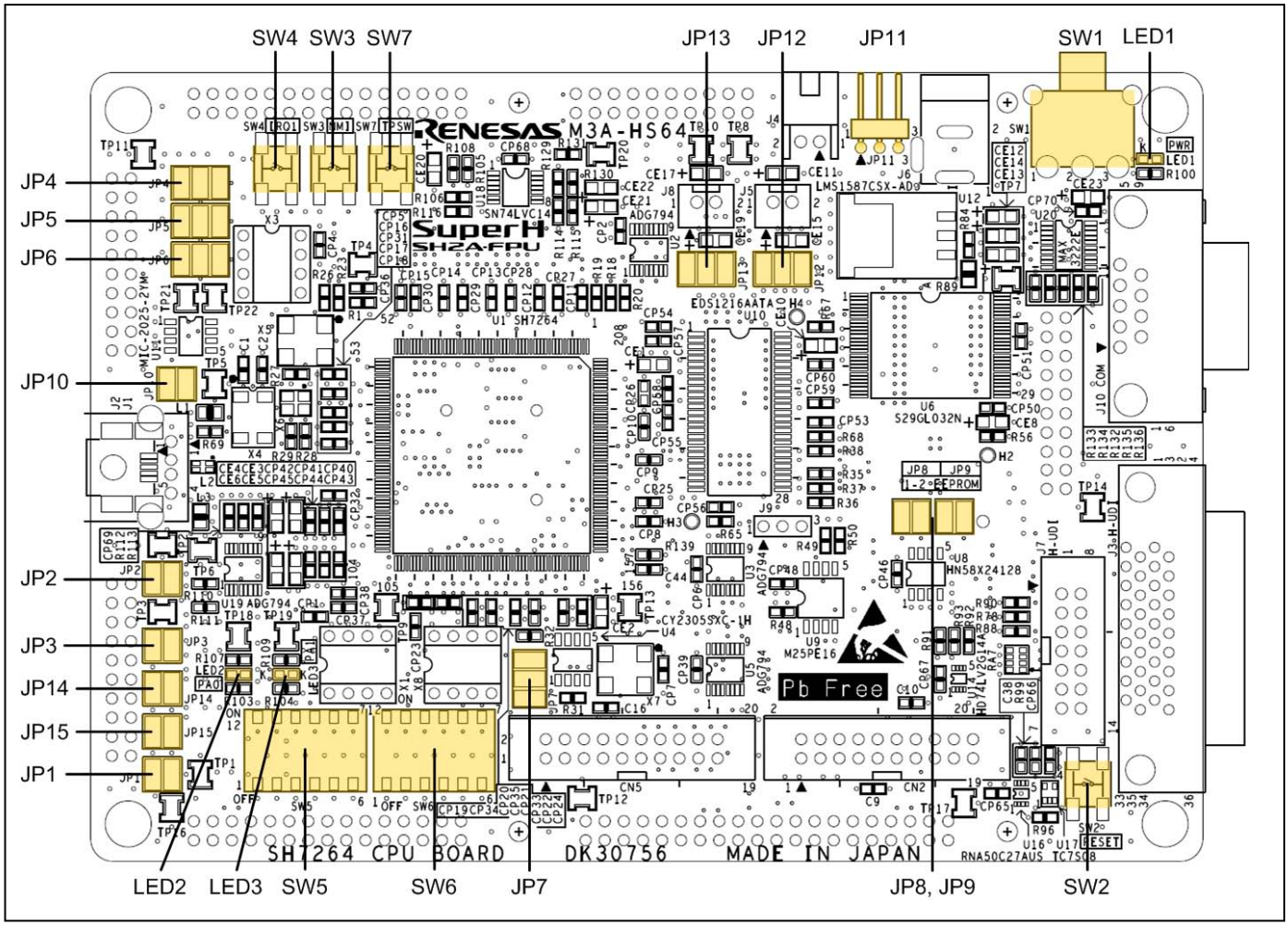


Figure 5.2.1 M3A-HS64 Operating Component Assignments

5.2.1 Jumpers (JP1 to JP15)

The M3A-HS64 includes 15 jumpers.

The figure below shows jumper assignments (JP1 to JP15) on the M3A-HS64.

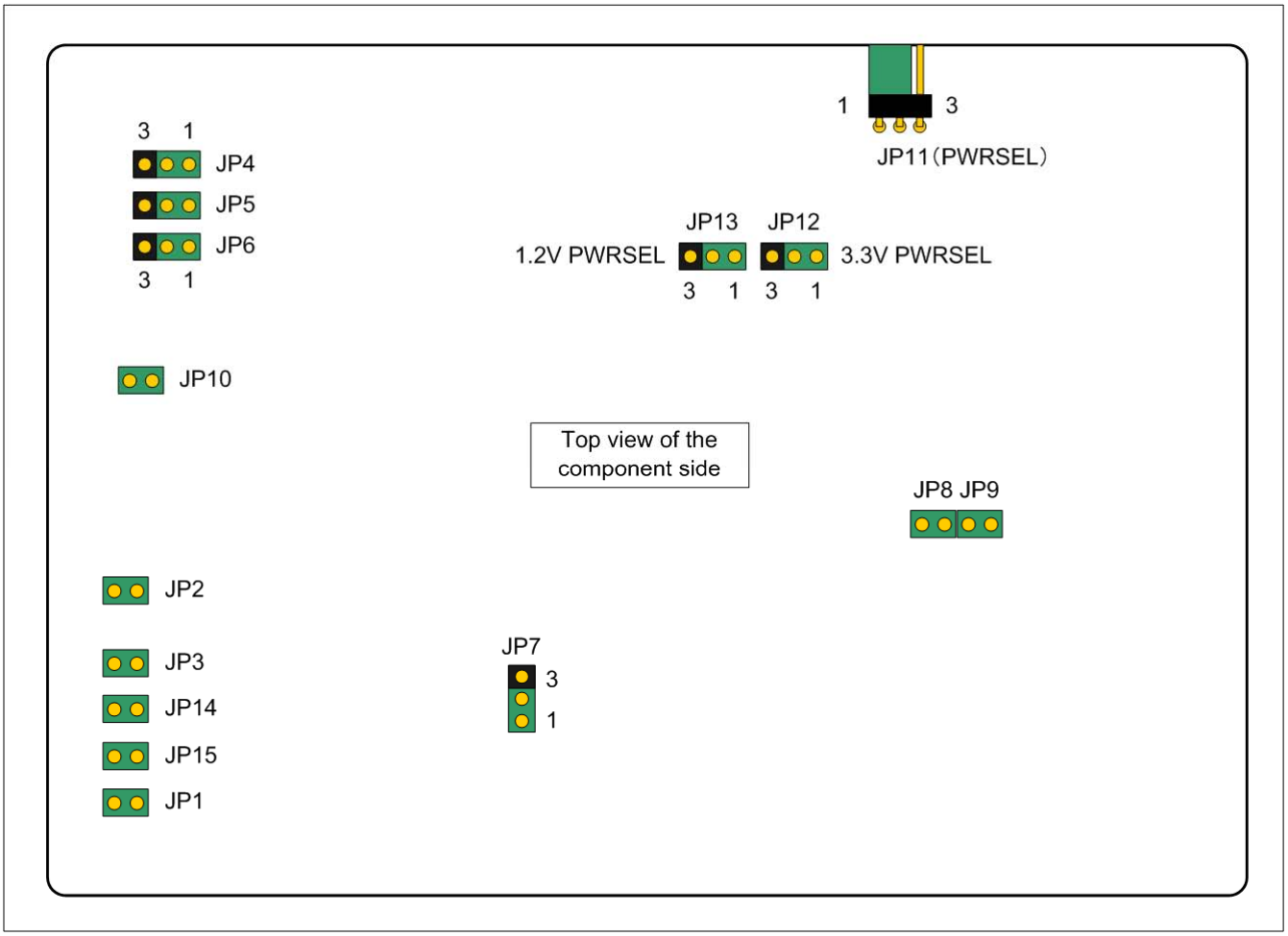


Figure 5.2.2 M3A-HS64 Jumper Assignments (JP1 to JP15)

The following table lists jumpers settings (JP1 to JP3).

Table 5.2.1 Analog Power Supply Jumpers Setting (JP1 to JP3)

Number	Setting	Description
JP1	1 - 2	Supplies 3.3 V analog power for the A/D converter (AVcc)
	Open	Does not supply 3.3 V analog power for the A/D converter (AVcc)
JP2	1 - 2	Supplies 3.3 V analog power for USB (USBAPVcc)
	Open	Does not supply 3.3 V analog power for USB (USBAPVcc)
JP3	1 - 2	Supplies 1.2 V analog power for USB (USBAVcc)
	Open	Does not supply 1.2 V analog power for USB (USBAVcc)

Notes:

1. The shaded row shows the default setting.
2. Do not change the jumper settings while the M3A-HS64 is ON. Be sure to turn the power OFF before changing the settings.

Table 5.2.2 Multiplexed Pin Switch Jumpers Setting (JP4 to JP6, JP8, and JP9)

Number	Setting	Description
JP4 TxD0/CTx0/IETxD	1 - 2	Connects the RS-232C driver (U20) as the TxD0 OUT pin
	2 - 3	Connects the expansion connector (CN1) as the CTx0/IETxD OUT pin
JP5 RxD0/CRx0/IERxD	1 - 2	Connects the RS-232C driver (U20) as the RxD0 IN pin
	2 - 3	Connects the expansion connector (CN1) as the CRx0/IERxD IN pin
JP6 IRQ1/CRx1	1 - 2	Connects IRQ1 switch (SW4) as the IRQ1 IN pin
	2 - 3	Connects the expansion connector (CN1) as the CRx1 IN pin
JP8 SCL1/IRQ2	1 - 2	Connects the EEPROM (U8) as the SCL1 OUT pin
	Open	Connects the expansion connector (CN7) as the IRQ2 IN pin
JP9 SDA1/IRQ3	1 - 2	Connects the EEPROM (U8) as the SDA1 I/O pin
	Open	Connects the expansion connector (CN7) as the IRQ3 IN pin

Table 5.2.3 AUDIO_X1 Frequency Switch Jumper Setting (JP7)

Number	Setting	Description
JP7	1 - 2	Inputs the clock of 11.2896 MHz to AUDIO_X1 pin
	2 - 3	Inputs the clock of 12.2880 MHz to AUDIO_X1 pin

Table 5.2.4 USB VBUS Power Supply Jumper Setting (JP10)

Number	Setting	Description
JP10	1 - 2	USB host mode (Supplies the power to VBUS)
	Open	USB function mode (Does not supply the power to VBUS)

Table 5.2.5 Power Supply Switch Jumper Setting (JP11 to JP13)

Number	Setting	Description
JP11 PWRSEL	1 - 2	Supplies the system power from J4
	2 - 3	Supplies the system power from J6 (AC adapter is used)
JP12 3.3V PWRSEL	1 - 2	Supplies 3.3 V power for the SH7264 from U12 (Internal power supply)
	2 - 3	Supplies 3.3 V power for the SH7264 from J5 (External power supply)
JP13 1.2V PWRSEL	1 - 2	Supplies 1.2 V power for the SH7264 from U15 (Internal power supply)
	2 - 3	Supplies 1.2 V power for the SH7264 from J8 (External power supply)

Table 5.2.6 Pin Pull up Jumpers Setting (JP14, JP15)

Number	Setting	Description
JP14 PH/AN[0:3]	1 - 2	Pulls up PN/AN[0:3] pin (1)
	None (Open)	Does not pull up PH/AN[0:3] pin
JP15 PH/AN[4:7]	1 - 2	Pulls up PH/AN[4:7] pin
	None (Open)	Does not pull up PH/AN[4:7] pin

Note:

1. Mount the resistors (R10 to R13) when using this setting.
2. The shaded row shows the default setting.
3. Do not change the jumper settings while the M3A-HS64 is ON. Be sure to turn the power OFF before changing the settings.

5.2.2 Switches and LEDs

The M3A-HS64 includes seven switches and three LEDs.

The figure below shows the assignments of switches and LEDs. Table 5.2.10 lists LEDs on the M3A-HS64.

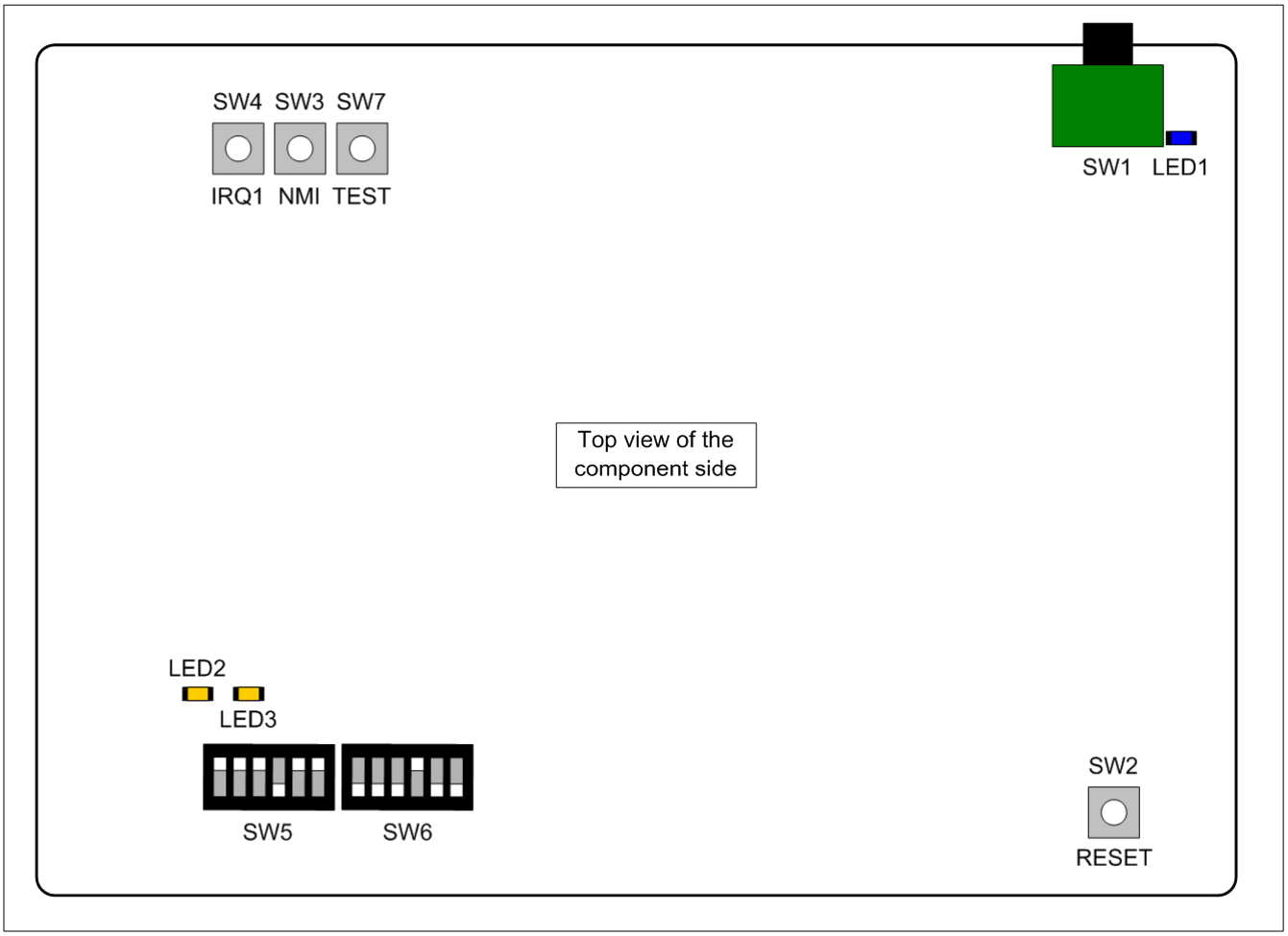


Figure 5.2.3 M3A-HS64 Switches and LEDs Assignments

The following table lists switches mounted on the board.

Table 5.2.7 Switches

Number	Name	Remarks
SW1	Power supply switch	-
SW2	Reset switch	Refer to Section 2.9 for details.
SW3	NMI switch	Refer to Section 2.7 for details.
SW4	IRQ1 switch	Refer to Section 2.7 for details.
SW5	System setting DIP switches (6/package)	Refer to Table 5.2.8 for details.
SW6	User DIP switches (6/package)	Refer to Table 5.2.9 for details.
SW7	TEST switch	Refer to Section 2.7 for details.

Table 5.2.8 System setting DIP switches

Number	Setting		Description
SW5-1 MD_CLK0	OFF	MD_CLK0 = High	Clock operating mode 3
	ON	MD_CLK0 = Low	Clock operating mode 2
SW5-2 MD_BOOT0	OFF	MD_BOOT0 = High	Boot mode: 0 — Boot options: NOR flash memory Boot mode: 1, 3 — Boot options: Serial flash memory Boot mode: 2 — Boot options: NAND flash memory
	ON	MD_BOOT0 = Low	
SW5-3 MD_BOOT1	OFF	MD_BOOT1 = High	
	ON	MD_BOOT1 = Low	
SW5-4 SD_SEL	OFF	SD_SEL = High	Connected to the SDRAM
	ON	SD_SEL = Low	Connected to the MTU2 interface
SW5-5 NAND_SEL	OFF	NAND_SEL = High	Connected to the NAND flash memory
	ON	NAND_SEL = Low	Connected to the device which is connected to the RSPI
SW5-6 RSPI_SEL	OFF	RSPI_SEL = High	Connected to the serial flash memory
	ON	RSPI_SEL = Low	Connected to the expansion connector (CD deck/RSPDIF/MTU2)

Note: The shaded row shows the default setting.

Table 5.2.9 User DIP Switches

Number	Setting		Description
SW6-1 NOR_WP#	OFF	NOR_WP# = High	NOR flash memory is write-enabled
	ON	NOR_WP# = Low	NOR flash memory is write-protected
SW6-2 NAND_WP#	OFF	NAND_WP# = High	NAND flash memory is write-enabled
	ON	NAND_WP# = Low	NAND flash memory is write-protected
SW6-3 SF_WP#	OFF	SF_WP# = High	Serial flash memory is write-enabled
	ON	SF_WP# = Low	Serial flash memory is write-protected
SW6-4 E2P_WP	OFF	EEPROM_WP = High	EEPROM is write-protected
	ON	EEPROM_WP = Low	EEPROM is write-enabled
SW6-5 PA2	OFF	PA2 = High	
	ON	PA2 = Low	
SW6-6 PA3	OFF	PA3 = High	
	ON	PA3 = Low	

Note: The shaded row shows the default setting.

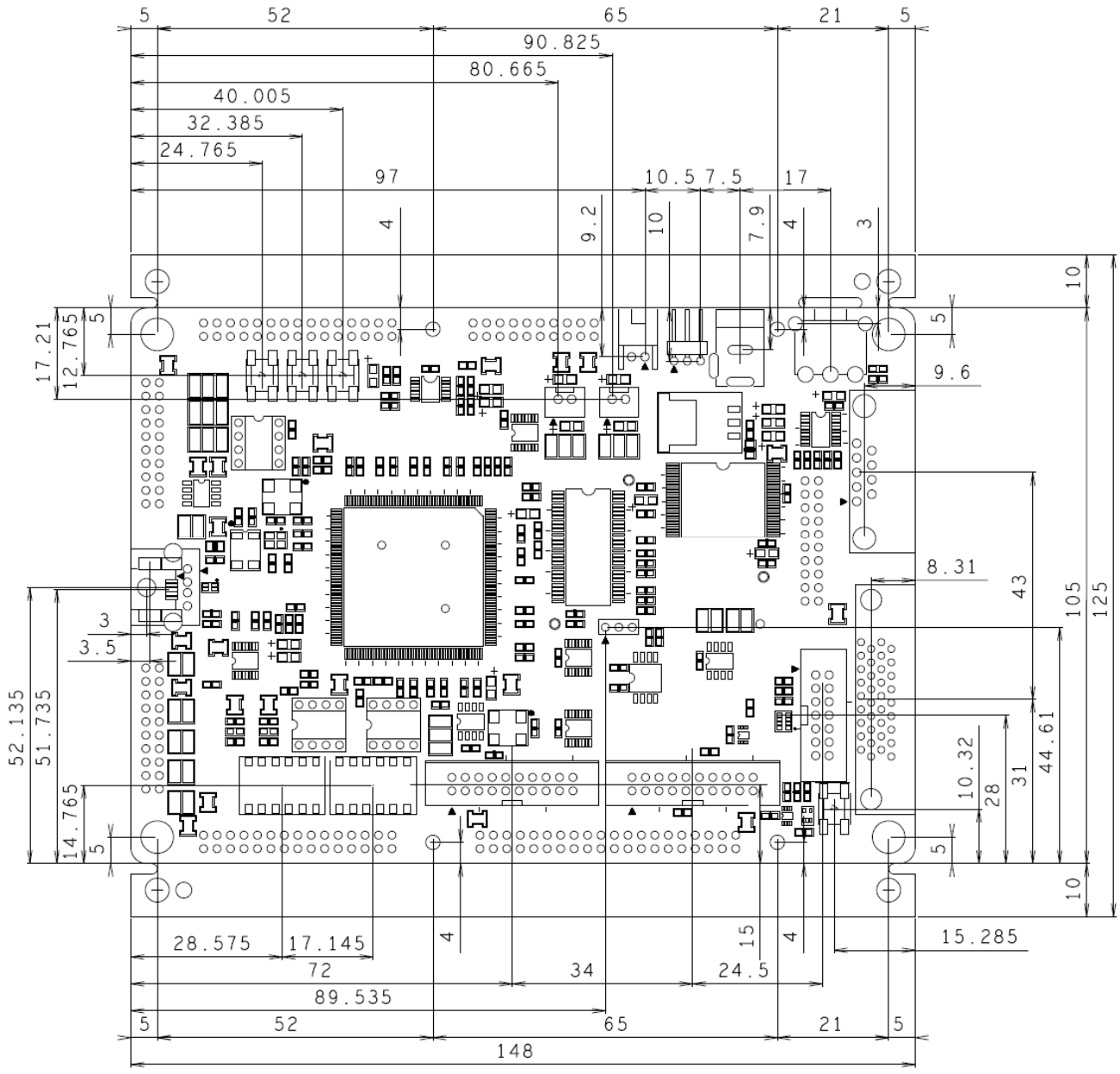
The following table lists LEDs.

Table 5.2.10 LEDs

Number	Color	Description
LED1	Blue	Power supply LED (LED1 is illuminated when 5 V power is supplied)
LED2	Yellow	User LED (LED2 is illuminated when PA0/MD_BOOT1 outputs low)
LED3	Yellow	User LED (LED3 is illuminated when PA1/MD_BOOT0 outputs low)

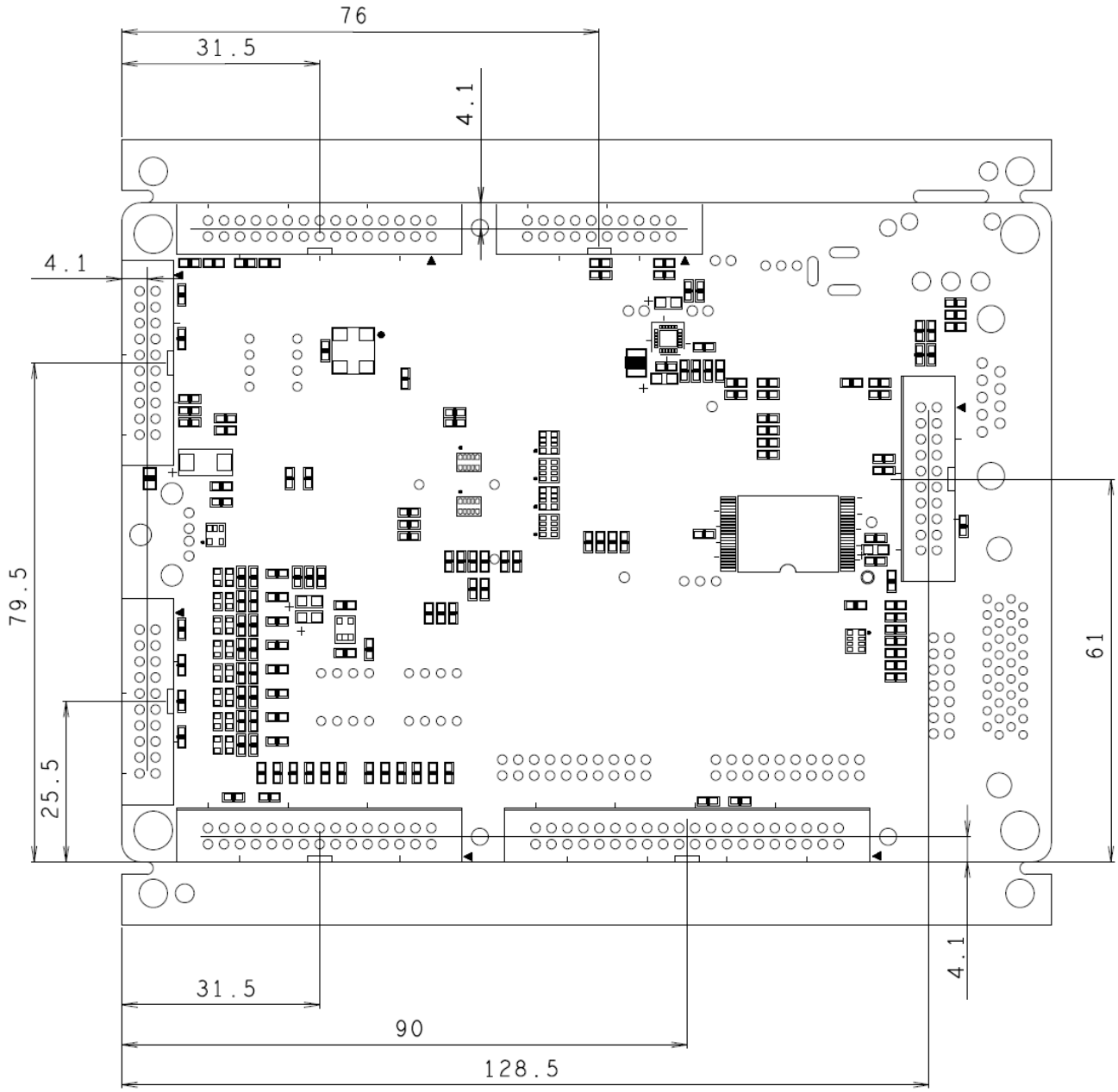
5.3 M3A-HS64 Dimensions

Figure 5.3.1 and Figure 5.3.2 show the M3A-HS64 dimensions.



Note: All measurements are in millimeters.

Figure 5.3.1 M3A-HS64 Dimensions (Top View of the Component Side)



Note: All measurements are in millimeters.

Figure 5.3.2 M3A-HS64 Dimensions (Transparent View of the Component Side)

Chapter 6
M3A-HS64G01 Operating Specifications

6.1 M3A-HS64G01 Connectors

Figure 6.1.1 and Figure 6.1.2 show the connector assignments for the M3A-HS64G01.

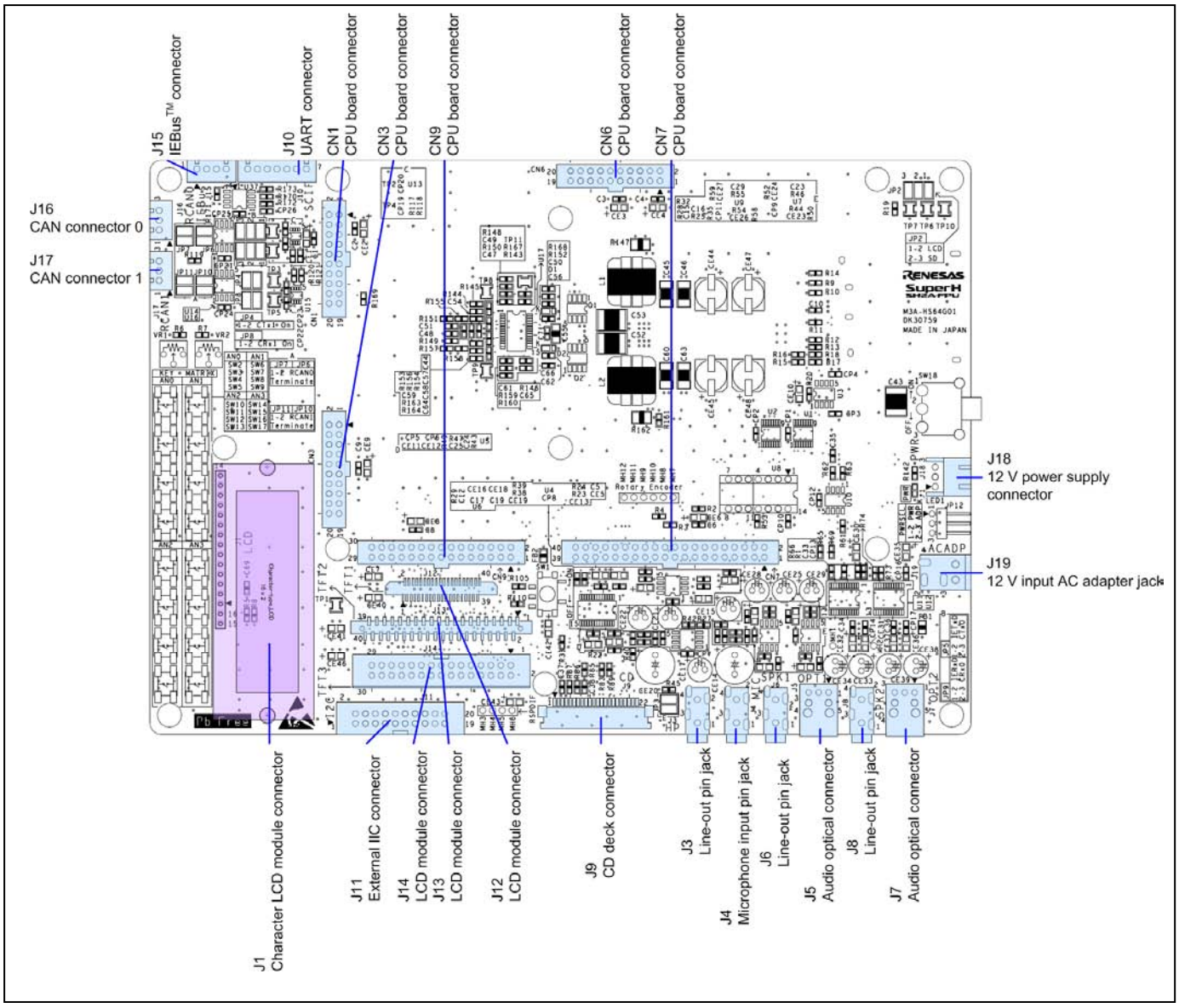


Figure 6.1.1 M3A-HS64G01 Connectors (Top View of the Component Side)

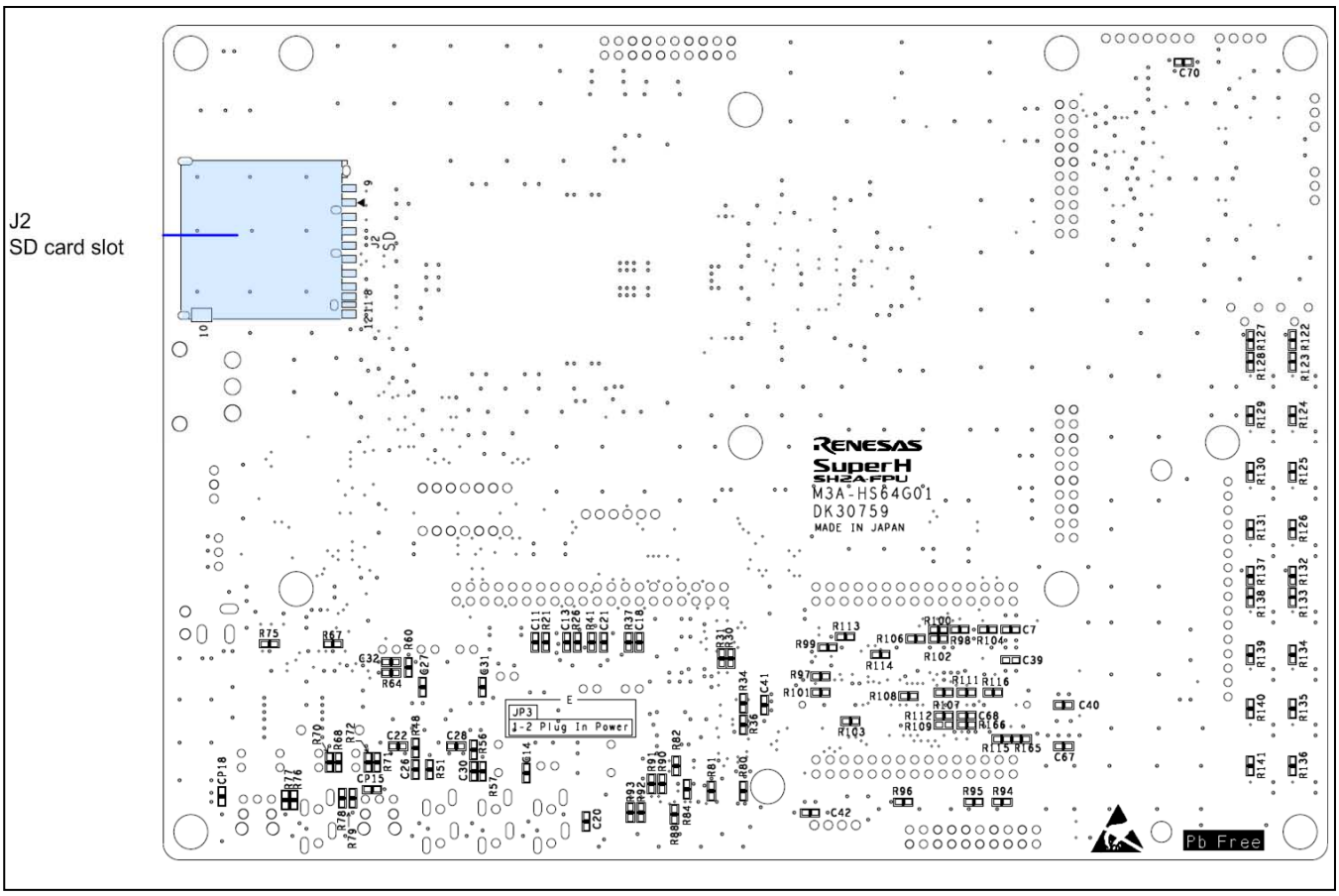


Figure 6.1.2 M3A-HS64G01 Connectors (Top View of the Solder Side)

6.1.1 CPU Board Connectors (CN1, CN3, CN6, CN7 and CN9)

The M3A-HS64G01 includes MIL-spec connectors (CN1, CN3, CN6, CN7, and CN9) for connecting the optional board to the M3A-HS64.

The following figure shows the pin assignments for the CPU board connectors.

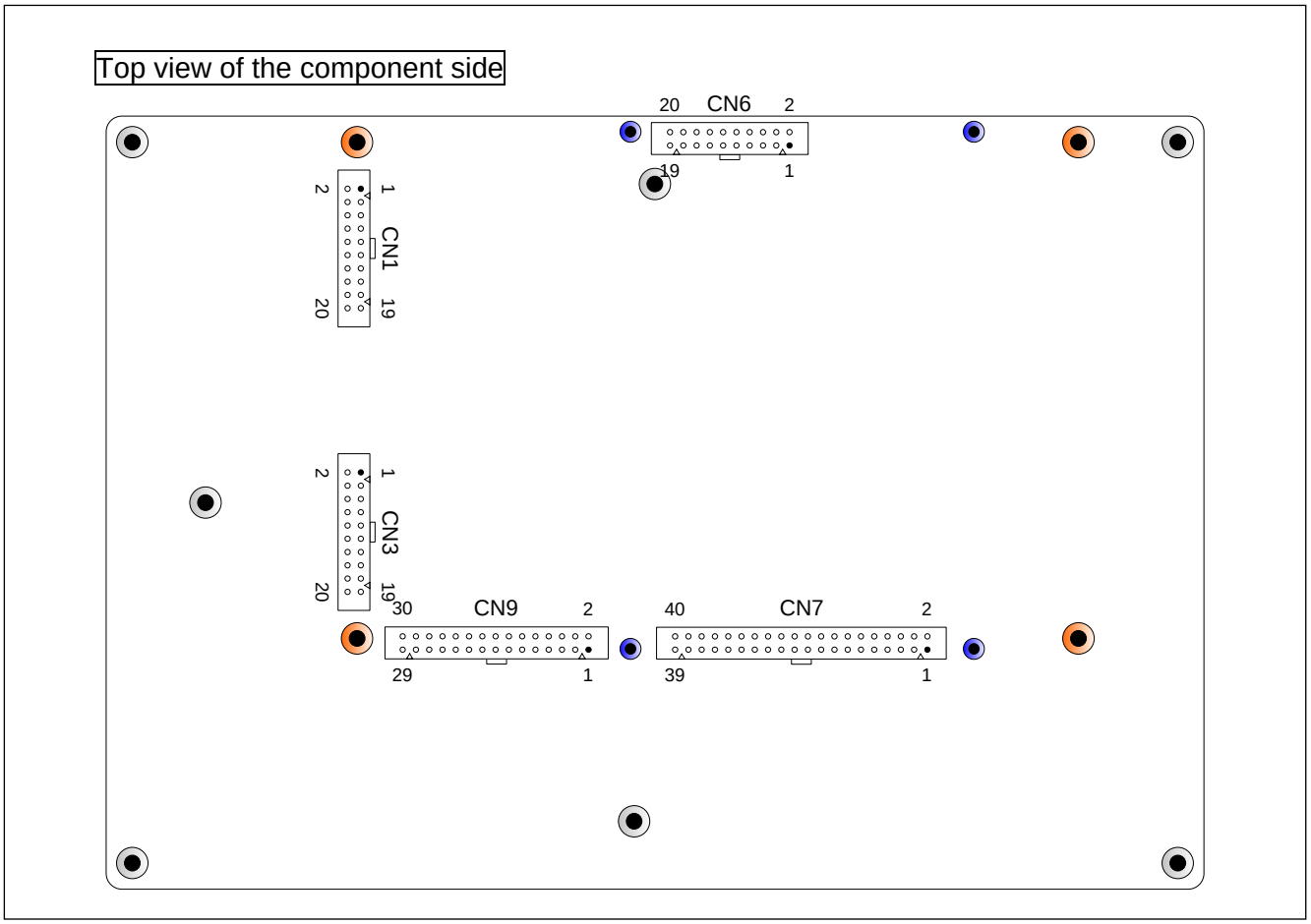


Figure 6.1.3 CPU Board Connectors Pin Assignments (CN1, CN3, CN6, CN7, and CN9)

The following table lists the pin descriptions for CN1.

Table 6.1.1 CN1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PJ11/PWM2H/DACK1 (NC)	2	PJ10/PWM2G/DREQ1
3	5 V	4	PJ9/PWM2F/TEND1
5	PJ8/PWM2E/RTS3#	6	3.3 V
7	PA3/MD_CLK0 (NC)	8	PA2/MD_CLK1 (NC)
9	PA1/MD_BOOT0 (NC)	10	PA0/MD_BOOT1 (NC)
11	GND	12	PJ7/TIOC1B/CTS3#
13	PJ6/TIOC1A/SCK3	14	PJ5/IERxD/TxD3
15	PJ4/IETxD/RxD3	16	GND
17	PJ3/CRx1/CRx0&CRx1/IRQ1	18	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP
19	PJ1/CRx0/IERxD/IRQ0/RxD0	20	PJ0/CTx0/IETxD/CS1#/TxD0/A0

The following table lists the pin descriptions for CN3.

Table 6.1.2 CN3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AVref (NC)	2	AVref (NC)
3	PH1/AN1	4	PH0/AN0
5	AVref (NC)	6	AVref (NC)
7	PH3/AN3	8	PH2/AN2
9	AVcc	10	AVcc
11	PH5/AN5 (NC)	12	PH4/AN4 (NC)
13	AVcc	14	AVcc
15	PH7/AN7	16	PH6/AN6 (NC)
17	AVss	18	AVss
19	AVss	20	AVss

The following table lists the pin descriptions for CN6.

Table 6.1.3 CN6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	2	5 V
3	5 V	4	5 V
5	PC0/CS0# (NC)	6	PC1/RD# (NC)
7	PC2/RDWR# (NC)	8	PC3/WE0#/DQML (NC)
9	PC4/WE1#/DQMU/WE# (NC)	10	3.3 V
11	3.3 V	12	PC9/TIOC2A
13	PC10/TIOC2B	14	PC5/RAS#/TIOC4A/IRQ4 (NC)
15	PC6/CAS#/TIOC4B/IRQ5 (NC)	16	PC7/CKE/TIOC4C/IRQ6 (NC)
17	PC8/CS3#/TIOC4D/IRQ6 (NC)	18	GND
19	GND	20	CKIO (NC)

The following table lists the pin descriptions for CN7.

Table 6.1.4 CN7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PK1/PWM1B/SD_D3	2	PK0/PWM1A/SD_D2
3	PK3/PWM1D/SD_CLK	4	PK2/PWM1C/SD_CMD
5	PE0/SCL0/AUDIO_CLK/IRQ0	6	RES#
7	PE2/SCL1/IRQ2	8	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#
9	PE4/SCL2/DV_VSYNC	10	PE3/SDA1/IRQ3
11	3.3 V	12	PE5/SDA2/DV_HSYNC
13	PK5/PWM1F/SD_D1	14	PK4/PWM1E/SD_D0
15	PK7/PWM1H/SD_CD	16	PK6/PWM1G/SD_WP
17	PF0/WAIT#/SSISCK1/DV_DATA0/SCK2/ TEND0/AUDCK	18	5 V
19	PF2/BACK#/SSIDATA1/DV_DATA2/TxD2 /DACK0/AUDATA0	20	PF1/BREQ#/SSIWS1/DV_DATA1/RxD2/ DREQ0/AUDSYNC#
21	GND	22	PF3/ICIORD#/SSISCK2/DV_DATA3/RxD3/ AUDATA1
23	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5 /TCLKC/AUDATA3	24	PF4/ICIOWR#/AH#/SSIWS2/DV_DATA4/ TxD3/AUDATA2
25	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/ TCLKB	26	GND
27	PF8/CE2B#/SSIDATA3/DV_CLK	28	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
29	GND	30	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
31	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN	32	PF10/A24/SSIWS3/SSL0/TIOC3B/FCE#
33	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT	34	GND
35	PK9/PWM2B/SSIWS0	36	PK8/PWM2A/SSISCK0
37	PK11/PWM2D/SSITxD0	38	PK10/PWM2C/SSIRxD0
39	GND	40	AUDIO_XTAL

The following table lists the pin descriptions for CN9.

Table 6.1.5 CN9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PG1/LCD_DATA1/SD_D3/PINT1	2	PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#
3	PG3/LCD_DATA3/SD_CLK/PINT3	4	PG2/LCD_DATA2/SD_CMD/PINT2
5	GND	6	PG4/LCD_DATA4/SD_D0/PINT4
7	PG6/LCD_DATA6/SD_WP/PINT6	8	PG5/LCD_DATA5/SD_D1/PINT5
9	PG7/LCD_DATA7/SD_CD/PINT7	10	GND
11	PG9/LCD_DATA9/SSIWS0/TxD4/SIOFSYNC	12	PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK
13	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/SIOFTxD	14	PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/SIOFRxD
15	GND	16	PG12/LCD_DATA12/TIOC0A/RxD1
17	PG14/LCD_DATA14/TIOC0C/SCK1	18	PG13/LCD_DATA13/TIOC0B/TxD1
19	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#	20	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
21	PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6	22	5 V
23	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7	24	PG18/LCD_DE/TIOC2A/SSL1/TxD6
25	3.3 V	26	PG20/LCD_EXTCLK/MISO1/TxD7 (NC)
27	PG22/SSL1/TIOC0B	28	PG21/RSPCK1/TIOC0A
29	PG24/MISO1/TIOC0D	30	PG23/MOSI1/TIOC0C

6.1.2 Character LCD Module Connector (J1)

The M3A-HS64G01 includes a character LCD module connector (J1).

The following figure shows the pin assignments for J1.

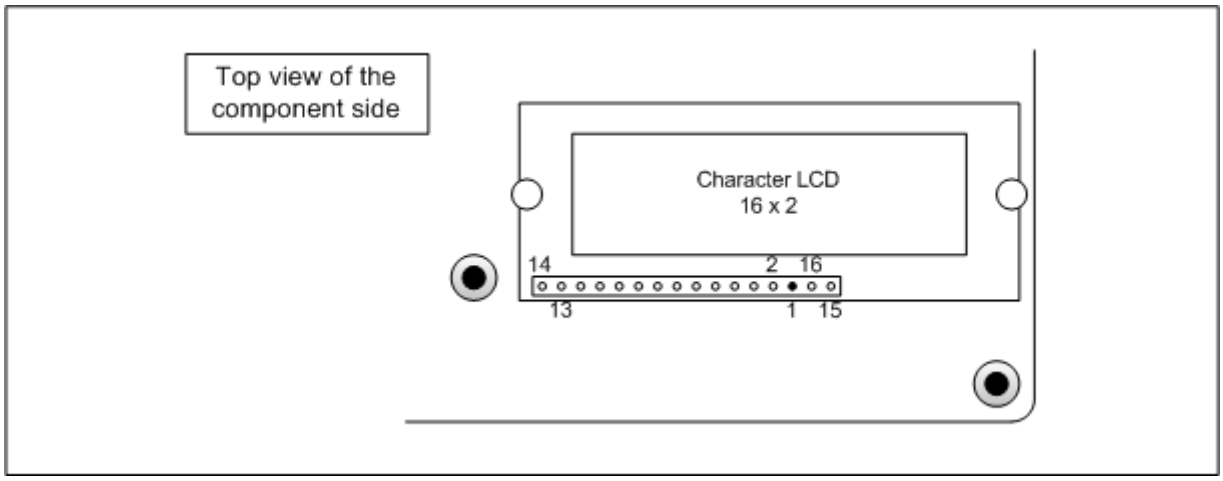


Figure 6.1.4 J1 Pin Assignments

The following table lists the pin descriptions for J1.

Table 6.1.6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	5 V
3	Vo (Adjust 5 V by the voltage resistor VR1 to input)	4	RS (PC9/TIOC2A)
5	R/W# (GND)	6	E (PC10/TIOC2B)
7	DB0 (PK0/PWM1A/SD_D2)	8	DB1 (PK1/PWM1B/SD_D3)
9	DB2 (PK2/PWM1C/SD_CMD)	10	DB3 (PK3/PWM1D/SD_CLK)
11	DB4 (PK4/PWM1E/SD_D0)	12	DB5 (PK5/PWM1F/SD_D1)
13	DB6 (PK6/PWM1G/SD_WP)	14	DB7 (PK7/PWM1H/SD_CD)
15	A (Adjust 5 V by the variable resistor VR2 to input)	16	K (GND)

6.1.3 SD Card Slot (J2)

The M3A-HS64G01 includes an SD card slot (J2).

The following table shows the pin assignments for J2.

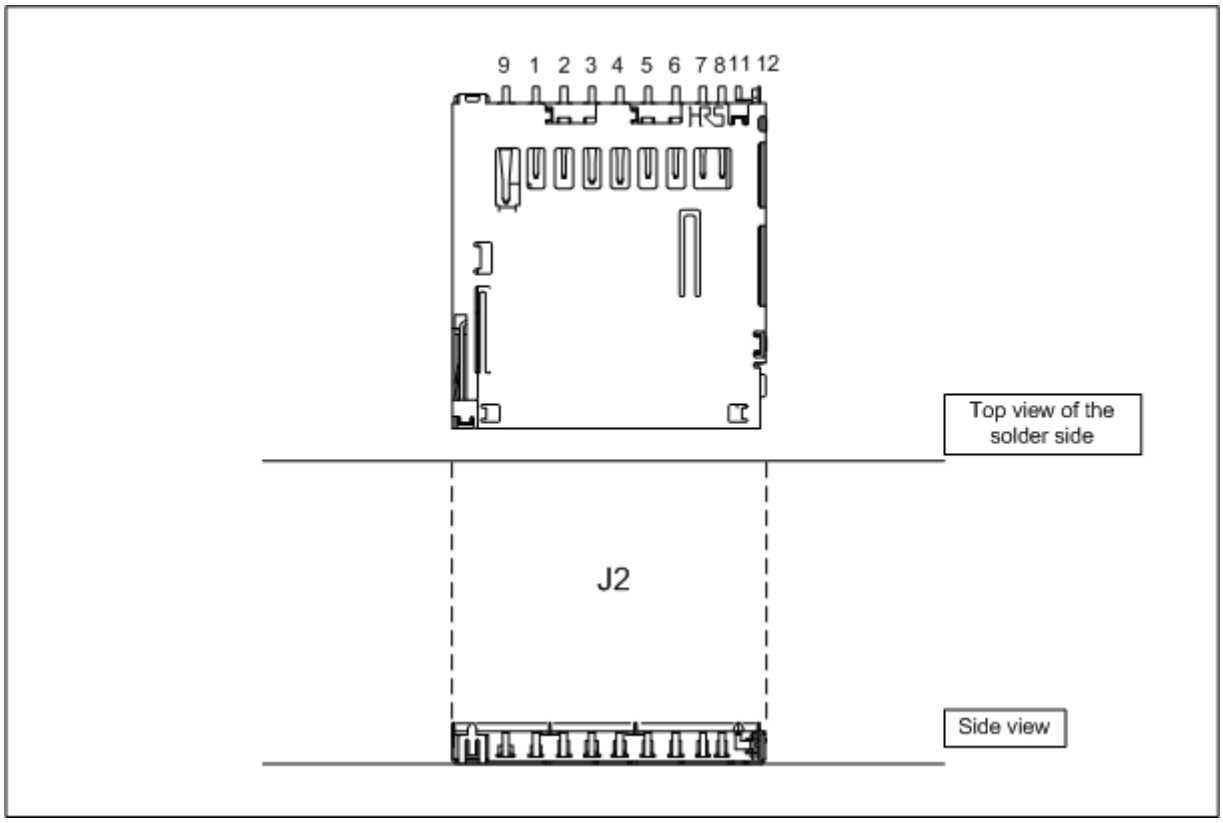


Figure 6.1.5 J2 Pin Assignments

The following table lists the pin descriptions for J2.

Table 6.1.7 J2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	DAT3 (PK1/PWM1B/SD_D3)	7	DAT0 (PK4/PWM1E/SD_D0)
2	CMD (PK2/PWM1C/SD_CMD)	8	DAT1 (PK5/PWM1F/SD_D1)
3	GND	9	DAT2 (PK0/PWM1A/SD_D2)
4	3.3 V	10	WP (PK6/PWM1G/SD_WP)
5	CLK (PK3/PWM1D/SD_CLK)	11	CD (PK7/PWM1H/SD_CD)
6	GND	12	COMMON (GND)

6.1.4 Line-out Pin Jacks (J3, J6, and J8)

The M3A-HS64G01 includes line-out pin jacks (J3, J6, and J8).

The following figure shows the pin assignments for J3, J6 and J8.

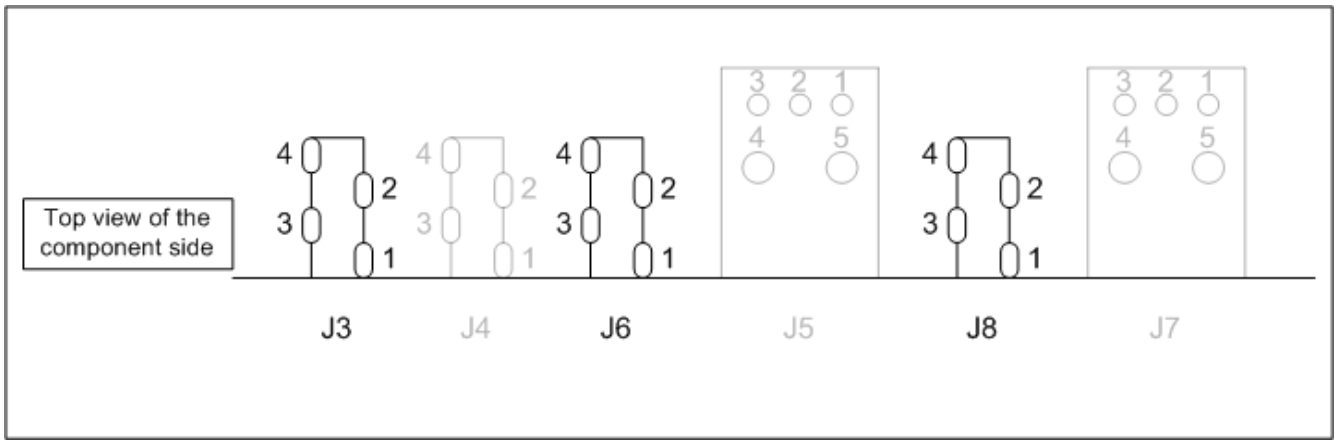


Figure 6.1.6 Line-out Pin Jacks Pin Assignments (J3, J6, and J8)

The following table lists the pin descriptions for J3, J6, and J8.

Table 6.1.8 Line-out Pin Jacks Pin Descriptions (J3, J6, and J8)

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AOUTR (An analog output R pin of the D/A converter)
2	AOUTL (An analog output L pin of the D/A converter)	4	NC

6.1.5 Microphone Input Pin Jack (J4)

The M3A-HS64G01 includes a microphone input pin jack (J4).

The following figure shows the pin assignments for J4.

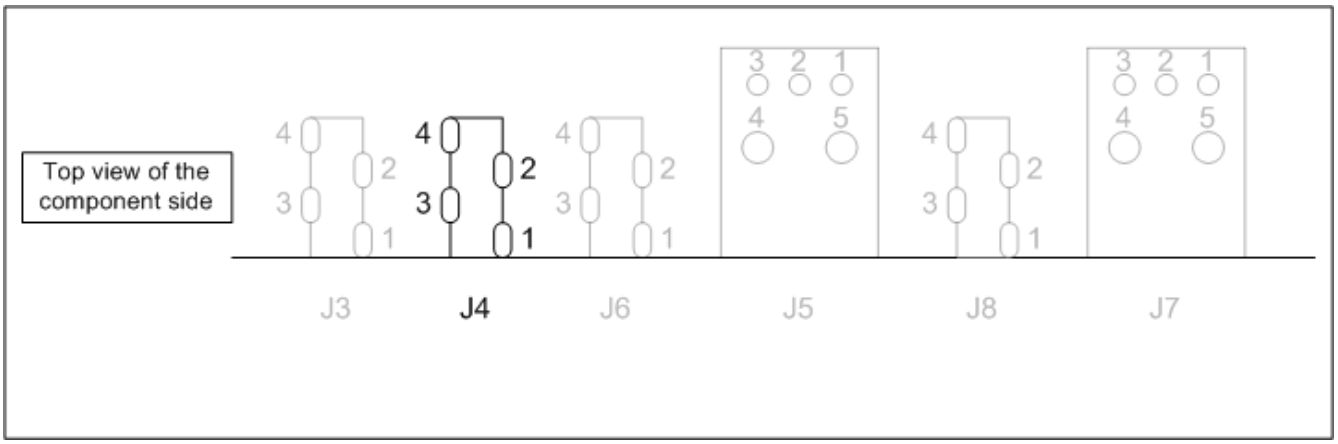


Figure 6.1.7 J4 Pin Assignments

The following table lists the pin descriptions for J4.

Table 6.1.9 J4 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AINR (An analog input R pin of the A/D converter)
2	AINL (An analog input L pin of the A/D converter)	4	NC

6.1.6 Audio Optical Connectors (J5 and J7)

The M3A-HS64G01 includes audio optical connectors (J5 and J7).

The following figure shows the pin assignments for J5 and J7.

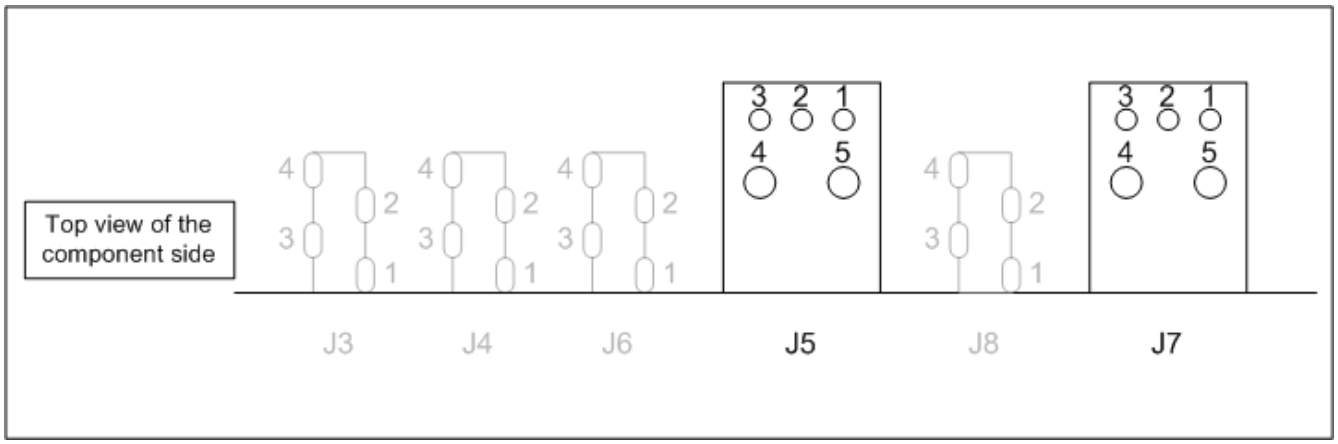


Figure 6.1.8 J5, J7 Pin Assignments

The following table lists the pin descriptions for J5 and J7.

Table 6.1.10 Pin Assignments for Optical Connectors (J5 and J7)

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	4	NC
2	3.3 V	5	NC
3	TX (An optical output pin of the D/A converter)	-	

6.1.7 CD Deck Connector (J9)

The M3A-HS64G01 includes a flexible connector (J9) for connecting a CD deck to the board.

The following figure shows the pin assignments for J9.

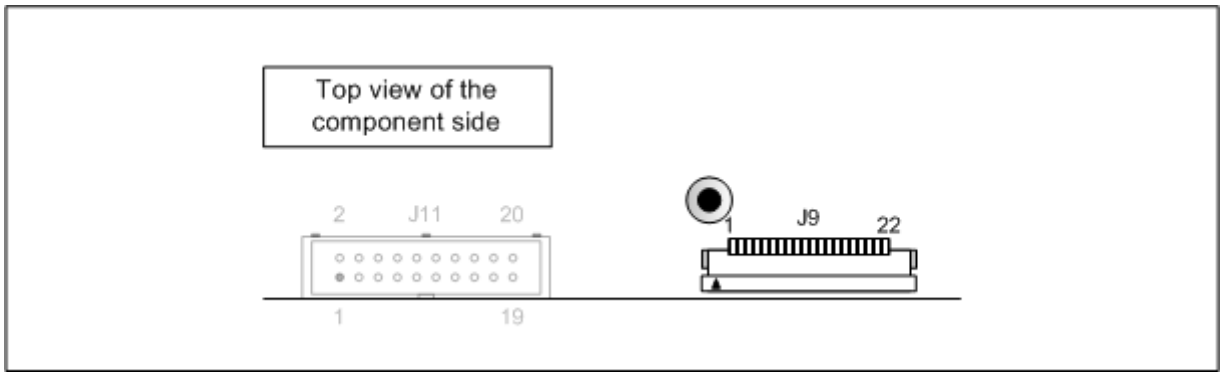


Figure 6.1.9 J9 Pin Assignments

The following table lists the pin descriptions for J9.

Table 6.1.11 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	12	CDFS (PF10/A24/SSIWS3/SSL0/TIOC3B/FCE#)
2	GND	13	CDSI (PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN)
3	8 V	14	CDCK (PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB)
4	8 V	15	CDSO (PF12/BS#/MISO0/TIOC3D/SPDIF_OUT)
5	FLAG6 (PJ9/PWM2F/TEND1)	16	NC
6	NC	17	IIS_BCK (PF6/CS6#/CE1B#/SSISCK3/DV_DATA6 /TCLKB)
7	CDRST (Connects the output of the reset IC)	18	IIS_LRCK (PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD)
8	GND	19	IIS_DATA/GND (PF8/CE2B#/SSIDATA3/DV_CLK)
9	3.3 V	20	BLKCK (PE1/SDA0/IOIS16#/IRQ1/TCLKA/ ADTRG#)
10	3.3 V	21	TRANS (PJ10/PWM2G/DREQ1)
11	GND	22	NC

6.1.8 UART Connector (J10)

The M3A-HS64G01 includes a UART connector (J10) with TTL-level flow control.

The following figure shows the pin assignments for J10.

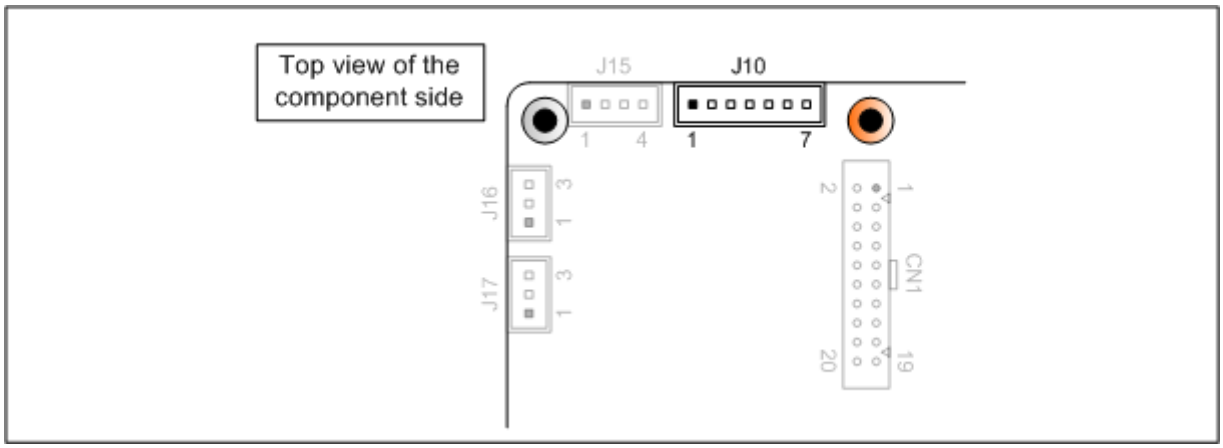


Figure 6.1.10 J10 Pin Assignments

The following table lists the pin descriptions for J10.

Table 6.1.12 J10 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	5	CTS# (PJ7/TIOC1B/CTS3#)
2	RXD (PJ4/IETxD/RxD3)	6	RTS# (PJ8/PWM2E/RTS3#)
3	TXD (PJ5/IERxD/TxD3)	7	GND
4	SCK (PJ6/TIOC1A/SCK3)	-	

6.1.9 External IIC Connector (J11)

The M3A-HS64G01 includes a MIL-spec connector (J11) for connecting an external IIC interface to the board.

The following figure shows the pin assignments for J11.

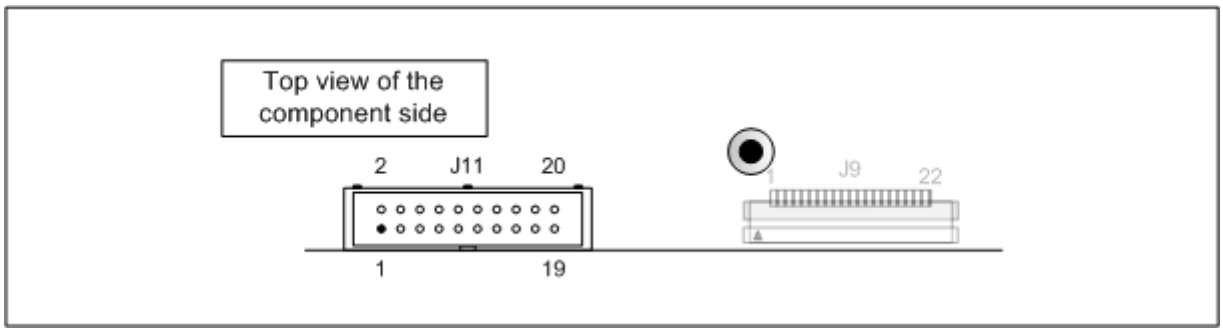


Figure 6.1.11 J11 Pin Assignments

Table 6.1.13 Pin Assignments for External IIC Connector (J11)

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	2	3.3 V
3		4	
5		6	GND (See note)
7		8	
9		10	GND (See note)
11		12	
13		14	
15		16	
17	SCL (PE4/SCL2/DV_VSYNC)	18	SDA (PE5/SDA2/DV_HSYNC)
19		20	GND (See note)

Note: For compatibility with other CPU boards, this connector is connected with the board via a 0 Ω resistor.

6.1.10 LCD Module Connectors (J12 to J14)

The M3A-HS64G01 includes two flexible connectors (J12 and J13) and one MIL-spec connector (J14) for connecting an LCD module to the board.

The following figure shows the pin assignments for LCD module connectors.

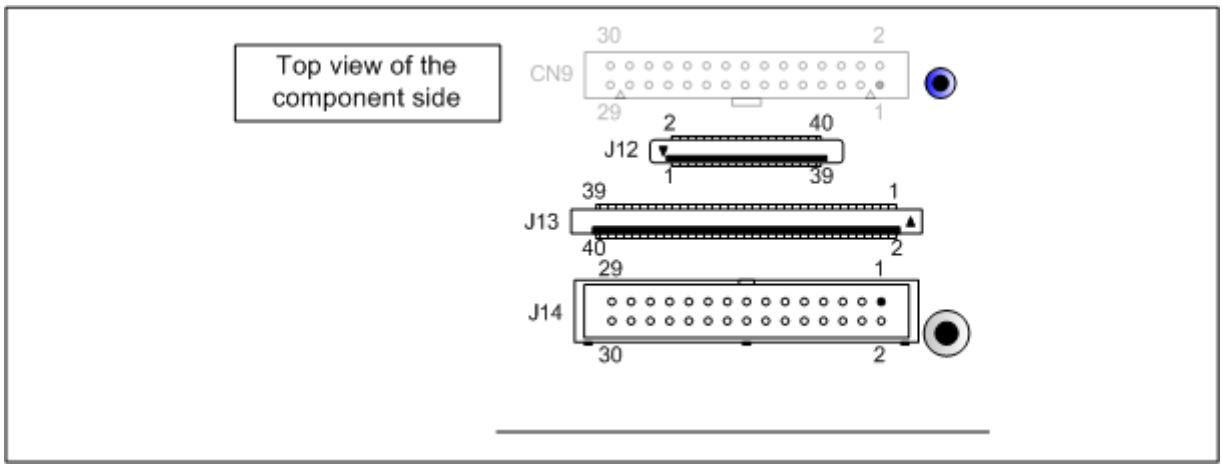


Figure 6.1.12 LCD Module Connectors Pin Assignments (J12 to J14)

The following table lists the pin descriptions for J12.

Table 6.1.14 J12 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	2	3.3 V
3	3.3 V	4	DCLK (PG19/LCD_CLK/TIOC2B/MOSI1/RxD7)
5	GND	6	HSYNC (PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6)
7	GND	8	DTMG (PG18/LCD_DE/TIOC2A/SSL1/TxD6)
9	GND	10	NC
11	GND	12	R5 (PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#)
13	R4 (PG14/LCD_DATA14/TIOC0C/SCK1)	14	R3 (PG13/LCD_DATA13/TIOC0B/TxD1)
15	GND	16	R2 (PG12/LCD_DATA12/TIOC0A/RxD1)
17	R1(PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)	18	R0 (PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/ SIOFTxD)
19	GND	20	G5 (PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/ SIOFRxD)
21	G4 (PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC)	22	G3 (PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK)
23	GND	24	G2 (PG7/LCD_DATA7/SD_CD/PINT7)
25	G1 (PG6/LCD_DATA6/SD_WP/PINT6)	26	G0 (PG5/LCD_DATA5/SD_D1/PINT5)
27	GND	28	B5 (PG4/LCD_DATA4/SD_D0/PINT4)
29	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)	30	B3 (PG2/LCD_DATA2/SD_CMD/PINT29
31	GND	32	B2 (PG1/LCD_DATA1/SD_D3/PINT1)
33	B1 (PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#)	34	B0 (PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#)
35	PCI (Inputs 3.3 V or GND by a toggle switch)	36	Vctrl (3.3 V)
37	NC	38	NC
39	NC	40	NC

The following table lists the pin descriptions for J13.

Table 6.1.15 J13 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	2	DTMG (PG18/LCD_DE/TIOC2A/SSL1/TxD6)
3	HREV (3.3 V or GND)	4	B5 (PG4/LCD_DATA4/SD_D0/PINT4)
5	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)	6	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)
7	B2 (PG1/LCD_DATA1/SD_D3/PINT1)	8	B1 (PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#)
9	B0 (PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#)	10	3.3 V
11	3.3 V	12	G5 (PG10/LCD_DATA10/SSIRxD0/IRQ2/ RxD5/SIOFRxD)
13	G4 (PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC)	14	G3 (PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK)
15	G2 (PG7/LCD_DATA7/SD_CD/PINT7)	16	G1 (PG6/LCD_DATA6/SD_WP/PINT6)
17	G0 (PG5/LCD_DATA5/SD_D1/PINT5)	18	GND
19	R5 (PG15/LCD_DATA15/TIOC0D/RxD3/ RTS1#)	20	R4 (PG14/LCD_DATA14/TIOC0C/SCK1)
21	R3 (PG13/LCD_DATA13/TIOC0B/TxD1)	22	R2 (PG12/LCD_DATA12/TIOC0A/RxD1)
23	R1 (PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)	24	R0 (PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/ SIOFTxD)
25	VREV (3.3 V or GND)	26	NC
27	NC	28	GND
29	DCLK (PG19/LCD_CLK/TIOC2B/MOSI1/ RxD7)	30	GND
31	GND	32	GND
33	GND	34	GND
35	TMZ (PH7/AN7)	36	GND
37	DIM (3.3 V)	38	NC
39	5 V	40	5 V

The following table lists the pin descriptions for J14.

Table 6.1.16 J14 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	2	3.3 V
3	3.3 V	4	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
5	PG14/LCD_DATA14/TIOC0C/SCK1	6	PG13/LCD_DATA13/TIOC0B/TxD1
7	PG12/LCD_DATA12/TIOC0A/RxD1	8	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/ SIOFTxD
9	PG10/LCD_DATA10/SSIRxD0/IRQ2/ RxD5/SIOFRxD	10	PG9/LCD_DATA9/SSIWS0/TxD4/SIOFSYNC
11	PG8/LCD_DATA8/SSISCK0/RxD4/ SIOFSCK	12	PG7/LCD_DATA7/SD_CD/PINT7
13	PG6/LCD_DATA6/SD_WP/PINT6	14	PG5/LCD_DATA5/SD_D1/PINT5
15	PG4/LCD_DATA4/SD_D0/PINT4	16	PG3/LCD_DATA3/SD_CLK/PINT3
17	PG2/LCD_DATA2/SD_CMD/PINT2	18	PG1/LCD_DATA1/SD_D3/PINT1
19	PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#	20	GND
21	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7	22	PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6
23	NC (LCD_VCPWC)	24	NC (Allowed to supply 5 V through 0 Ω resistor)
25	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#	26	PG18/LCD_DE/TIOC2A/SSL1/TxD6
27	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP	28	GND
29	GND	30	GND

6.1.11 IEBus™ Connector (J15)

The M3A-HS64G01 includes an IEBus™ connector (J15).

The following figure shows the pin assignments for J15.

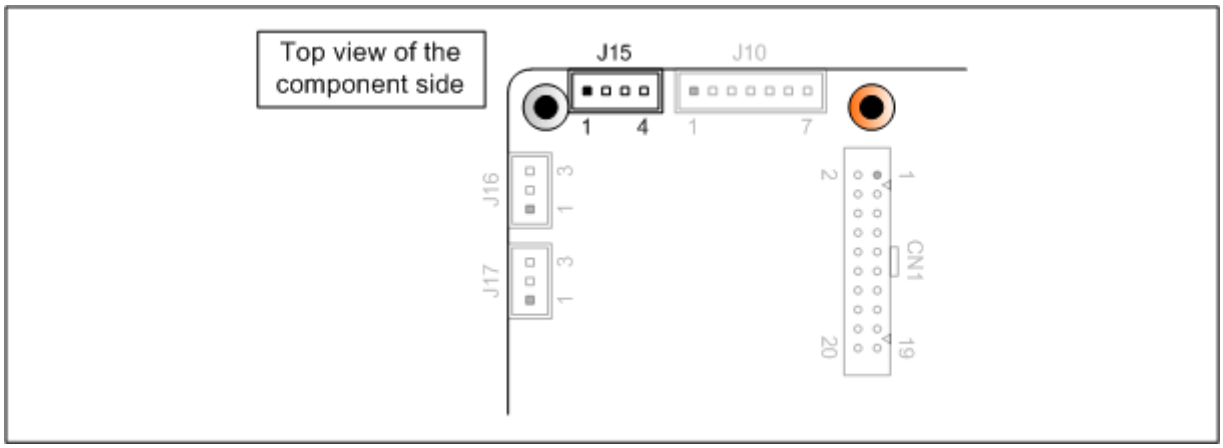


Figure 6.1.13 J15 Pin Assignments

The following table lists the pin descriptions for J15.

Table 6.1.17 J15 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	3	BUS+
2	BUS-	4	GND

6.1.12 CAN Connectors (J16 and J17)

The M3A-HS64G01 includes CAN connectors (J16 and J17).

The following figure shows the pin assignments for J16 and J17.

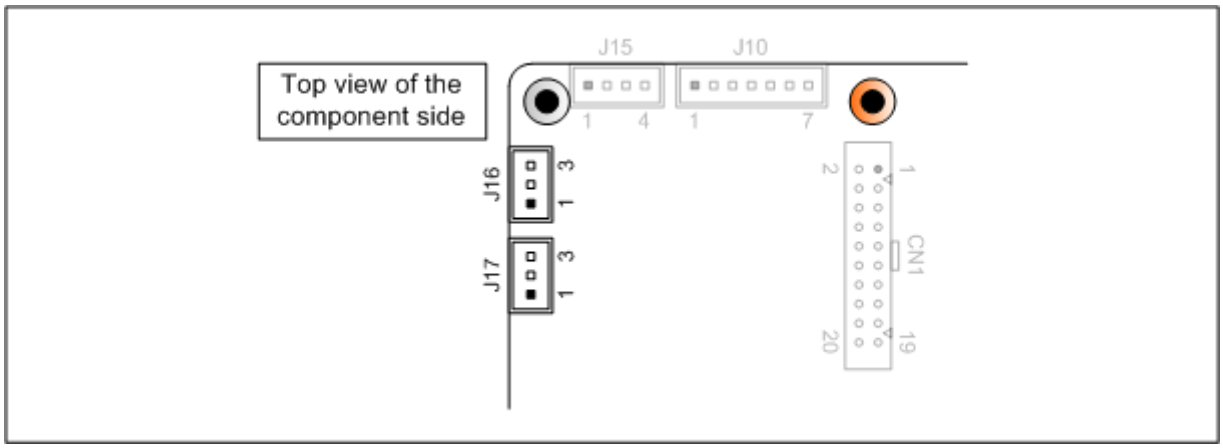


Figure 6.1.14 J16, J17 Pin Assignments

The following table lists the pin descriptions for J16 and J17.

Table 6.1.18 J16, J17 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	CANH	3	GND
2	CANL	-	

J16 and J17 are connected to channel 0 (CTx0/CRx0) and channel 1 (CTx1/CRx1), respectively.

6.1.13 12 V Power Supply Connector (J18)

The M3A-HS64G01 includes a system power supply connector (J18). The number of pins of this connector differs from the power supply connector mounted on the M3A-HS64 to prevent improper insertion.

The following figure shows the pin assignments for J18.

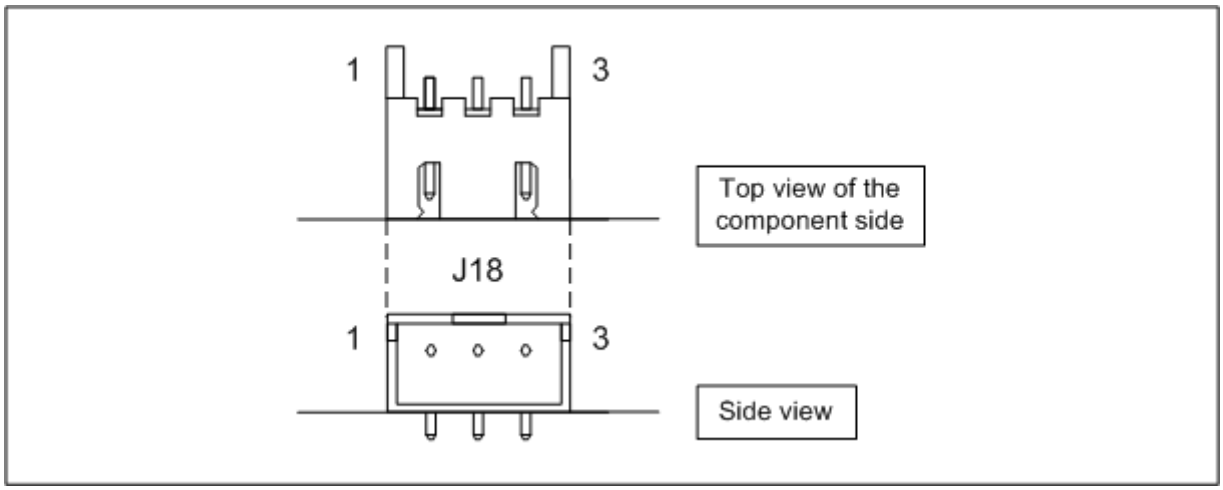


Figure 6.1.15 J18 Pin Assignments

The following table lists the pin descriptions for J18.

Table 6.1.19 J18 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	12 V	3	GND
2	NC	-	

6.1.14 12 V Input AC Adapter Jack (J19)

The M3A-HS64G01 includes an AC adapter jack (J19) for 12 V DC input.

The following figure shows the pin assignments for J19.

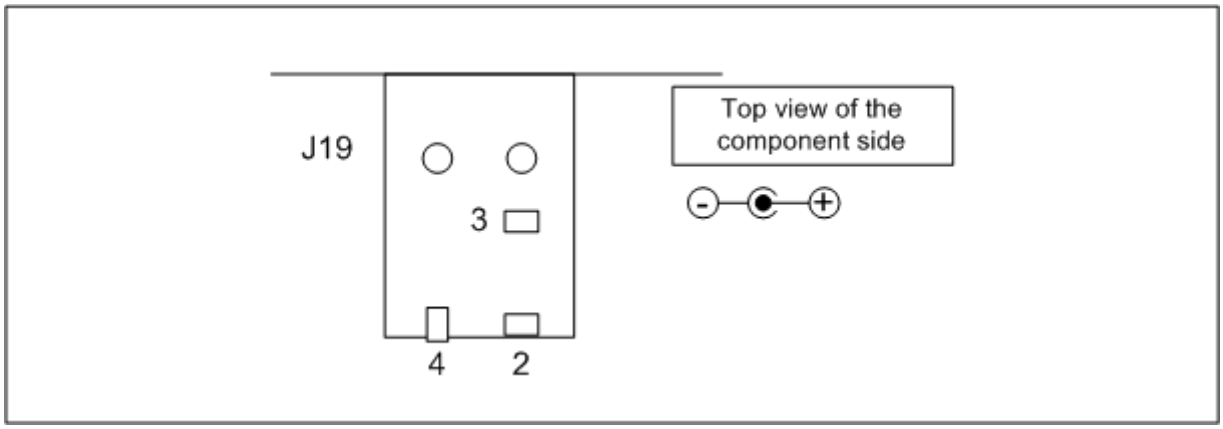


Figure 6.1.16 J19 Pin Assignments

The following table lists the pin descriptions for J19.

Table 6.1.20 J19 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC (No pins)	2	12 V
3	GND	4	GND

6.2 M3A-HS64G01 Operating Components

The following figure shows the assignments of the M3A-HS64G01 operating components.

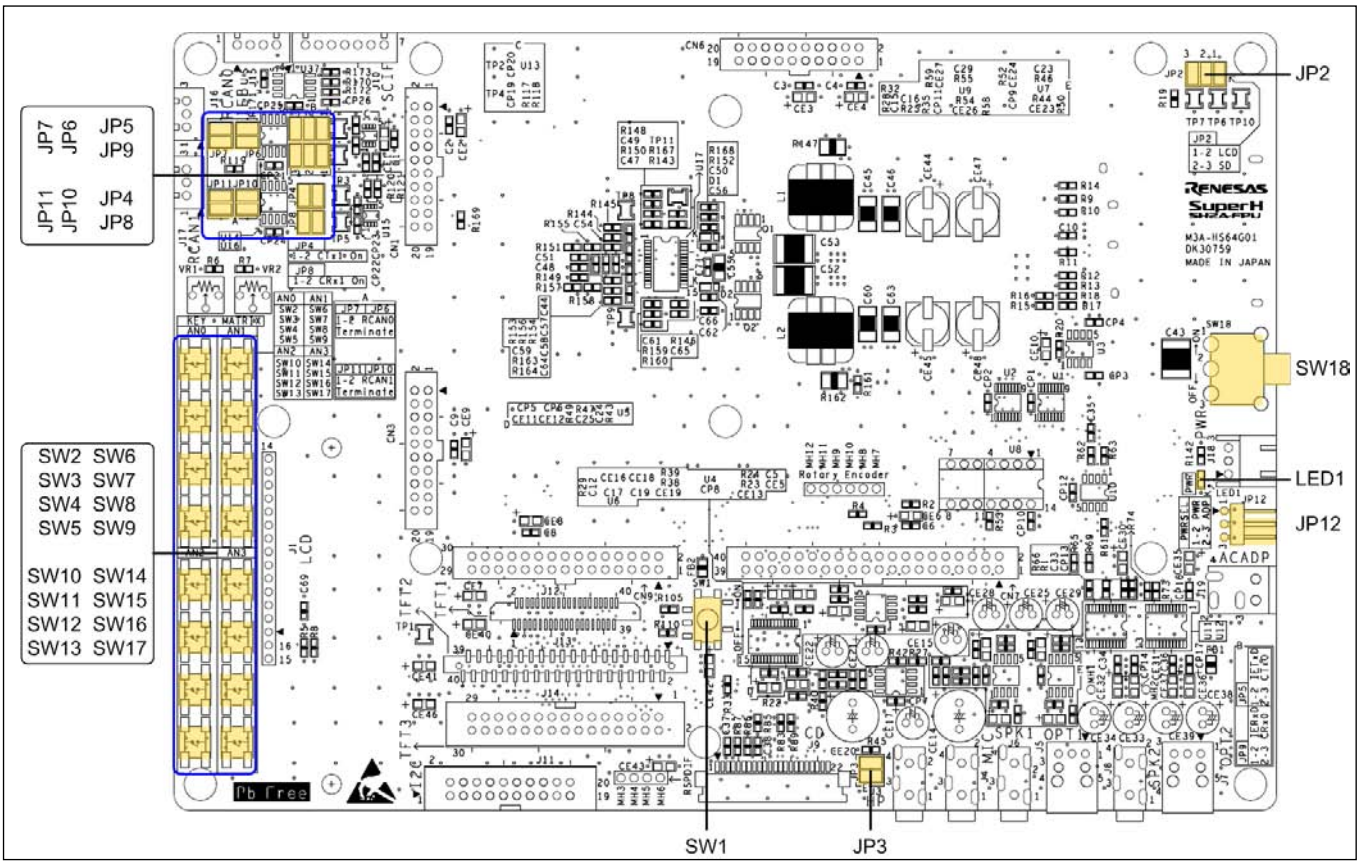


Figure 6.2.1 M3A-HS64G01 Operating Component Assignments (Top View of the Component Side)

6.2.1 Jumpers (JP2 to JP12)

The M3A-HS64G01 includes 11 jumpers.

The following figure shows jumper assignments (JP2 to JP12) on the M3A-HS64G01.

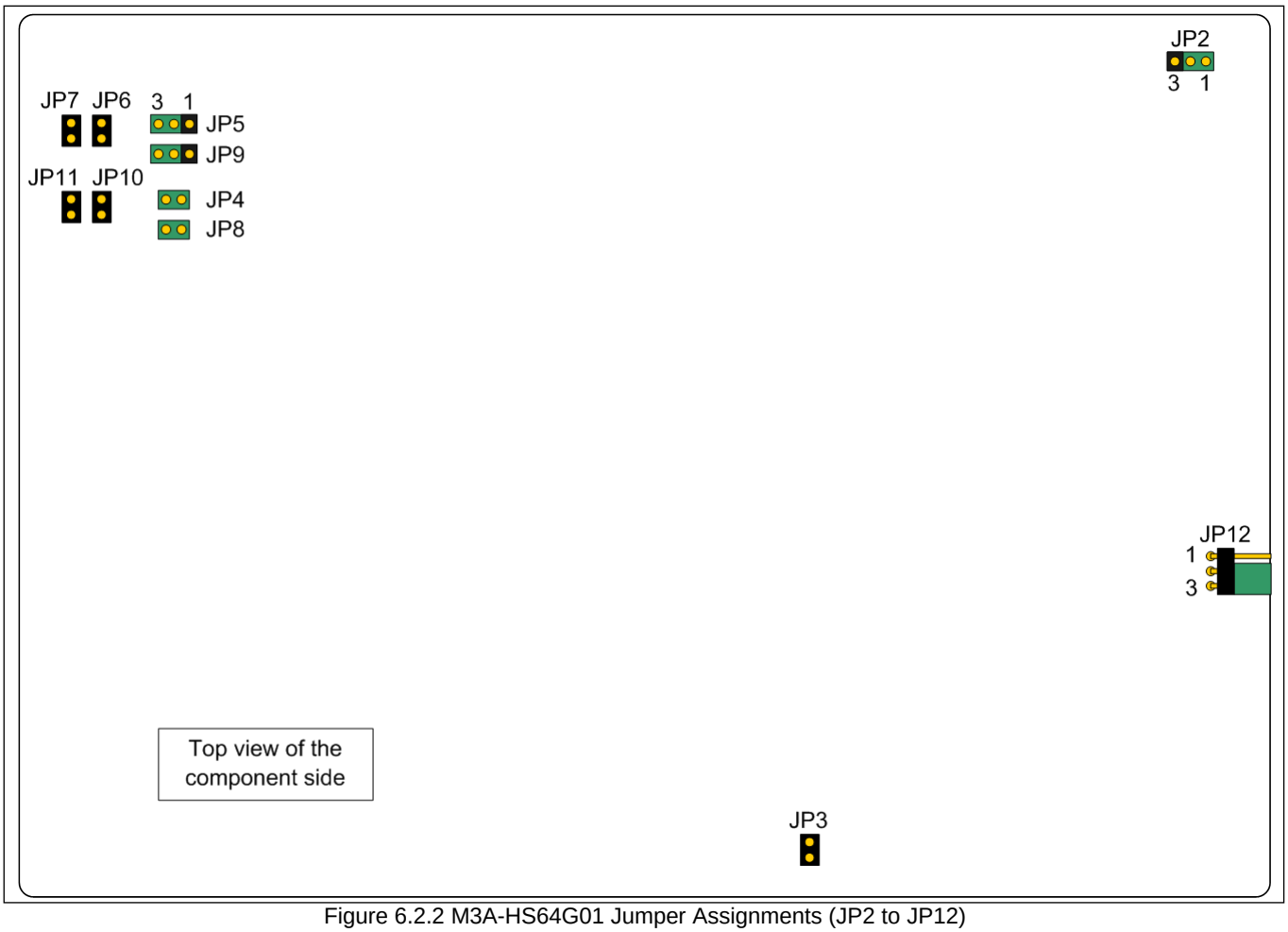


Figure 6.2.2 M3A-HS64G01 Jumper Assignments (JP2 to JP12)

The following table lists the jumpers setting for JP2, JP5, and JP9.

Table 6.2.1 Multiplexed Pin Switch Jumpers Setting (JP2, JP5, and JP9)

Number	Setting	Description
JP2	1 - 2	Connects the character LCD connector (J1) as the LCD data output pin
LCD/SD	2 - 3	Connects the SD card slot (J1) as the SDHI I/O pin
JP5	1 - 2	Connects the IEBus™ driver (U37) as the IETxD output pin
IETxD/CTx0	2 - 3	Connects the CAN driver (U14) as the CTx0 output pin
JP9	1 - 2	Connects the IEBus™ driver (U37) as the IERxD input pin
IERxD/CRx0	2 - 3	Connects the CAN driver (U14) as the CRx0 input pin

Notes:

1. The shaded row shows the default setting.
2. Do not change the jumper settings while the M3A-HS64G01 is ON. Be sure to turn the power OFF before changing the settings.

The following table lists the jumpers setting for JP3.

Table 6.2.2 Plug-in Power Microphone Jumper Setting (JP3)

Number	Setting	Description
JP3	1 - 2	Supplies the power (Plug-in power microphone)
	Open	Does not supply the power (Typical microphone)

The following table lists the jumpers setting for JP4, JP6, JP7, JP8, JP10, and JP11.

Table 6.2.3 CAN Evaluation Jumpers Setting (JP4, JP6, JP7, JP8, JP10, and JP11)

Number	Setting	Description
JP4 Connects CTx1	1 - 2	Connects the CTx1 pin to the CAN driver (U16)
	Open	Leaves the CTx1 pin disconnected to the CAN driver (U16)
JP8 Connects CRx1	1 - 2	Connects the CRx1 pin to the CAN driver (U16)
	Open	Leaves the CRx1 pin disconnected to the CAN driver (U16)
JP6 Terminates CANL (ch0)	1 - 2	Terminates the CANL (ch0) pin
	Open	Leaves the CANL (ch0) pin not terminated
JP7 Terminates CANH (ch0)	1 - 2	Terminates the CANH (ch0) pin
	Open	Leaves the CANH (ch0) pin not terminated
JP10 Terminates CANL (ch1)	1 - 2	Terminates the CANL (ch1) pin
	Open	Leaves the CANL (ch1) pin not terminated
JP11 Terminates CANH (ch1)	1 - 2	Terminates the CANH (ch1) pin
	Open	Leaves the CANH (ch1) pin not terminated

The following table lists the jumpers setting for JP12.

Table 6.2.4 Power Supply Switch Jumper Setting (JP12)

Number	Setting	Description
JP12 PWRSEL	1 - 2	Supplies the system power from J18
	2 - 3	Supplies the system power from J19 (AC adapter is used)

Notes:

1. The shaded row shows the default setting.
2. Do not change the jumper settings while the M3A-HS64G01 is ON. Be sure to turn the power OFF before changing the settings.

6.2.2 Switches and LED

The M3A-HS64G01 includes 18 switches and one LED.

The following figure shows assignments for switches and the LED.

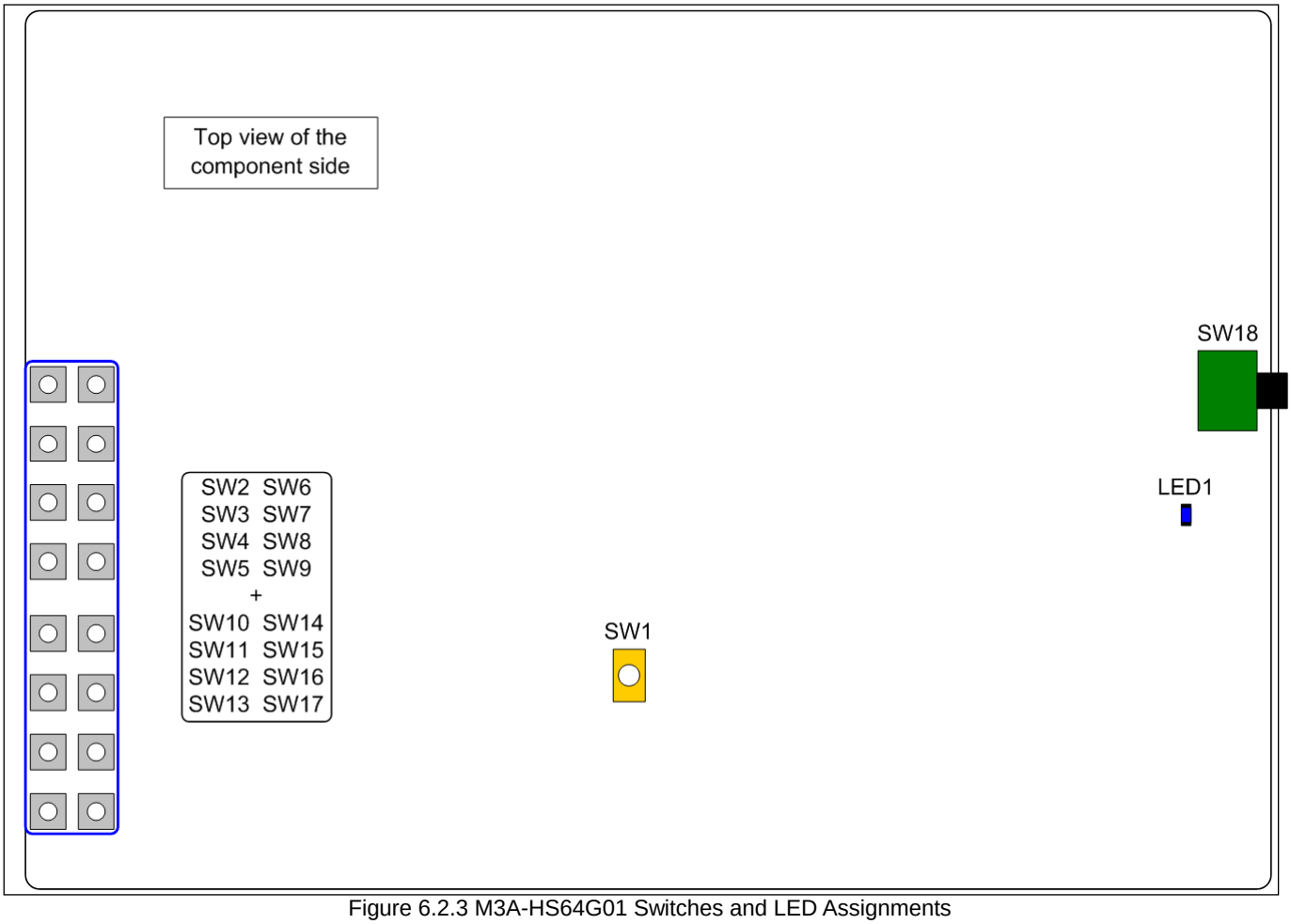


Figure 6.2.3 M3A-HS64G01 Switches and LED Assignments

The following table lists the switches mounted on the board.

Table 6.2.5 Switches

Number	Name	Remarks
SW1	LCD module connector (J12) power supply switch	Optional
SW2 to SW17	Key input switches	Refer to Section 3.10 for details
SW18	Power supply switch	-

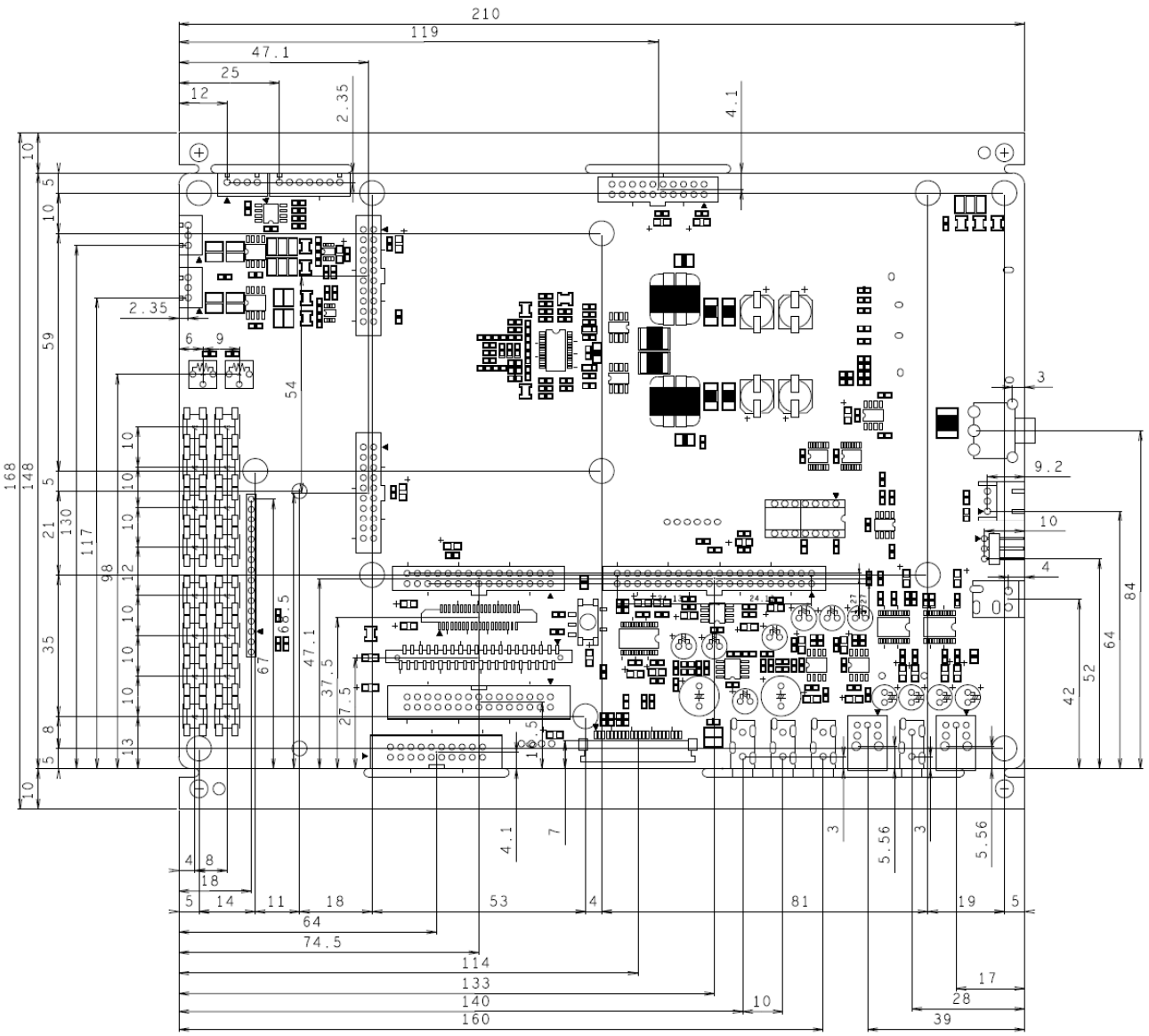
The following table lists the LED mounted on the board.

Table 6.2.6 LED

Number	Color	Description
LED1	Blue	Power supply LED (LED1 is illuminated when 12 V power is supplied)

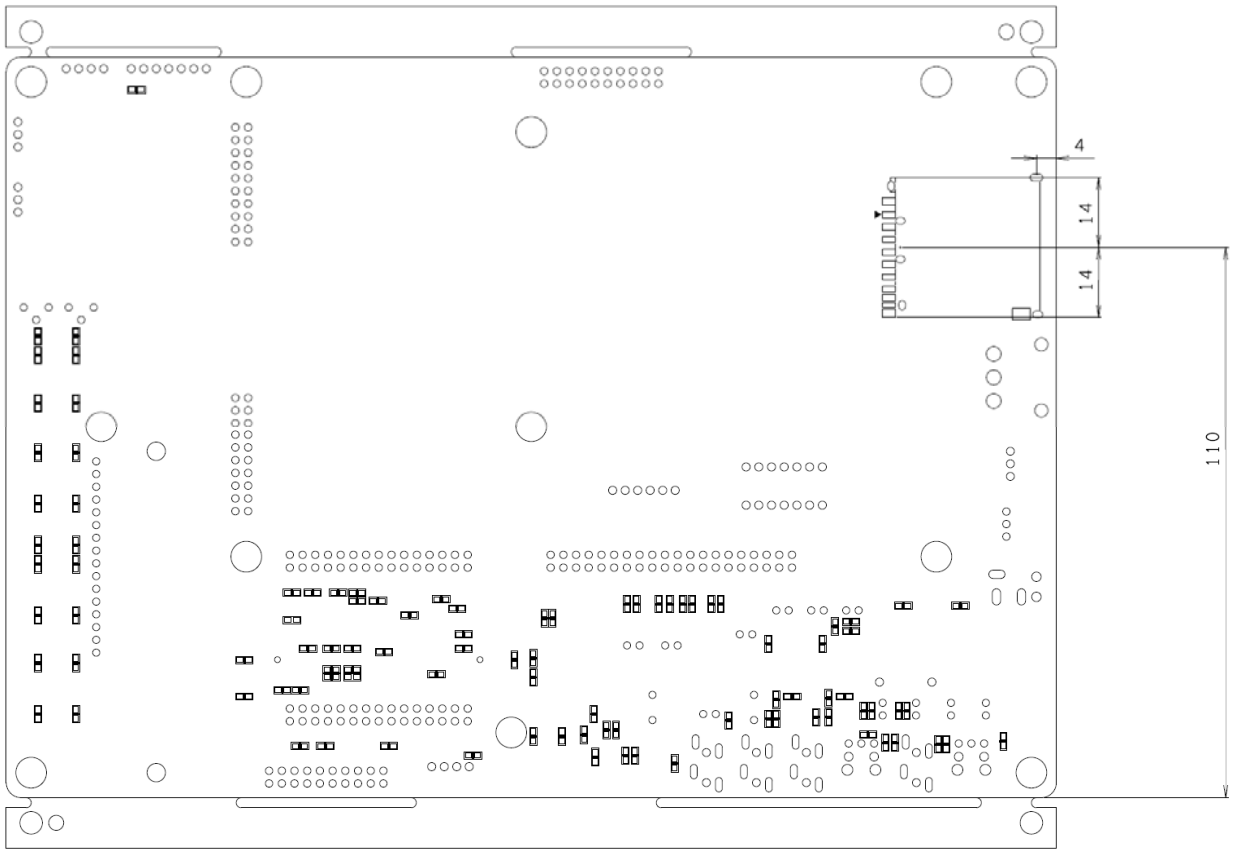
6.3 M3A-HS64G01 Dimensions

Figure 6.3.1 and Figure 6.3.2 show the M3A-HS64G01 dimensions.



Note: All measurements are in millimeters.

Figure 6.3.1 M3A-HS64G01 Dimensions (Top View of the Component Side)



Note: All measurements are in millimeters.

Figure 6.3.2 M3A-HS64G01 Dimensions (Transparent View of the Component Side)

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Chapter 7
M3A-HS64G02 Operating Specifications

7.1 M3A-HS64G02 Connectors

Figure 7.1.1 and Figure 7.1.2 show the M3A-HS64G02 connector assignments.

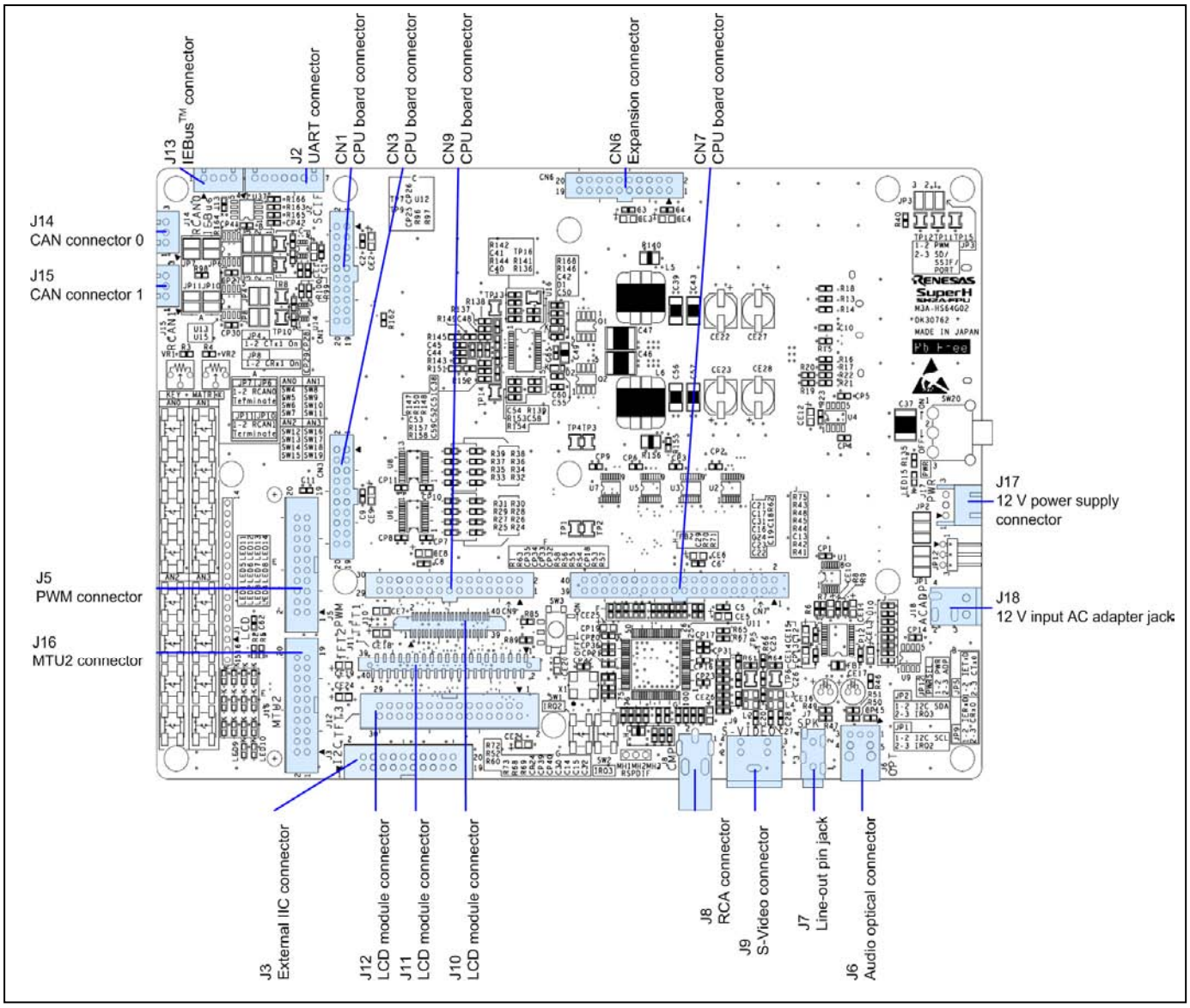


Figure 7.1.1 M3A-HS64G02 Connectors (Top View of the Component Side)

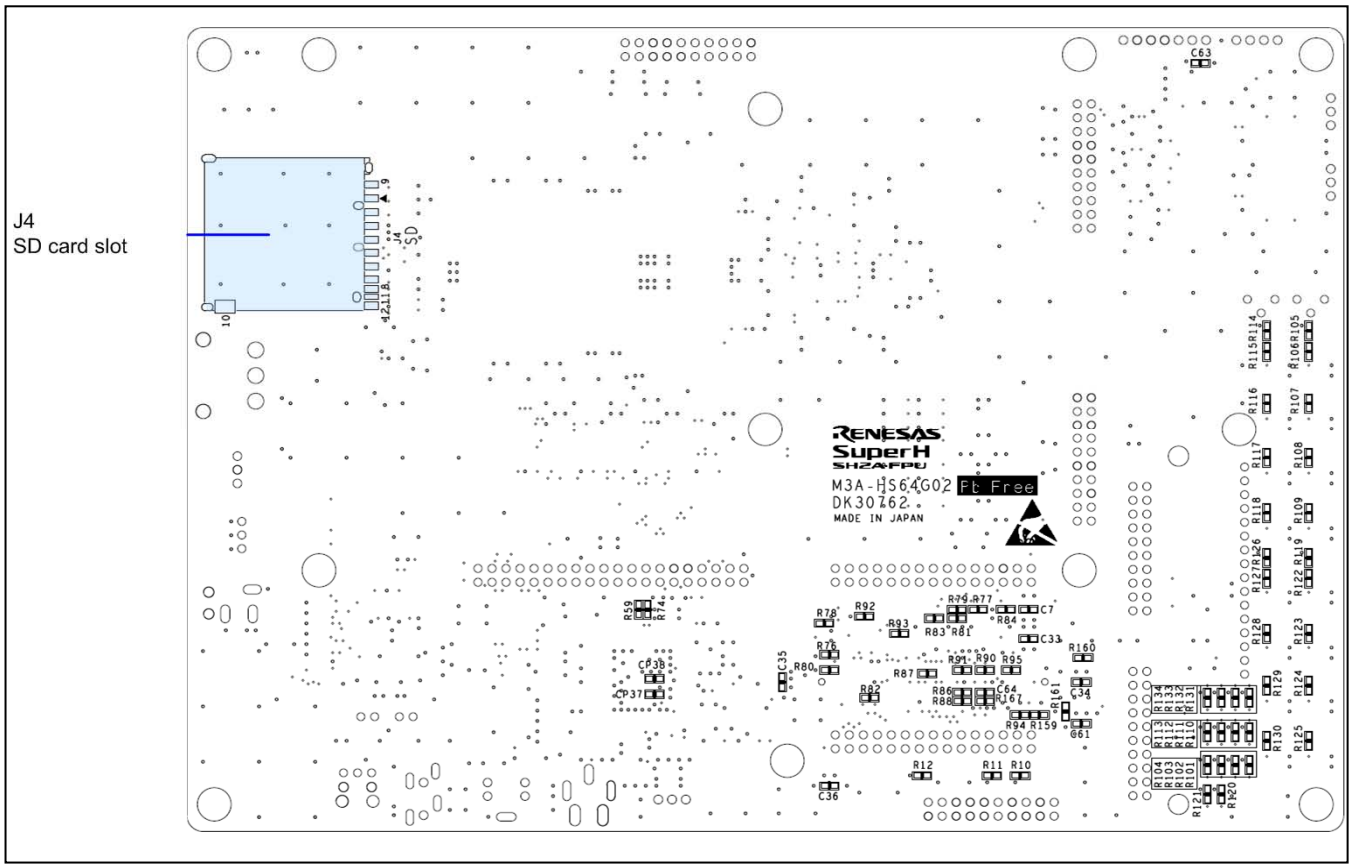


Figure 7.1.2 M3A-HS64G02 Connectors (Top View of the Solder Side)

7.1.1 CPU Board Connectors (CN1, CN3, CN6, CN7 and CN9)

The M3A-HS64G02 includes five MIL-spec connectors (CN1, CN3, CN6, CN7, and CN9) for connecting this optional board to the M3A-HS64. The following figure shows the pin assignments for CPU board connectors.

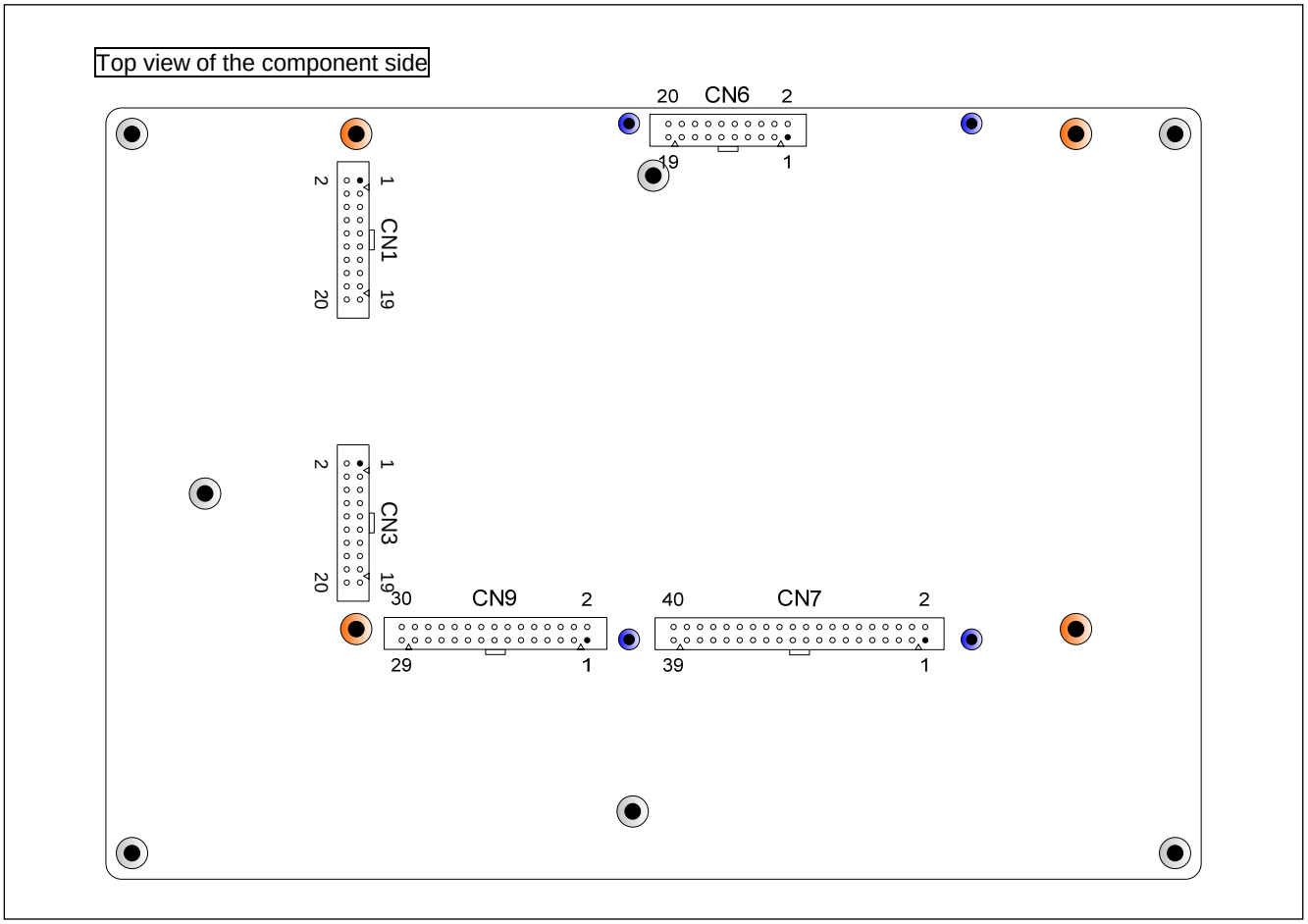


Figure 7.1.3 CPU Board Connectors Pin assignments (CN1, CN3, CN6, CN7, and CN9)

The following table lists the pin descriptions for CN1.

Table 7.1.1 CN1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PJ11/PWM2H/DACK1	2	PJ10/PWM2G/DREQ1
3	5 V	4	PJ9/PWM2F/TEND1
5	PJ8/PWM2E/RTS3#	6	3.3 V
7	PA3/MD_CLK0 (NC)	8	PA2/MD_CLK1 (NC)
9	PA1/MD_BOOT0 (NC)	10	PA0/MD_BOOT1 (NC)
11	GND	12	PJ7/TIOC1B/CTS3#
13	PJ6/TIOC1A/SCK3	14	PJ5/IERxD/TxD3
15	PJ4/IETxD/RxD3	16	GND
17	PJ3/CRx1/CRx0&CRx1/IRQ1	18	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP
19	PJ1/CRx0/IERxD/IRQ0/RxD0	20	PJ0/CTx0/IETxD/CS1#/TxD0/A0

The following table lists the pin descriptions for CN3.

Table 7.1.2 CN3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AVref (NC)	2	AVref (NC)
3	PH1/AN1	4	PH0/AN0
5	AVref (NC)	6	AVref (NC)
7	PH3/AN3	8	PH2/AN2
9	AVcc	10	AVcc
11	PH5/AN5 (NC)	12	PH4/AN4 (NC)
13	AVcc	14	AVcc
15	PH7/AN7	16	PH6/AN6 (NC)
17	AVss	18	AVss
19	AVss	20	AVss

The following table lists the pin descriptions for CN6.

Table 7.1.3 CN6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	2	5 V
3	5 V	4	5 V
5	PC0/CS0# (NC)	6	PC1/RD# (NC)
7	PC2/RDWR# (NC)	8	PC3/WE0#/DQML (NC)
9	PC4/WE1#/DQMU/WE# (NC)	10	3.3 V
11	3.3 V	12	PC9/TIOC2A
13	PC10/TIOC2B	14	PC5/RAS#/TIOC4A/IRQ4
15	PC6/CAS#/TIOC4B/IRQ5	16	PC7/CKE/TIOC4C/IRQ6
17	PC8/CS3#/TIOC4D/IRQ6	18	GND
19	GND	20	CKIO (NC)

The following table lists the pin descriptions for CN7.

Table 7.1.4 CN7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PK1/PWM1B/SD_D3	2	PK0/PWM1A/SD_D2
3	PK3/PWM1D/SD_CLK	4	PK2/PWM1C/SD_CMD
5	PE0/SCL0/AUDIO_CLK/IRQ0	6	RES#
7	PE2/SCL1/IRQ2	8	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#
9	PE4/SCL2/DV_VSYNC	10	PE3/SDA1/IRQ3
11	3.3 V	12	PE5/SDA2/DV_HSYNC
13	PK5/PWM1F/SD_D1	14	PK4/PWM1E/SD_D0
15	PK7/PWM1H/SD_CD	16	PK6/PWM1G/SD_WP
17	PF0/WAIT#/SSISCK1/DV_DATA0/SCK2/ TEND0/AUDCK	18	5 V
19	PF2/BACK#/SSIDATA1/DV_DATA2/TxD2/ DACK0/AUDATA0	20	PF1/BREQ#/SSIWS1/DV_DATA1/RxD2/ DREQ0/AUDSYNC#
21	GND	22	PF3/ICIORD#/SSISCK2/DV_DATA3/RxD3/ AUDATA1
23	PF5/CS5#/CE1A#/SSIDATA2/DV_DATA5/ TCLKC/AUDATA3	24	PF4/ICIOWR#/AH#/SSIWS2/DV_DATA4/ TxD3/AUDATA2
25	PF6/CS6#/CE1B#/SSISCK3/DV_DATA6/ TCLKB	26	GND
27	PF8/CE2B#/SSIDATA3/DV_CLK	28	PF7/CE2A#/SSIWS3/DV_DATA7/TCLKD
29	GND	30	PF9/A23/SSISCK3/RSPCK0/TIOC3A/ FRB (NC)
31	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN	32	PF10/A24/SSIWS3/SSL0/TIOC3B/ FCE# (NC)
33	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT	34	GND
35	PK9/PWM2B/SSIWS0	36	PK8/PWM2A/SSISCK0
37	PK11/PWM2D/SSITxD0	38	PK10/PWM2C/SSIRxD0
39	GND	40	AUDIO_XTAL

The following table lists the pin descriptions for CN9.

Table 7.1.5 CN9 Pin Descriptions

No.	Signal Name	No.	Signal Name
1	PG1/LCD_DATA1/SD_D3/PINT1	2	PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#
3	PG3/LCD_DATA3/SD_CLK/PINT3	4	PG2/LCD_DATA2/SD_CMD/PINT2
5	GND	6	PG4/LCD_DATA4/SD_D0/PINT4
7	PG6/LCD_DATA6/SD_WP/PINT6	8	PG5/LCD_DATA5/SD_D1/PINT5
9	PG7/LCD_DATA7/SD_CD/PINT7	10	GND
11	PG9/LCD_DATA9/SSIWS0/TxD4/SIOFSYNC	12	PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK
13	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/ SIOFTxD	14	PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/ SIOFRxD
15	GND	16	PG12/LCD_DATA12/TIOC0A/RxD1
17	PG14/LCD_DATA14/TIOC0C/SCK1	18	PG13/LCD_DATA13/TIOC0B/TxD1
19	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#	20	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
21	PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6	22	5 V
23	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7	24	PG18/LCD_DE/TIOC2A/SSL1/TxD6
25	3.3 V	26	PG20/LCD_EXTCLK/MISO1/TxD7 (NC)
27	PG22/SSL1/TIOC0B	28	PG21/RSPCK1/TIOC0A
29	PG24/MISO1/TIOC0D	30	PG23/MOSI1/TIOC0C

7.1.2 UART Connector (J2)

The M3A-HS64G02 includes a UART connector (J2) with TTL-level flow control.

The following figure shows the pin assignments for J2.

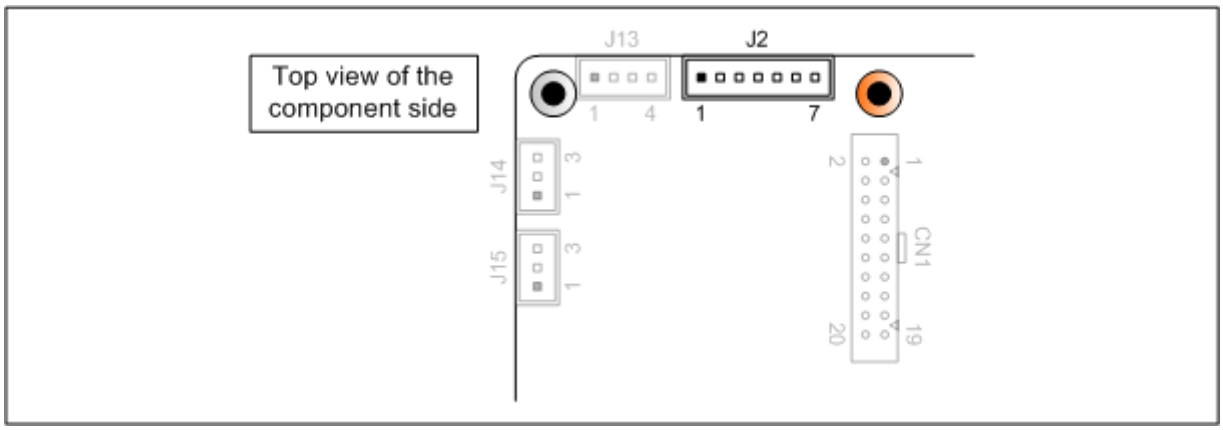


Figure 7.1.4 J2 Pin Assignments

The following table lists the pin descriptions for J2.

Table 7.1.6 J2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	5	NC
2	RXD (PJ4/IETxD/RxD3)	6	NC
3	TXD (PJ5/IERxD/TxD3)	7	GND
4	NC	-	

7.1.3 External IIC Connector (J3)

The M3A-HS64G01 includes a MIL-spec connector (J3) for connecting an external IIC interface to this optional board.

The following figure shows the pin assignments for J3.

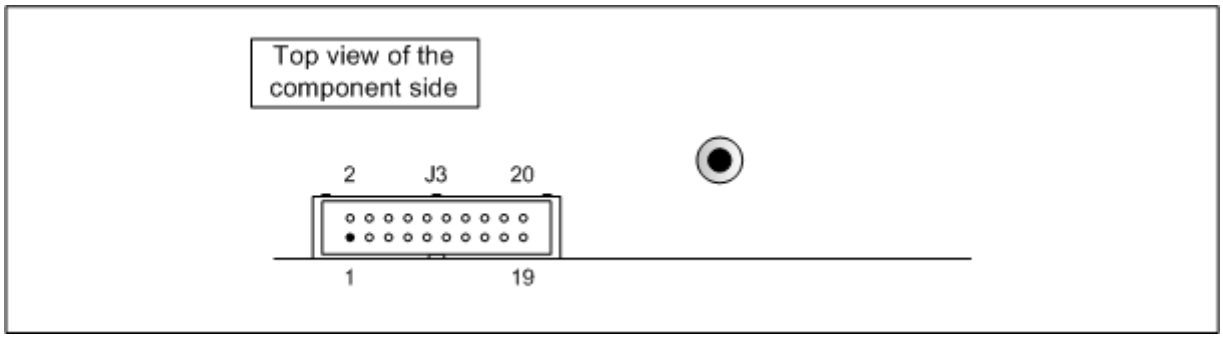


Figure 7.1.5 J3 Pin Assignments

The following table lists the pin descriptions for J3.

Table 7.1.7 J3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	2	3.3 V
3		4	
5		6	GND (See note)
7		8	
9		10	GND (See note)
11		12	
13		14	
15		16	
17	SCL (PE0/SCL0/AUDIO_CLK/IRQ0)	18	SDA (PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#)
19		20	GND (See note)

Note: For compatibility with other CPU boards, this connector is connected with the board via a 0 Ω resistor.

7.1.4 SD Card Slot (J4)

The M3A-HS64G02 includes an SD card slot (J4).

The following figure shows the pin assignments for J4.

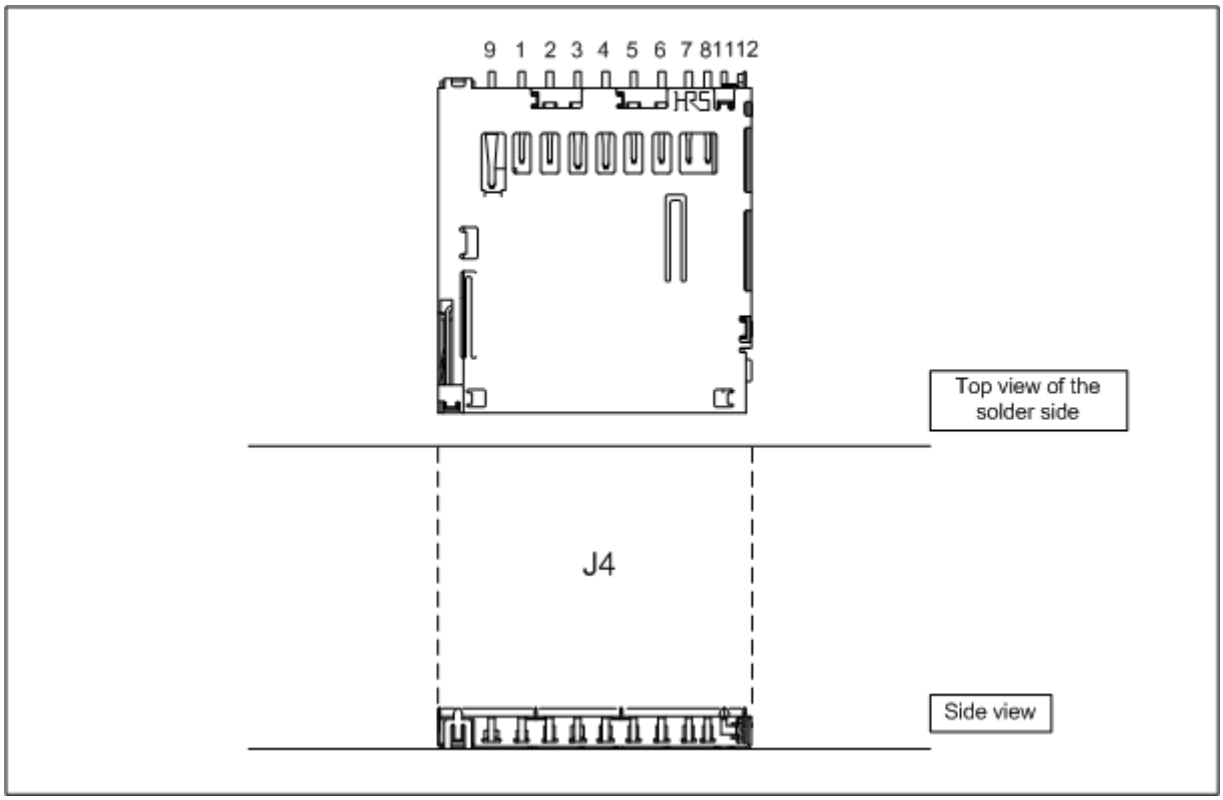


Figure 7.1.6 J4 Pin Assignments

The following table lists the pin descriptions for J4.

Table 7.1.8 J4 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	DAT3 (PK1/PWM1B/SD_D3)	7	DAT0 (PK4/PWM1E/SD_D0)
2	CMD (PK2/PWM1C/SD_CMD)	8	DAT1 (PK5/PWM1F/SD_D1)
3	GND	9	DAT2 (PK0/PWM1A/SD_D2)
4	3.3 V	10	WP (PK6/PWM1G/SD_WP)
5	CLK (PK3/PWM1D/SD_CLK)	11	CD (PK7/PWM1H/SD_CD)
6	GND	12	COMMON (GND)

7.1.5 PWM Connector (J5)

The M3A-HS64G02 includes one MIL-spec connector (J5) for PWM output.

The following figure shows the pin assignments for J5.

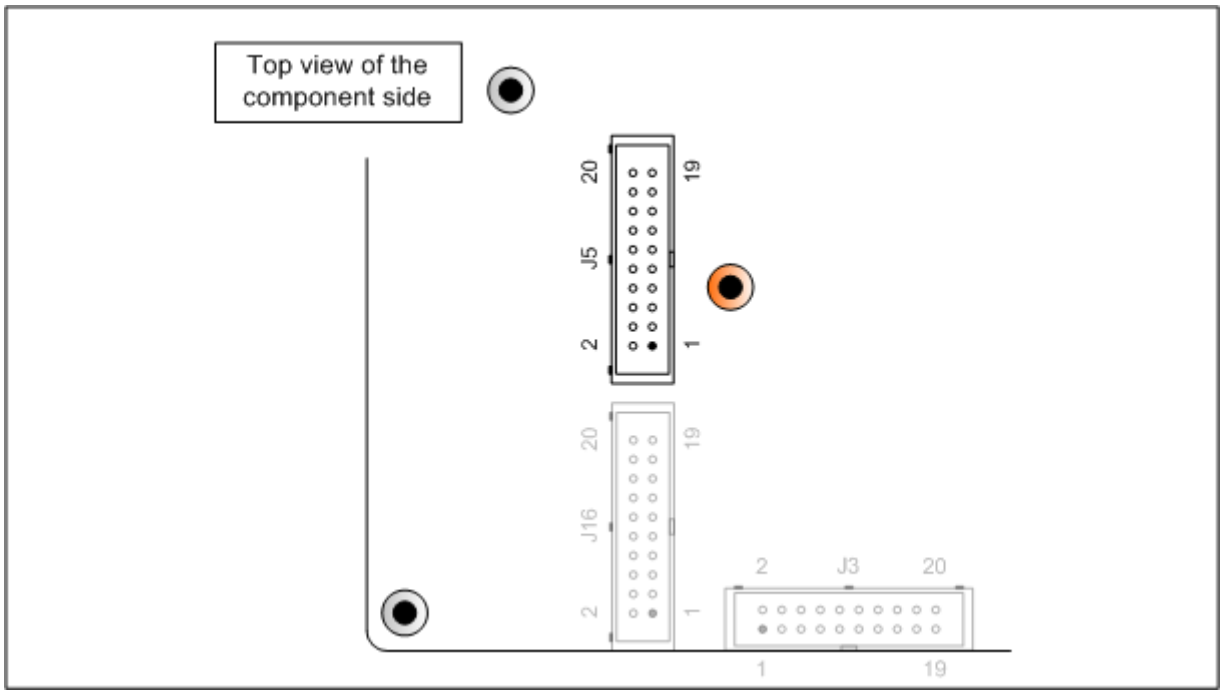


Figure 7.1.7 J5 Pin Assignments

The following table lists the pin descriptions for J5.

Table 7.1.9 J5 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PK0/PWM1A/SD_D2	2	PK1/PWM1B/SD_D3
3	PK2/PWM1C/SD_CMD	4	PK3/PWM1D/SD_CLK
5	PK4/PWM1E/SD_D0	6	PK5/PWM1F/SD_D1
7	PK6/PWM1G/SD_WP	8	PK7/PWM1H/SD_CD
9	GND	10	GND
11	PK8/PWM2A/SSISCK0	12	PK9/PWM2B/SSIWS0
13	PK10/PWM2C/SSIRxD0	14	PK11/PWM2D/SSITxD0
15	PJ8/PWM2E/RTS3#	16	PJ9/PWM2F/TEND1
17	PJ10/PWM2G/DREQ1	18	PJ11/PWM2H/DACK1
19	5 V	20	5 V

7.1.6 Audio Optical Connector (J6)

The M3A-HS64G02 includes an audio optical connector (J6).

The following figure shows the pin assignments for J6.

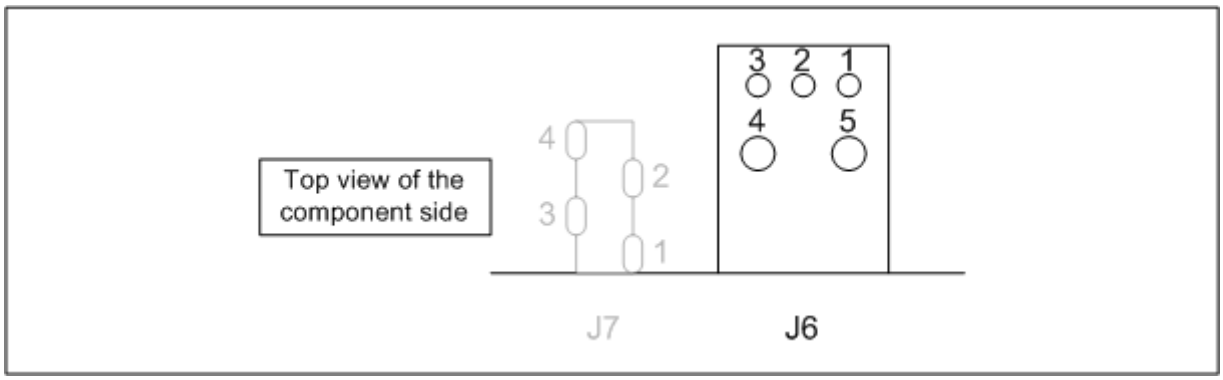


Figure 7.1.8 J6 Pin Assignments

The following table lists the pin descriptions for J6.

Table 7.1.10 J6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	4	NC
2	3.3 V	5	NC
3	TX (An optical output pin of the D/A converter)	-	

7.1.7 Line-out Pin Jack (J7)

The M3A-HS64G02 includes a line-out pin jack (J7).

The following figure shows the pin assignments for J7.

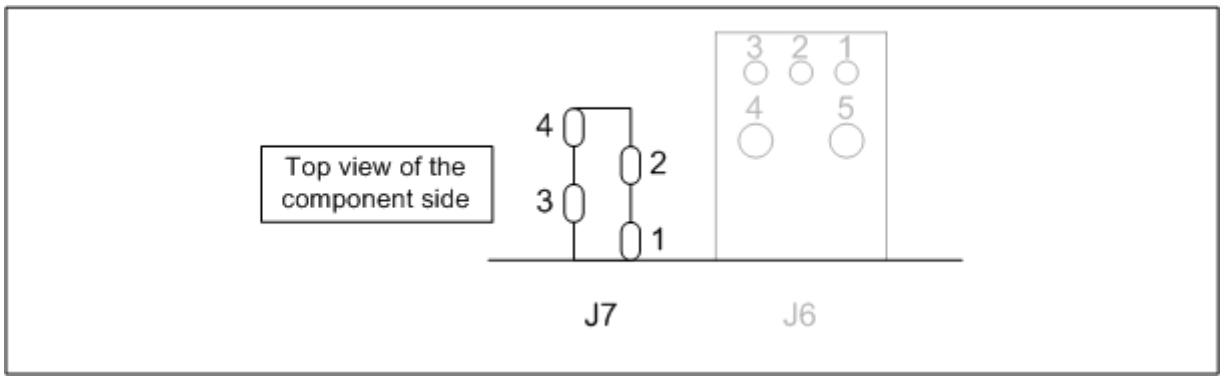


Figure 7.1.9 J7 Pin Assignments

The following table lists the pin descriptions for J7.

Table 7.1.11 J7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AOUTR (An analog output R pin of the D/A converter)
2	AOUTL (An analog output L pin of the D/A converter)	4	NC

7.1.8 RCA Connector (J8)

The M3A-HS64G02 includes an RCA connector (J8).

The following figure shows the pin assignments for J8.

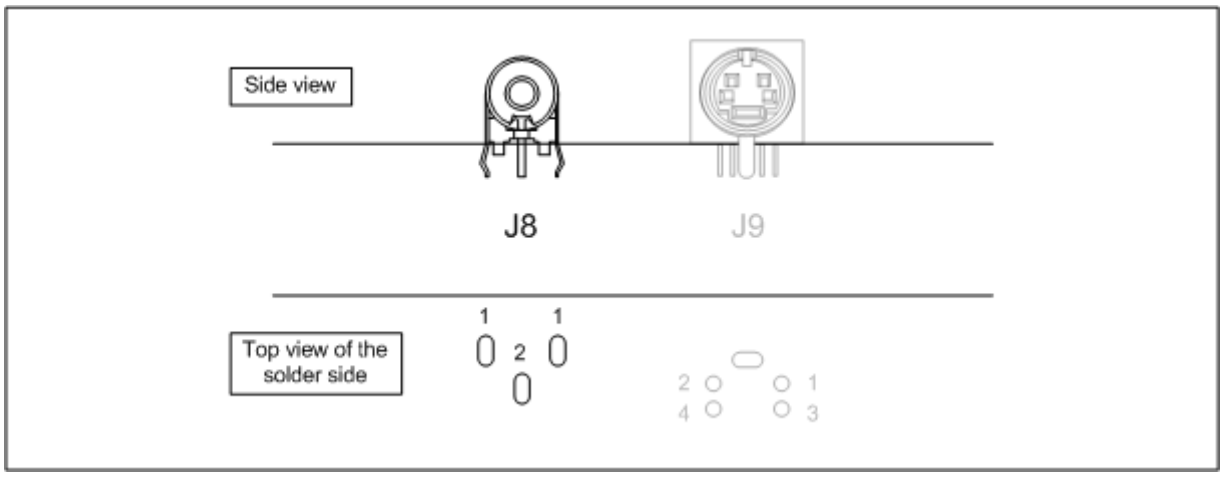


Figure 7.1.10 J8 Pin Assignments

The following table lists the pin descriptions for J8.

Table 7.1.12 J8 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	AIN2 (An analog input pin of the video decoder)

7.1.9 S-Video Connector (J9)

The M3A-HS64G02 includes an S-Video connector (J9).

The following figure shows the pin assignments for J9.

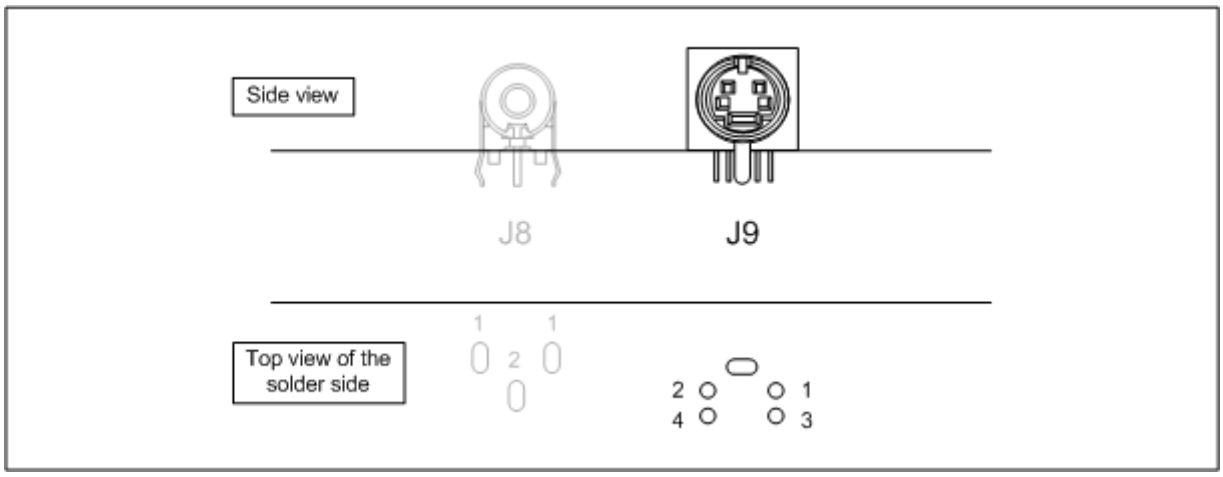


Figure 7.1.11 J9 Pin Assignments

The following table lists the pin descriptions for J9.

Table 7.1.13 J9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	GND
3	AIN2 (An analog input pin of the video decoder)	4	AIN5 (An analog input pin of the video decoder)

7.1.10 LCD Module Connectors (J10 to J12)

The M3A-HS64G02 includes two flexible connectors (J10 and J11), and one MIL-spec connector (J12) for connecting an LCD module to this optional board.

The following figure shows the pin assignments for LCD module connectors.

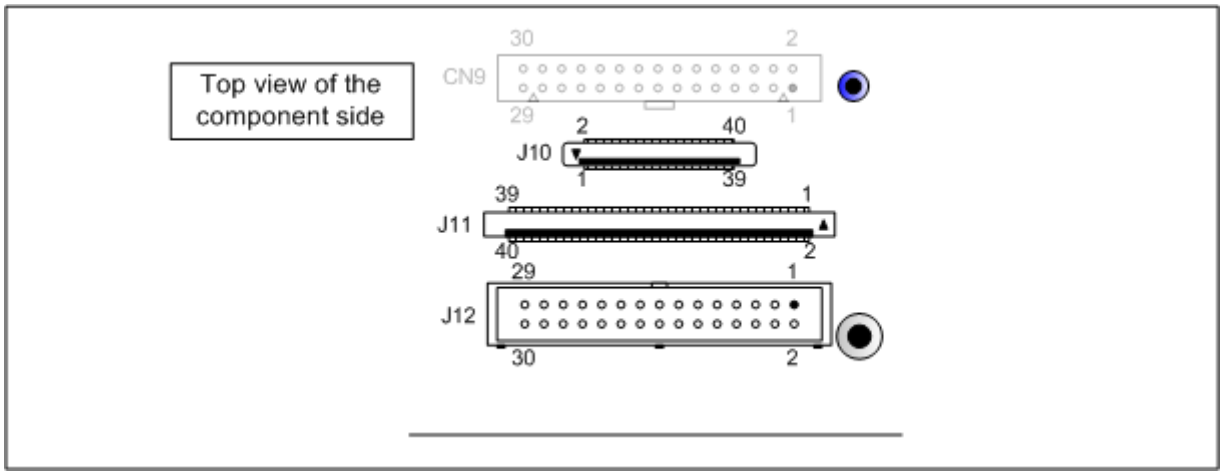


Figure 7.1.12 LCD Module Connectors Pin Assignments (J10 to J12)

The following table lists the pin descriptions for J10.

Table 7.1.14 J10 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	2	3.3 V
3	3.3 V	4	DCLK (PG19/LCD_CLK/TIOC2B/MOSI1/RxD7)
5	GND	6	HSYNC (PG17/LCD_HSYNC/TIOC1B/RSPCK1/RxD6)
7	GND	8	DTMG (PG18/LCD_DE/TIOC2A/SSL1/TxD6)
9	GND	10	NC
11	GND	12	R5 (PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#)
13	R4 (PG14/LCD_DATA14/TIOC0C/SCK1)	14	R3 (PG13/LCD_DATA13/TIOC0B/TxD1)
15	GND	16	R2 (PG12/LCD_DATA12/TIOC0A/RxD1)
17	R1 (PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)	18	R0 (PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)
19	GND	20	G5 (PG10/LCD_DATA10/SSIRxD0/IRQ2/ RxD5/SIOFRxD)
21	G4 (PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC)	22	G3 (PG8/LCD_DATA8/SSISCK0/RxD4/ SIOFSCK)
23	GND	24	G2 (PG7/LCD_DATA7/SD_CD/PINT7)
25	G1 (PG6/LCD_DATA6/SD_WP/PINT6)	26	G0 (PG5/LCD_DATA5/SD_D1/PINT5)
27	GND	28	B5 (PG4/LCD_DATA4/SD_D0/PINT4)
29	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)	30	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)
31	GND	32	B2 (PG1/LCD_DATA1/SD_D3/PINT1)
33	B1 (PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#)	34	B0 (PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#)
35	PCI (Inputs 3.3 V or GND by a toggle switch)	36	Vctrl (3.3 V)
37	NC	38	NC
39	NC	40	NC

The following table lists the pin descriptions for J11.

Table 7.1.15 J11 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	2	DTMG (PG18/LCD_DE/TIOC2A/SSL1/ TxD6)
3	HREV (3.3 V or GND)	4	B5 (PG4/LCD_DATA4/SD_D0/PINT4)
5	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)	6	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)
7	B2 (PG1/LCD_DATA1/SD_D3/PINT1)	8	B1 (PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#)
9	B0 (PG0/LCD_DATA0/SD_D2/PINT0/ WDTOVF#)	10	3.3 V
11	3.3 V	12	G5 (PG10/LCD_DATA10/SSIRxD0/IRQ2/ RxD5/SIOFRxD)
13	G4 (PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC)	14	G3 (PG8/LCD_DATA8/SSISCK0/RxD4/ SIOFSCK)
15	G2 (PG7/LCD_DATA7/SD_CD/PINT7)	16	G1 (PG6/LCD_DATA6/SD_WP/PINT6)
17	G0 (PG5/LCD_DATA5/SD_D1/PINT5)	18	GND
19	R5(PG15/LCD_DATA15/TIOC0D/RxD3/ RTS1#)	20	R4 (PG14/LCD_DATA14/TIOC0C/SCK1)
21	R3(PG13/LCD_DATA13/TIOC0B/TxD1)	22	R2(PG12/LCD_DATA12/TIOC0A/RxD1)
23	R1(PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)	24	R0 (PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)
25	VREV (3.3 V or GND)	26	NC
27	NC	28	GND
29	DCLK (PG19/LCD_CLK/TIOC2B/MOSI1/ RxD7)	30	GND
31	GND	32	GND
33	GND	34	GND
35	TMZ (PH7/AN7)	36	GND
37	DIM (PG21/TIOC0A)	38	NC
39	5 V	40	5 V

The following table lists the pin descriptions for J12.

Table 7.1.16 J12 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	2	3.3 V
3	3.3 V	4	PG15/LCD_DATA15/TIOC0D/RxD3/RTS1#
5	PG14/LCD_DATA14/TIOC0C/SCK1	6	PG13/LCD_DATA13/TIOC0B/TxD1
7	PG12/LCD_DATA12/TIOC0A/RxD1	8	PG11/LCD_DATA11/SSITxD0/IRQ3/TxD5/ SIOFTxD
9	PG10/LCD_DATA10/SSIRxD0/IRQ2/RxD5/ SIOFRxD	10	PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC
11	PG8/LCD_DATA8/SSISCK0/RxD4/SIOFSCK	12	PG7/LCD_DATA7/SD_CD/PINT7
13	PG6/LCD_DATA6/SD_WP/PINT6	14	PG5/LCD_DATA5/SD_D1/PINT5
15	PG4/LCD_DATA4/SD_D0/PINT4	16	PG3/LCD_DATA3/SD_CLK/PINT3
17	PG2/LCD_DATA2/SD_CMD/PINT2	18	PG1/LCD_DATA1/SD_D3/PINT1
19	PG0/LCD_DATA0/SD_D2/PINT0/WDTOVF#	20	GND
21	PG19/LCD_CLK/TIOC2B/MOSI1/RxD7	22	PG17/LCD_HSYNC/TIOC1B/RSPCK1/ RxD6
23	NC (LCD_VCPWC)	24	NC (Allowed to supply 5 V through 0 Ω resistor)
25	PG16/LCD_VSYNC/TIOC1A/TxD3/CTS1#	26	PG18/LCD_DE/TIOC2A/SSL1/TxD6
27	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP	28	GND
29	GND	30	GND

7.1.11 IEBus™ Connector (J13)

The M3A-HS64G02 includes an IEBus™ connector (J13).

The following figure shows the pin assignments for J13.

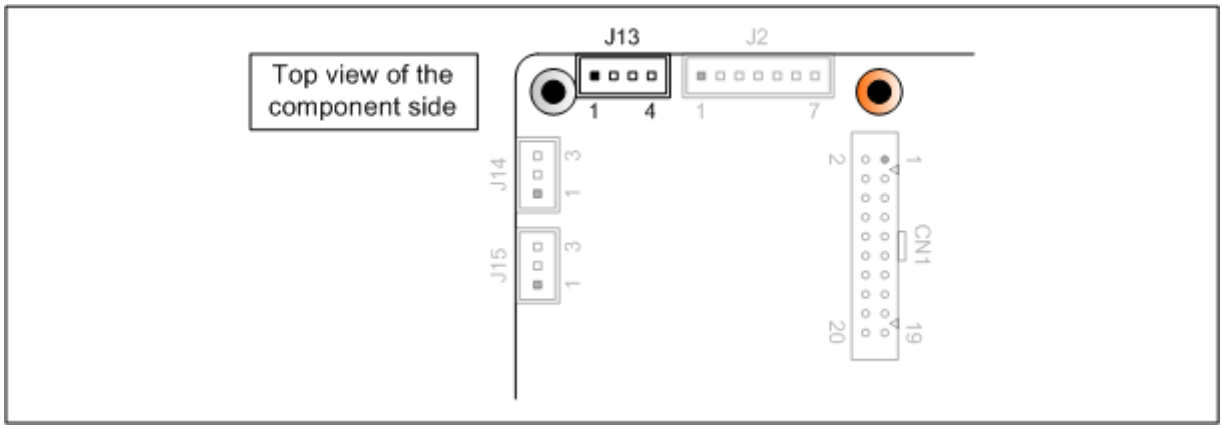


Figure 7.1.13 J13 Pin Assignments

The following table lists the pin descriptions for J13.

Table 7.1.17 J13 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	3	BUS+
2	BUS-	4	GND

7.1.12 CAN Connectors (J14 and J15)

The M3A-HS64G02 includes two CAN connectors (J14 and J15).

The following figure shows the pin assignments for J14 and J15.

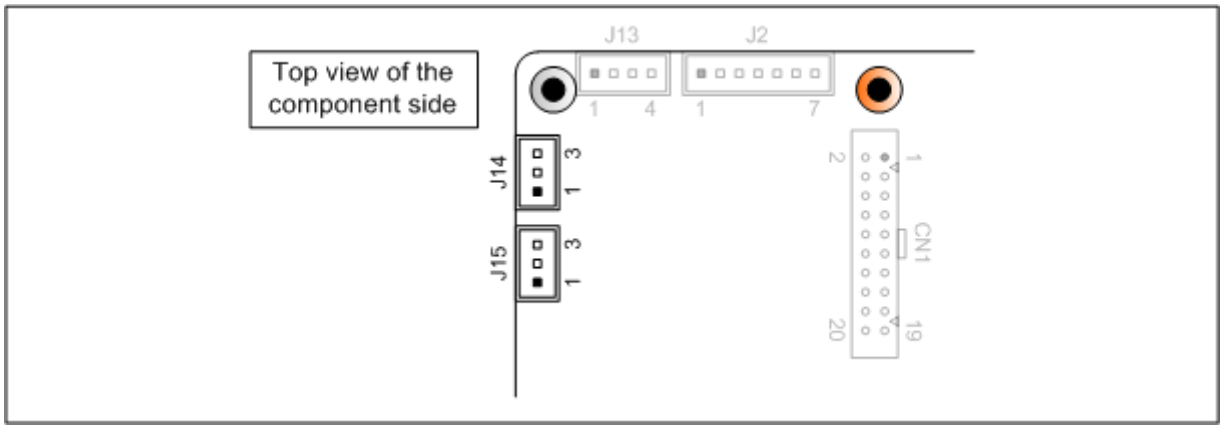


Figure 7.1.14 J14, J15 Pin Assignments

The following table lists the pin descriptions for J14 and J15.

Table 7.1.18 J14, J15 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	CANH	3	GND
2	CANL	-	

J14 and J15 are connected to channel 0 (CTx0/CRx0) and channel 1 (CTx1/CRx1), respectively.

7.1.13 MTU2 Connector (J16)

The M3A-HS64G02 includes a MIL-spec connector (J16) for MTU2 output.

The following figure shows the pin assignments for J16.

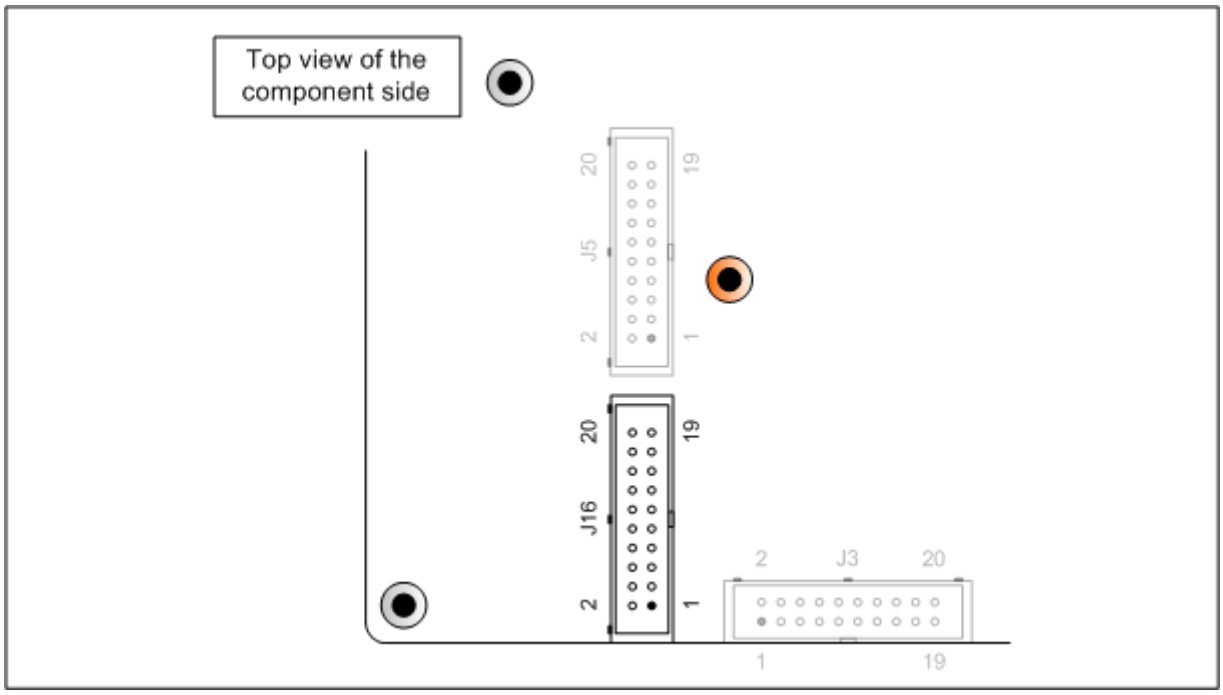


Figure 7.1.15 Pin Assignments for MTU2 Connector (J16)

The following table lists the pin descriptions for J16.

Table 7.1.19 J16 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN	2	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
3	GND	4	GND
5	PG22/SSL1/TIOC0B	6	PG24/MISO1/TIOC0D
7	PG21/RSPCK1/TIOC0A	8	PG23/MOSI1/TIOC0C
9	GND	10	GND
11	PJ6/TIOC1A/SCK3	12	PJ7/TIOC1B/CTS3#
13	GND	14	GND
15	PC7/CKE/TIOC4C/IRQ6	16	PC8/CS3#/TIOC4D/IRQ6
17	PC5/RAS#/TIOC4A/IRQ4	18	PC6/CAS#/TIOC4B/IRQ5
19	PC9/TIOC2A	20	PC10/TIOC2B

7.1.14 12 V Power Supply Connector (J17)

The M3A-HS64G02 includes a system power supply connector (J17). The number of pins of this connector differs from the power supply connector mounted on the M3A-HS64 to prevent improper insertion.

The following figure shows the pin assignments for J17.

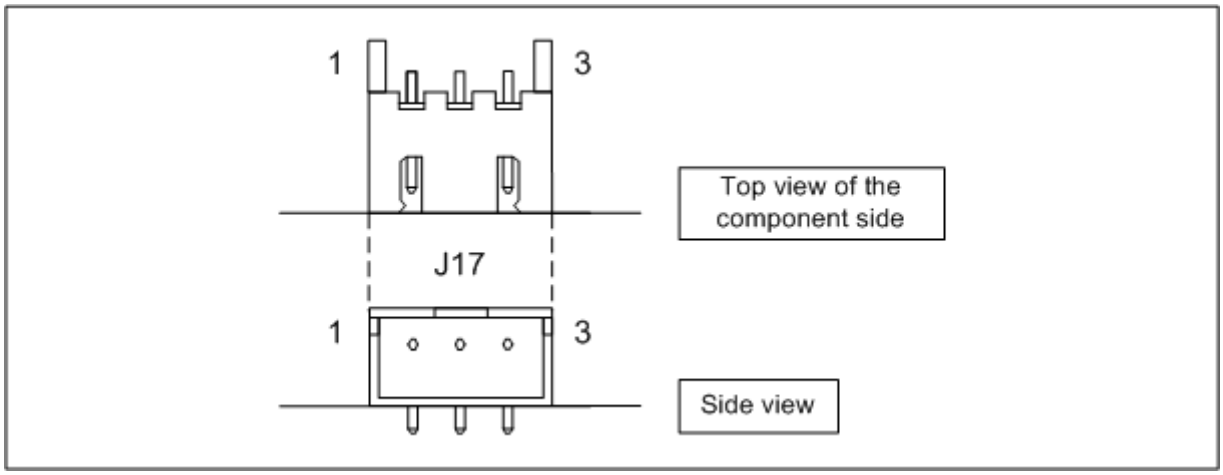


Figure 7.1.16 J17 Pin Assignments

The following table lists the pin descriptions for J17.

Table 7.1.20 J17 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	12 V	3	GND
2	NC	-	

7.1.15 12 V Input AC Adapter Jack (J18)

The M3A-HS64G02 includes an AC adapter jack (J18) for 12 V DC input.

The following figure shows the pin assignments for J18.

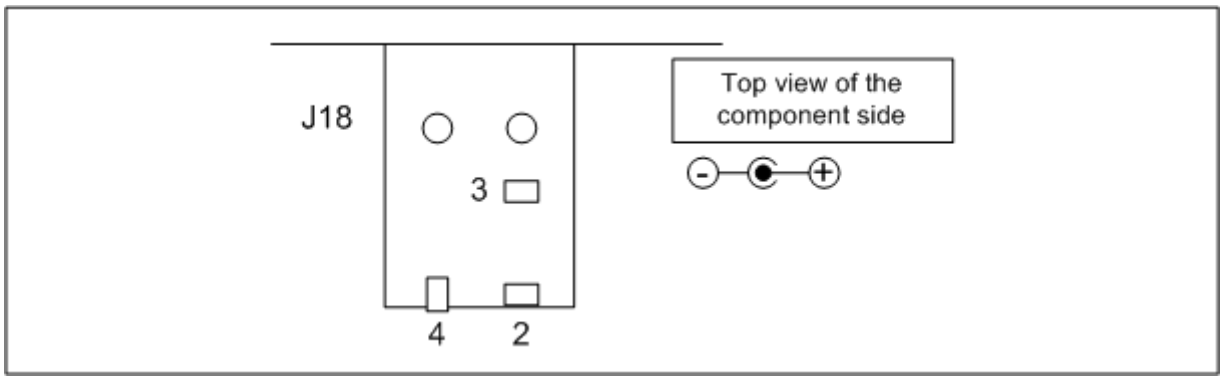


Figure 7.1.17 J18 Pin Assignments

The following table lists the pin descriptions for J18.

Table 7.1.21 J18 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC (No pins)	2	12 V
3	GND	4	GND

7.2 M3A-HS64G02 Operating Components

The following figure shows the assignments of the M3A-HS64G02 operating components.

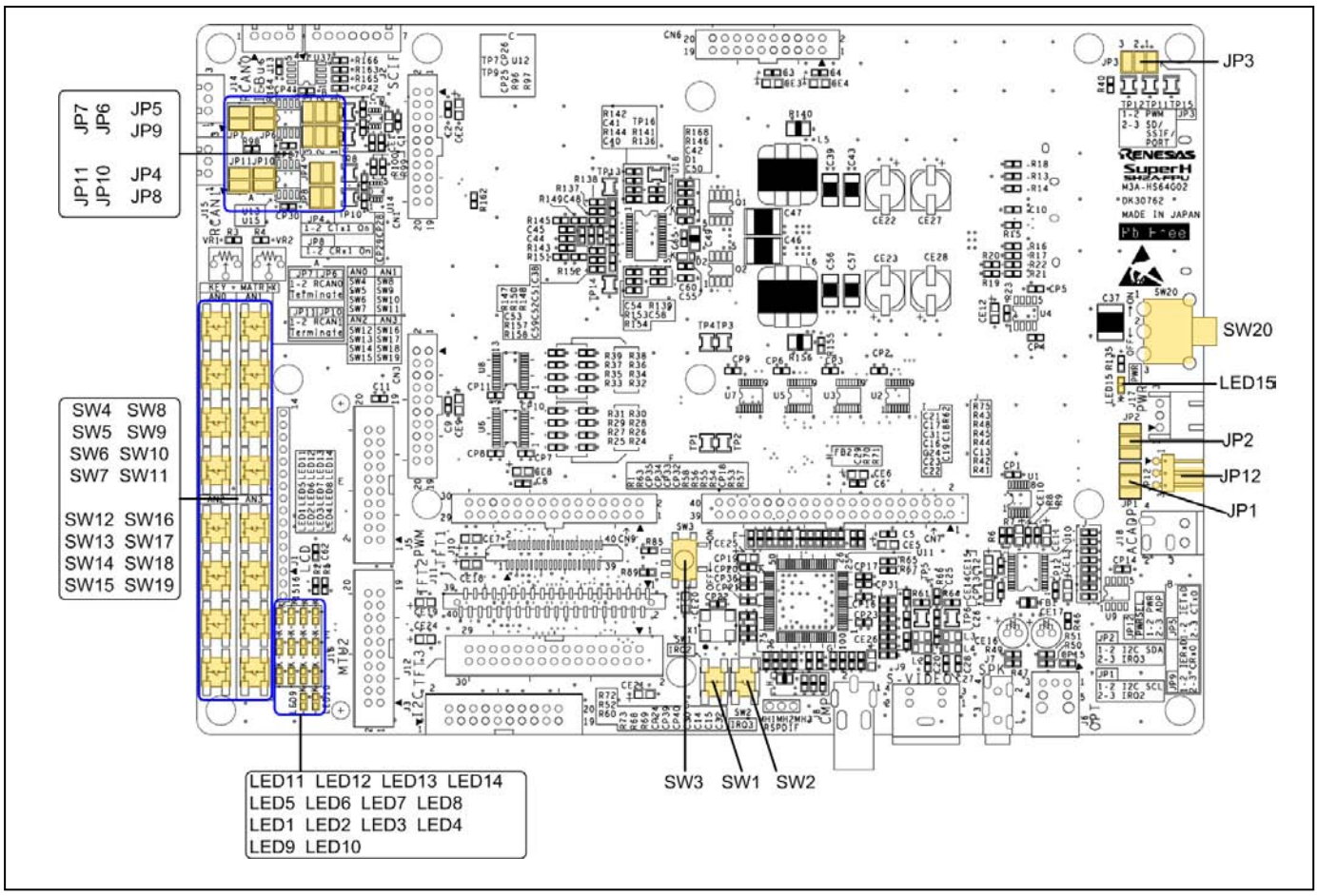


Figure 7.2.1 M3A-HS64G02 Operating Components (Top View of the Component Side)

7.2.1 Jumpers (JP1 to JP12)

The M3A-HS64G02 includes 12 jumpers. The following figure shows jumper assignments (JP1 to JP12) on the M3A-HS64G02.

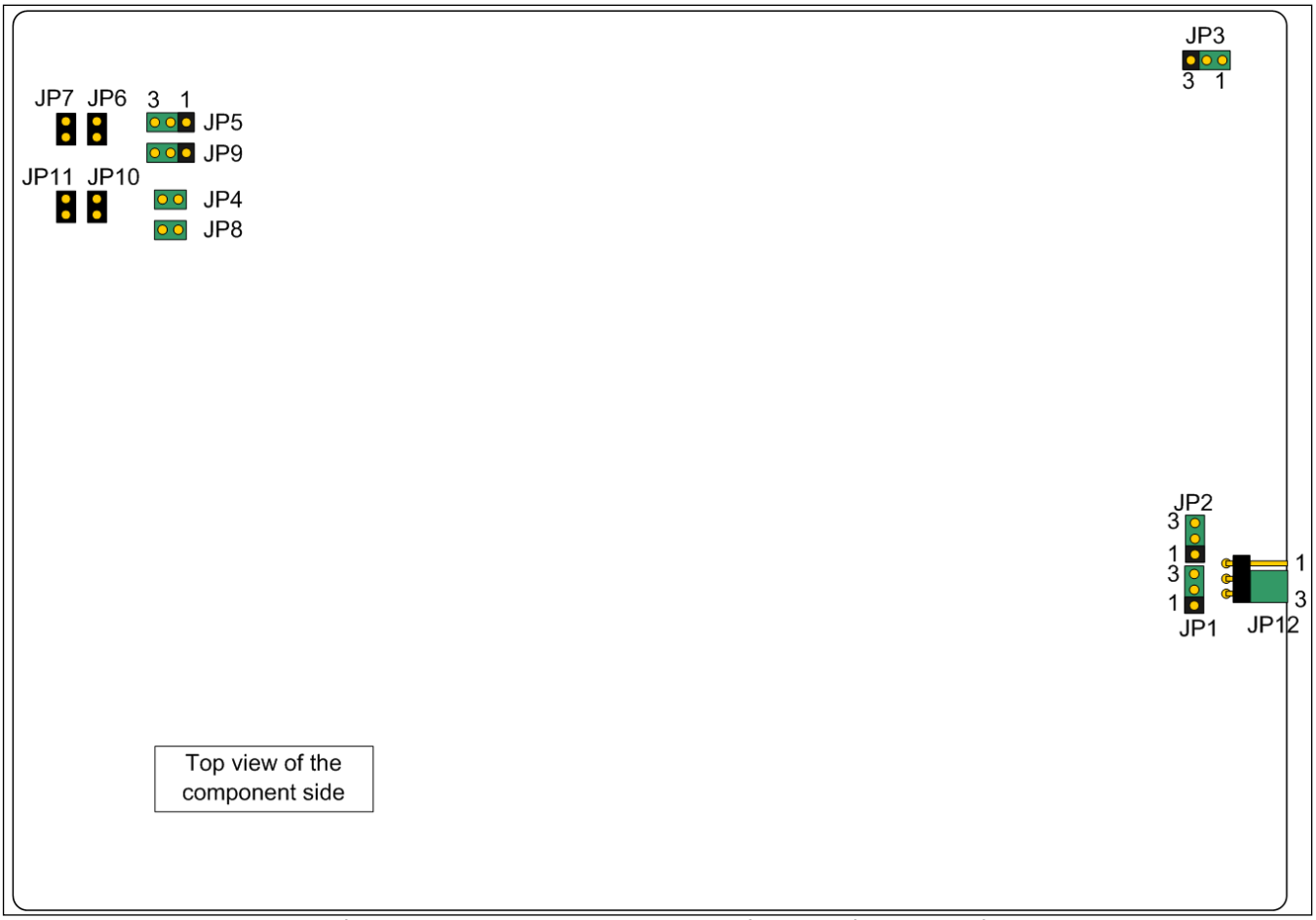


Figure 7.2.2 M3A-HS64G02 Jumper Assignments (JP1 to JP12)

The following table lists the jumpers setting for JP1, JP2, JP3, JP5, and JP9.

Table 7.2.1 Multi-function Pin Switch Jumpers Setting (JP1, JP2, JP3, JP5, and JP9)

Number	Setting	Description
JP1	1 - 2	Connects the D/A converter (U10) as the SCL1 output pin
SCL1/IRQ2	2 - 3	Connects the push-button switch (SW1) as the IRQ2 input pin
JP2	1 - 2	Connects the D/A converter (U10) as the SDA1 I/O pin
SDA1/IRQ3	2 - 3	Connects the push-button switch (SW2) as the IRQ3 input pin
JP3	1 - 2	Connects the MIL-spec connector (J5) as the PWM data output pin
PWM/ (SD/SSIF/PORT)	2 - 3	Connects the SD card slot (J4), DAC (U10), and test pins (TP1 to TP4) as the SDHI, SSIF, and PORT I/O pins
JP5	1 - 2	Connects the IEBus™ driver (U37) as the IETxD output pin
IETxD/CTx0	2 - 3	Connects the CAN driver (U13) as the CTx0 output pin
JP9	1 - 2	Connects the IEBus™ driver (U37) as the IERxD input pin
IERxD/CRx0	2 - 3	Connects the CAN driver (U13) as the CRx0 input pin

Table 7.2.2 CAN Evaluation Jumper Setting (JP4, JP6, JP7, JP8, JP10, and JP11)

Number	Setting	Description
JP4 Connects CTx1	1 - 2	Connects the CTx1 pin to the CAN driver (U16)
	Open	Leaves the CTx1 pin disconnected to the CAN driver (U16)
JP8 Connects CRx1	1 - 2	Connects the CRx1 pin to the CAN driver (U16)
	Open	Leaves the CRx1 pin disconnected to the CAN driver (U16)
JP6 Terminates CANL (ch0)	1 - 2	Terminates the CANL (ch0) pin
	Open	Leaves the CANL (ch0) pin not terminated
JP7 Terminates CANH (ch0)	1 - 2	Terminates the CANH (ch0) pin
	Open	Leaves the CANH (ch0) pin not terminated
JP10 Terminates CANL (ch1)	1 - 2	Terminates the CANL (ch1) pin
	Open	Leaves the CANL (ch1) pin not terminated
JP11 Terminates CANH (ch1)	1 - 2	Terminates the CANH (ch1) pin
	Open	Leaves the CANH (ch1) pin not terminated

Table 7.2.3 Power Supply Switch Jumper Setting (JP12)

Number	Setting	Description
JP12 PWRSEL	1 - 2	Supplies the system power from J17
	2 - 3	Supplies the system power from J18 (AC adapter is used)

Notes:

1. The shaded row shows the default setting.
2. Do not change the jumper settings while the M3A-HS64G02 is ON. Be sure to turn the power OFF before changing the settings.

7.2.2 Switches and LEDs

The M3A-HS64G02 includes 20 switches and 15 LEDs. The following figure shows assignments of switches and LEDs.

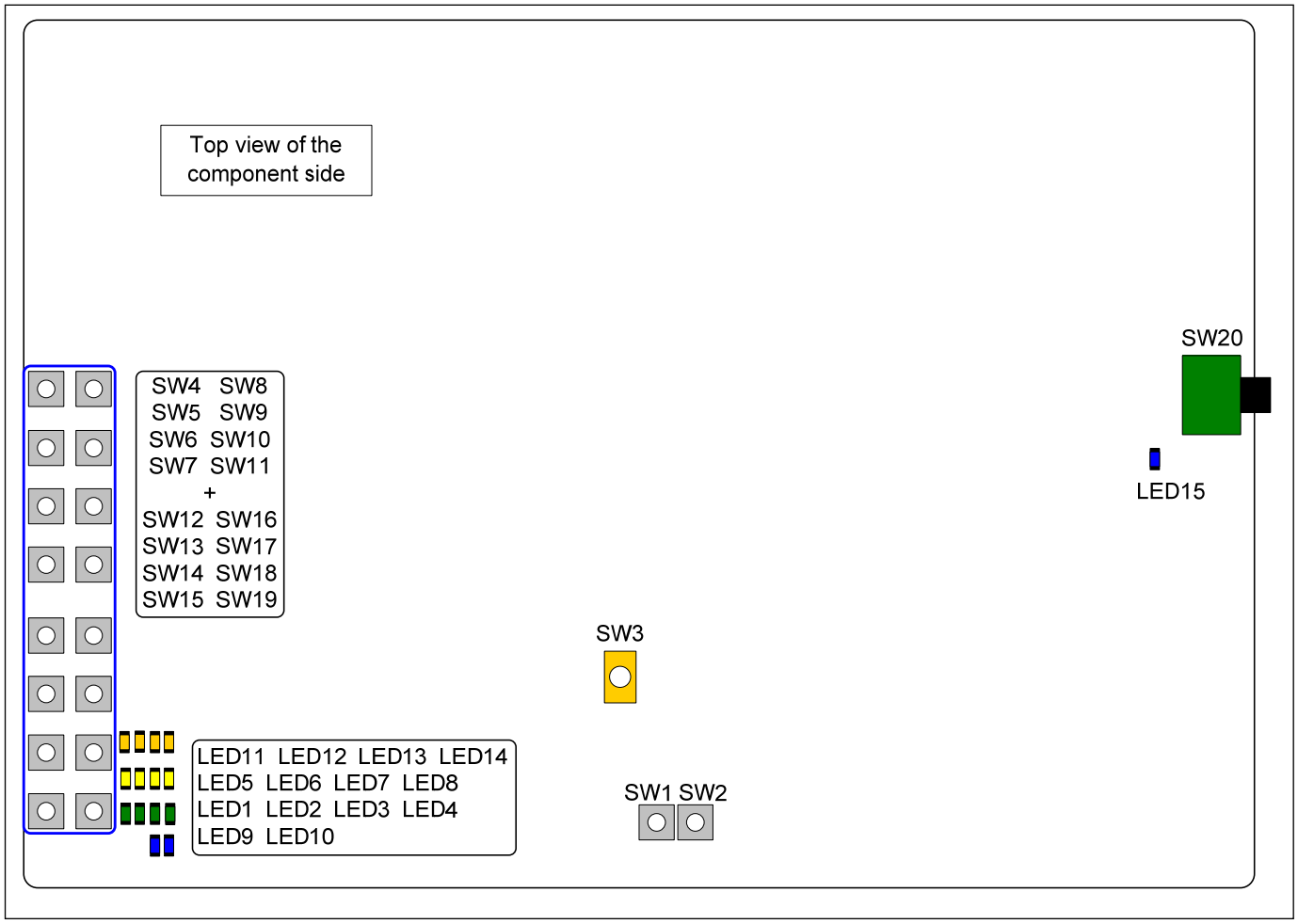


Figure 7.2.3 M3A-HS64G02 Switches and LEDs Assignments

The following table lists switches mounted on the M3A-HS64G02.

Table 7.2.4 M3A-HS64G02 Switches

Number	Name	Remarks
SW1	IRQ2 switch	Refer to Section 4.13 for details.
SW2	IRQ3 switch	Refer to Section 4.13 for details.
SW3	LCD module connector (J10) power supply switch	Optional
SW4 to SW19	Key input switches	Refer to Section 4.12 for details.
SW20	Power supply switch	-

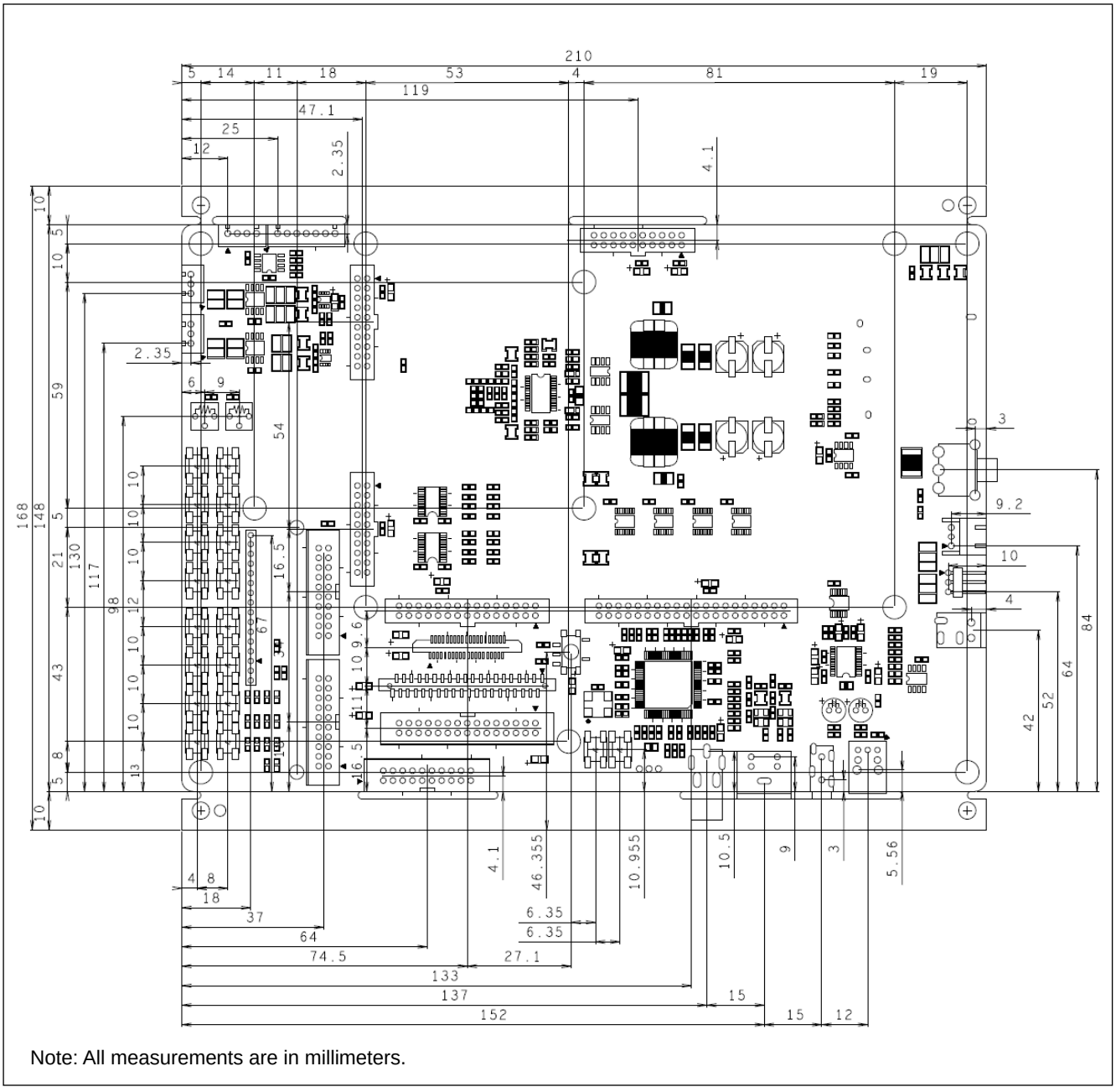
The following table lists LEDs mounted on the M3A-HS64G02.

Table 7.2.5 M3A-HS64G02 LEDs

Number	Color	Description
LED1 to LED4	Green	Brightness-control LEDs (MTU2 output pins: TIOC0A to 0D are connected)
LED5 to LED8	Yellow	Brightness-control LEDs (MTU2 output pins: TIOC1A, 1B, TIOC2A, and 2B are connected)
LED9 and LED10	Blue	Brightness-control LEDs (MTU2 output pins: TIOC3C and 3D are connected)
LED11 to LED14	Orange	Brightness-control LEDs (MTU2 output pins: TIOC4A to 4D are connected)
LED15	Blue	Power supply LED (LED15 is illuminated when 12 V power is supplied)

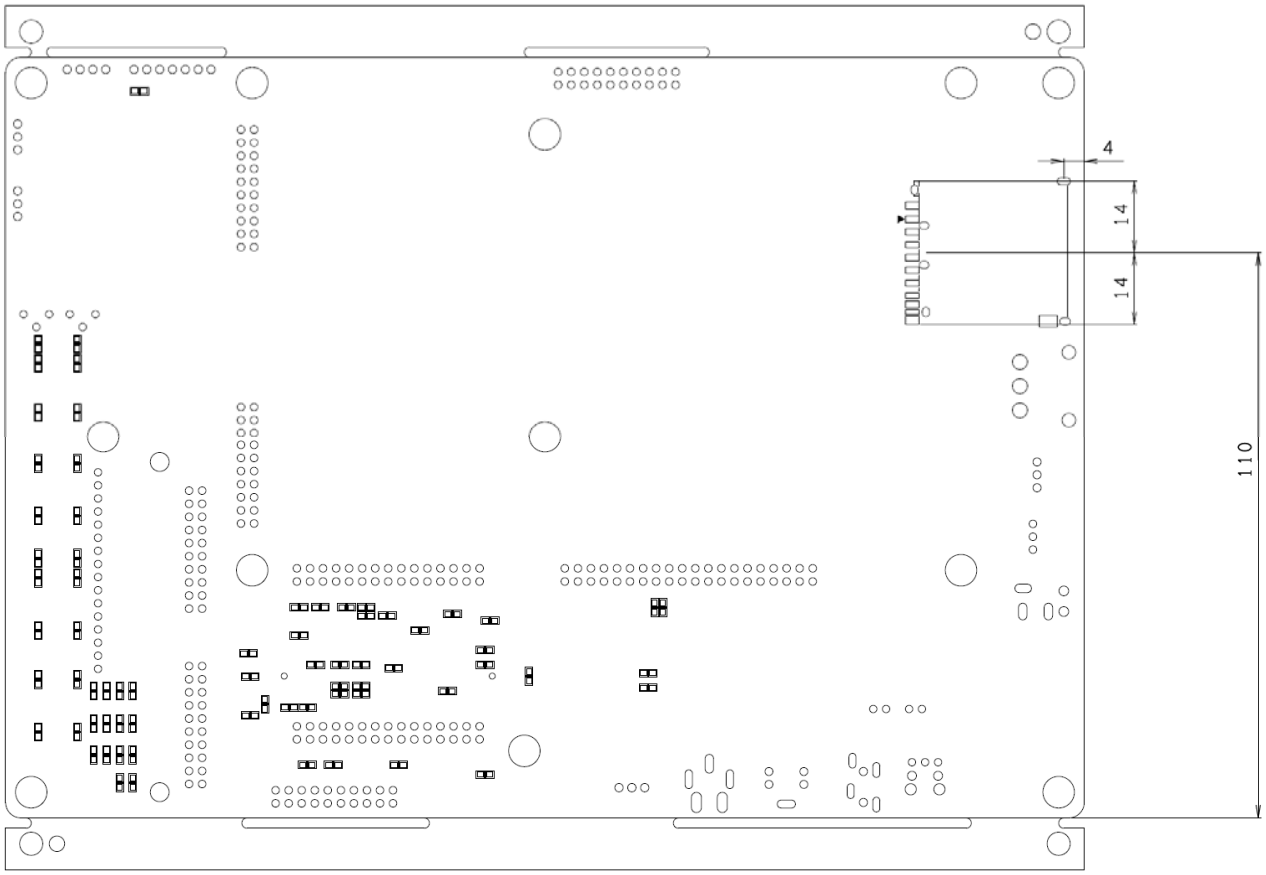
7.3 M3A-HS64G02 Dimensions

Figure 7.3.1 and Figure 7.3.2 show the M3A-HS64G02 dimensions.



Note: All measurements are in millimeters.

Figure 7.3.1 M3A-HS64G02 Dimensions (Top View of the Component Side)



Note: All measurements are in millimeters.

Figure 7.3.2 M3A-HS64G02 Dimensions (Transparent View of the Component Side)

Appendix
Schematics

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SH7264 CPU board M3A-HS64 SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVss)

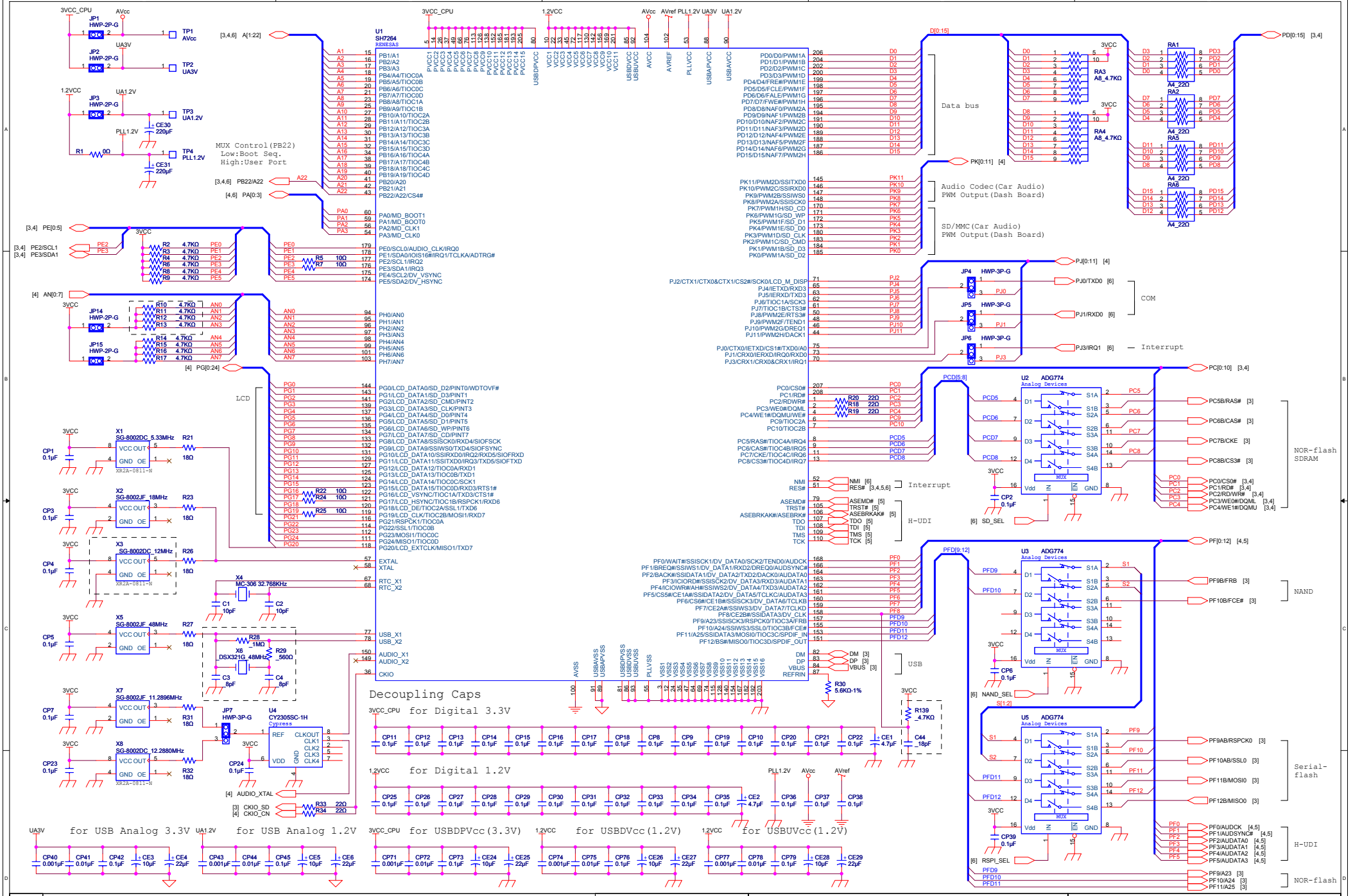
USB Analog GND (USB_AVSS)

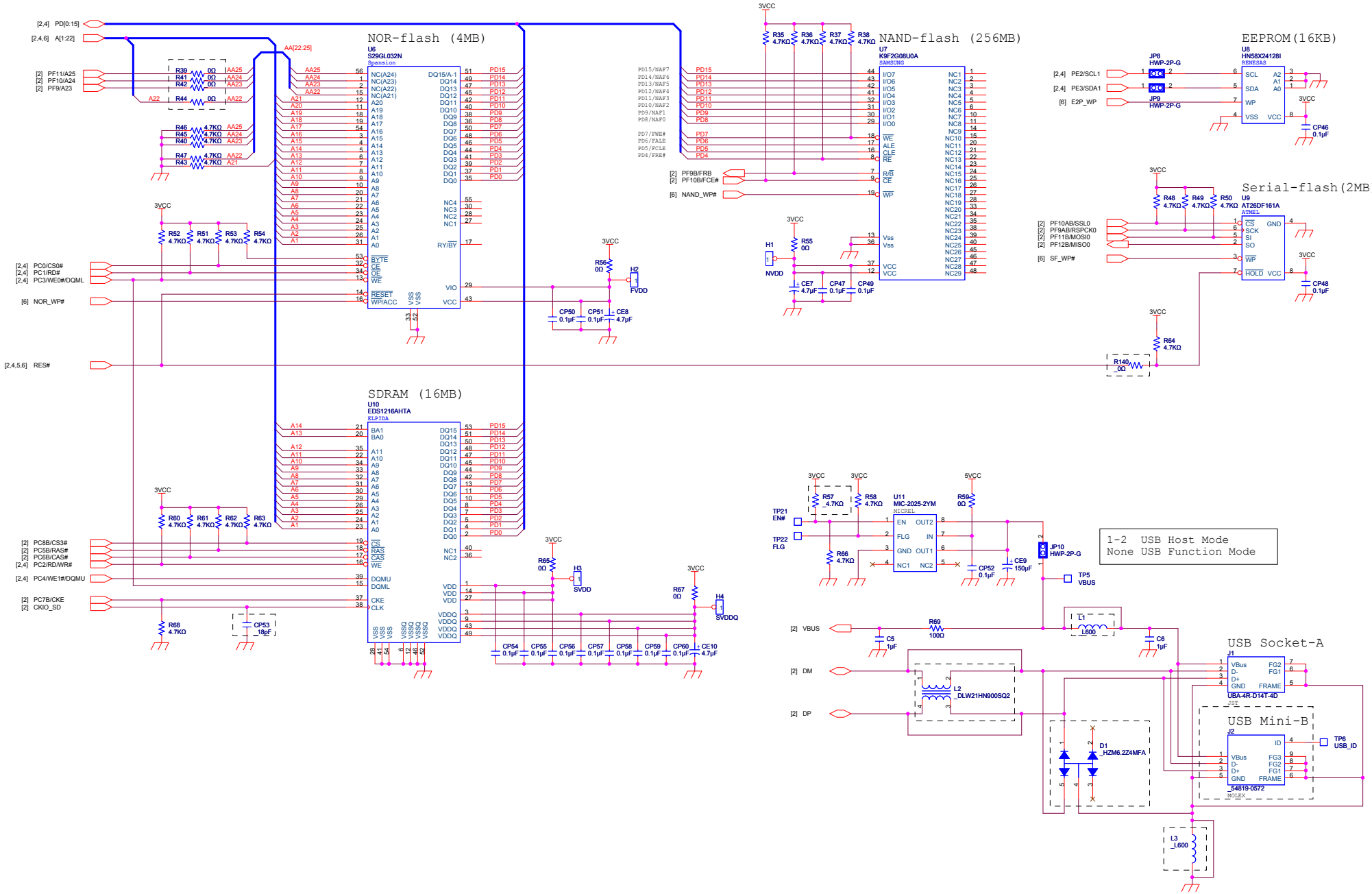
Not mounted

5VCC = Digital 5V
3VCC = Digital 3.3V
3VCC_CPU = 3.3V for CPU
1.2VCC = 1.2V
PLL1.2V = 1.2V for PLL
UA3V = Analog 3.3V for USB
UA1.2V = Analog 1.2V for USB
AVcc = Analog 3.3V
AVref = 3.3V for ADC Voltage Reference

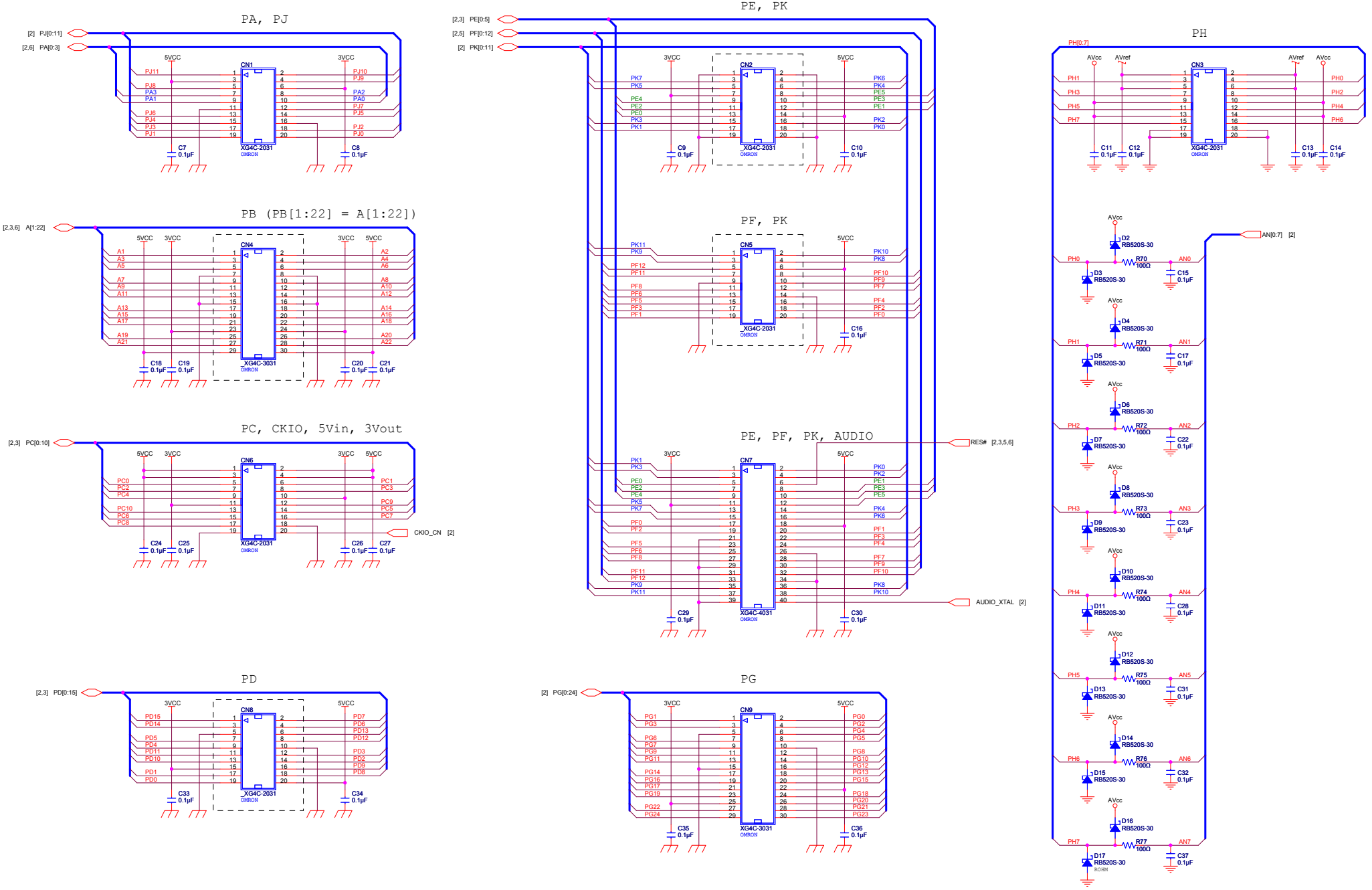
R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64 INDEX (1 / 6)
		SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	
Ver.1.00A		DATE 09-03-02					DK30756-A


U1
SH7264
RENESAS
Data bus
MUX Control(PB22)
Low:Boot Seq.
High:User Port
Audio Codec(Car Audio)
PWM Output(Dash Board)
SD/MMC(Car Audio)
PWM Output(Dash Board)
COM
Interrupt
LCD
H-UDI
USB
NOR-flash
SDRAM
NAND
Serial-
flash
Decoupling Caps
for Digital 3.3V
for Digital 1.2V
for USB Analog 3.3V
for USB Analog 1.2V
for USBDPVcc(3.3V)
for USBDVcc(1.2V)
for USBUVcc(1.2V)
RENESAS SOLUTIONS CORPORATION
M3A-HS64
CPU SH7264, Clock, MUX
(2 / 6)
DK30756-A
CHANGE
Ver.1.00A
SCALE
DATE
09-03-02
DRAWN
CHECKED
DESIGNED
APPROVED

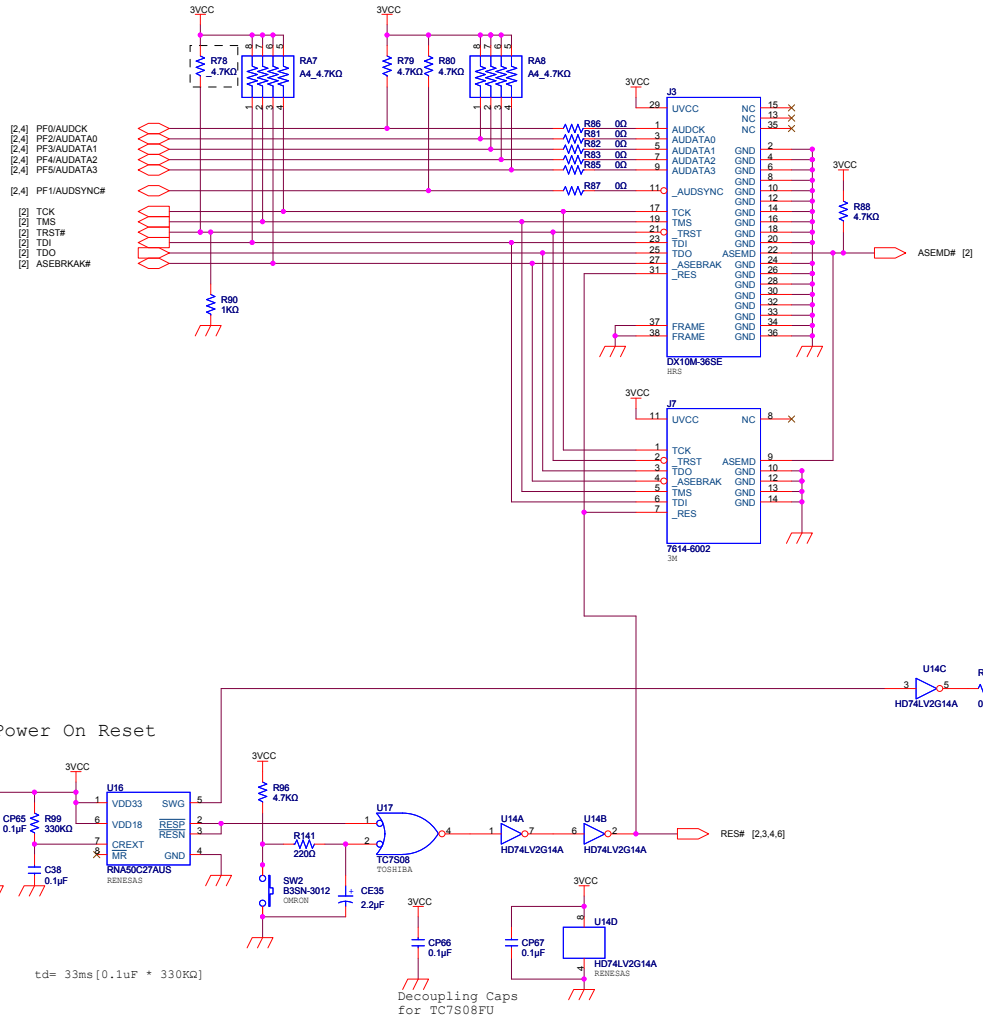


CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64
			DRAWN / CHECKED / DESIGNED / APPROVED		Memory, USB
					(3 / 6)
Ver.1.00A		SCALE			DK30756-A
		DATE	09-03-02		

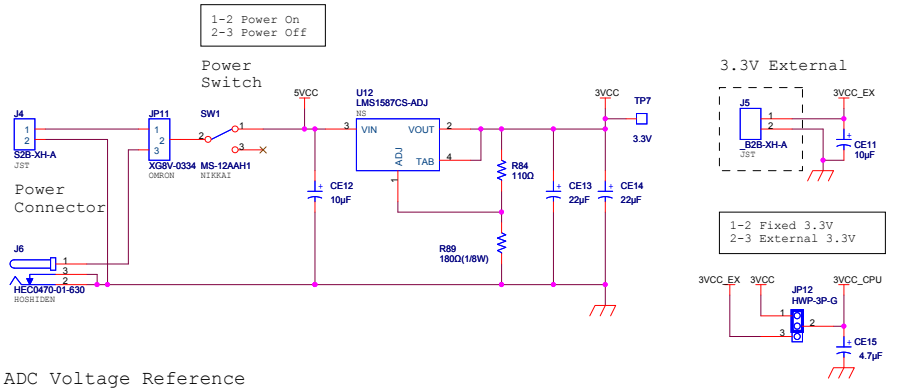


CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64
			DRAWN / CHECKED / DESIGNED / APPROVED		Ext. Connector, AD Protection (4 / 6)
Ver.1.00A		SCALE			DK30756-A
		DATE	09-03-02		

H-UDI Interface

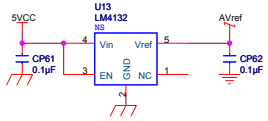


5V To 3.3V Linear Regulator

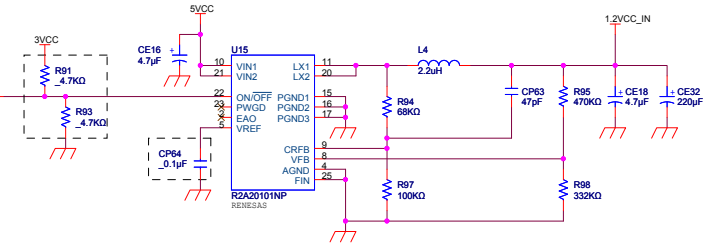


3.3V External

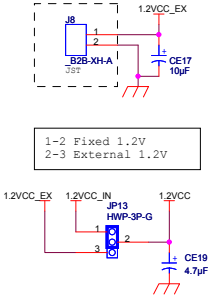
ADC Voltage Reference



5V TO 1.2V STEP DOWN REGULATOR

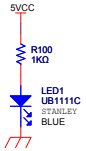


1.2V EXTERNAL

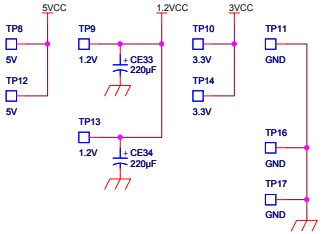


Power On Reset

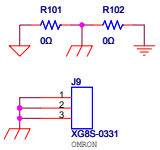
Power LED



POWER TEST PIN

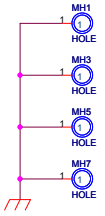


AGND-DGND

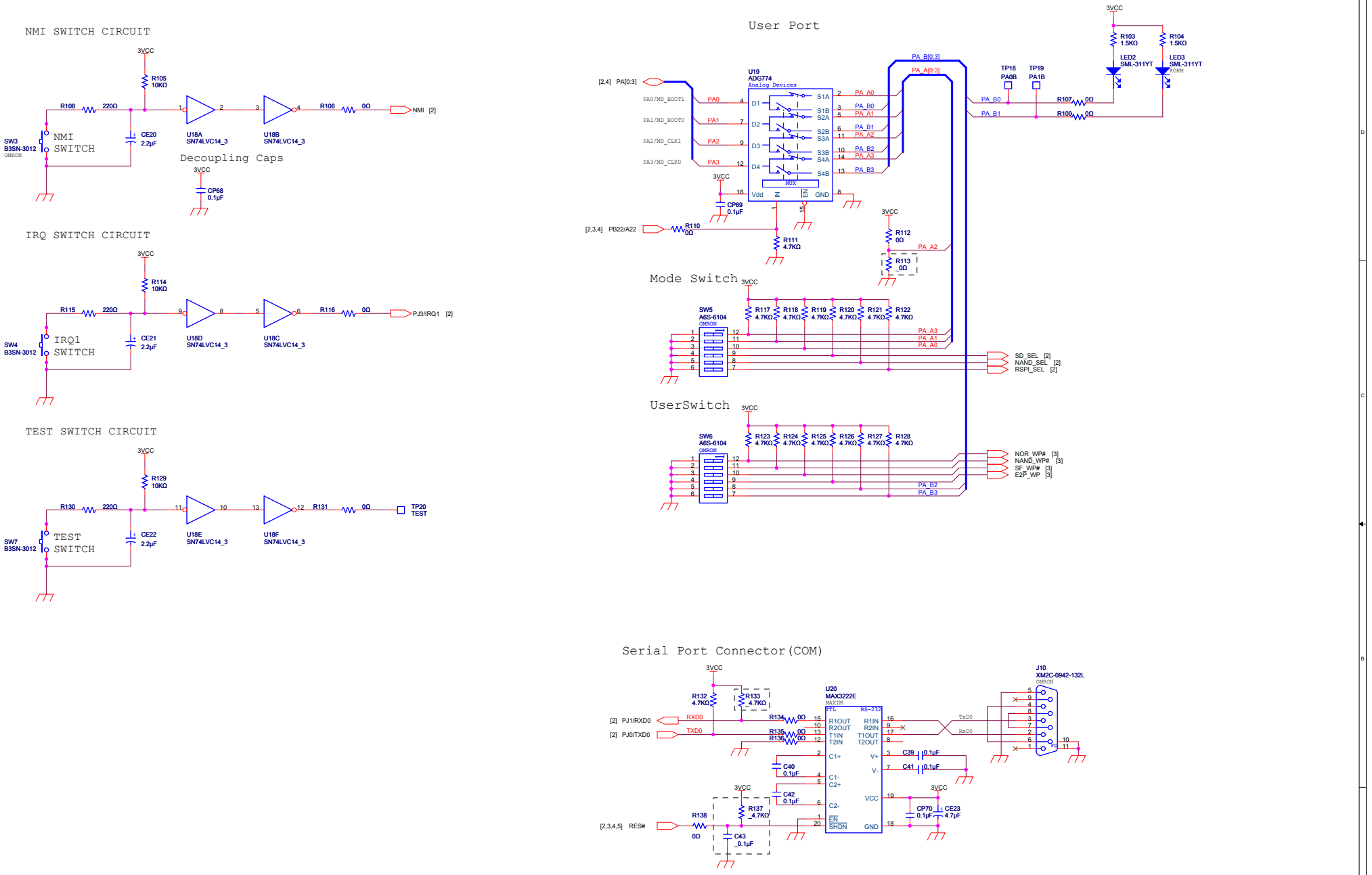


Board fixed hole.

for Corner(M3)



CHANGE		RENESAS SOLUTIONS CORPORATION				M3A-HS64
Ver.1.00A	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	H-UDI,Power, Reset, Hole, TP (5 / 6)
	DATE 09-03-02					DK30756-A



CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64
Ver.1.00A		DRAWN	CHECKED	DESIGNED	APPROVED	Switch, User Port, UART (6 / 6)
	SCALE					
	DATE	09-03-02				DK30756-A

SH7264/62 Optional board M3A-HS64G01 SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVSS)

Analog GND (AGND)

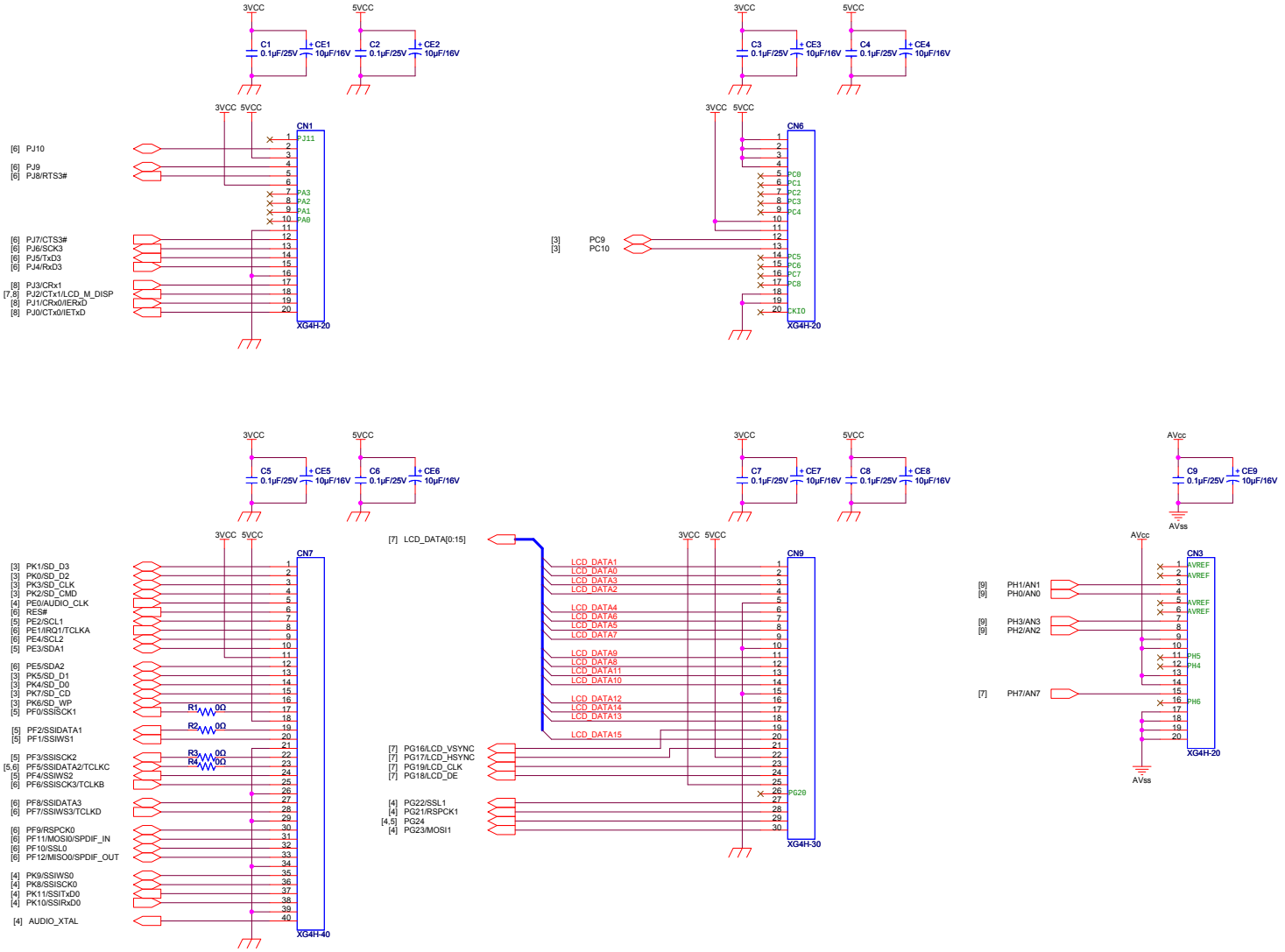
Not mounted

12VCC = Digital 12V Power in
8VCC = Digital 8V for CD
5VCC = Digital 5V
5AVCC = Analog 5V for Audio CODEC
3VCC = Digital 3.3V
3AVCC = Analog 3.3V for Audio DAC
AVcc = Analog 3.3V for Key Input
MCVCC = Digital 3.3V / 5V for SD

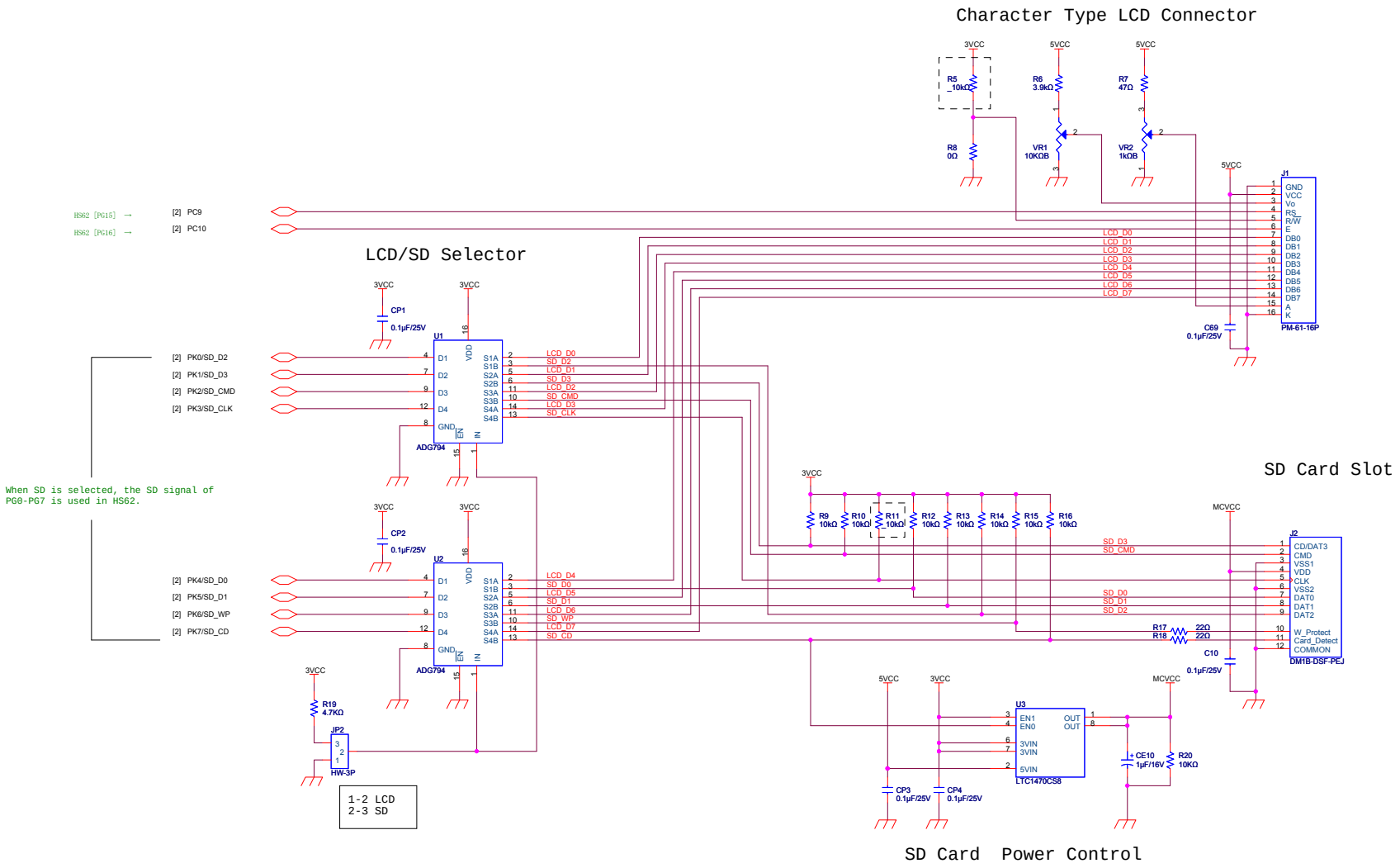
R = Fixed Resistors
C = Ceramic Caps
CP = Decoupling Caps
CE = Electrolytic Caps (Tantal / Electric)

CHANGE							
Ver. 1.00A	SCALE		RENESAS SOLUTIONS CORPORATION				M3A-HS64G01
	DATE	09-03-02	DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 10)
							DK30759

M3A-HS64/HS62 CPU Board Stack Connector

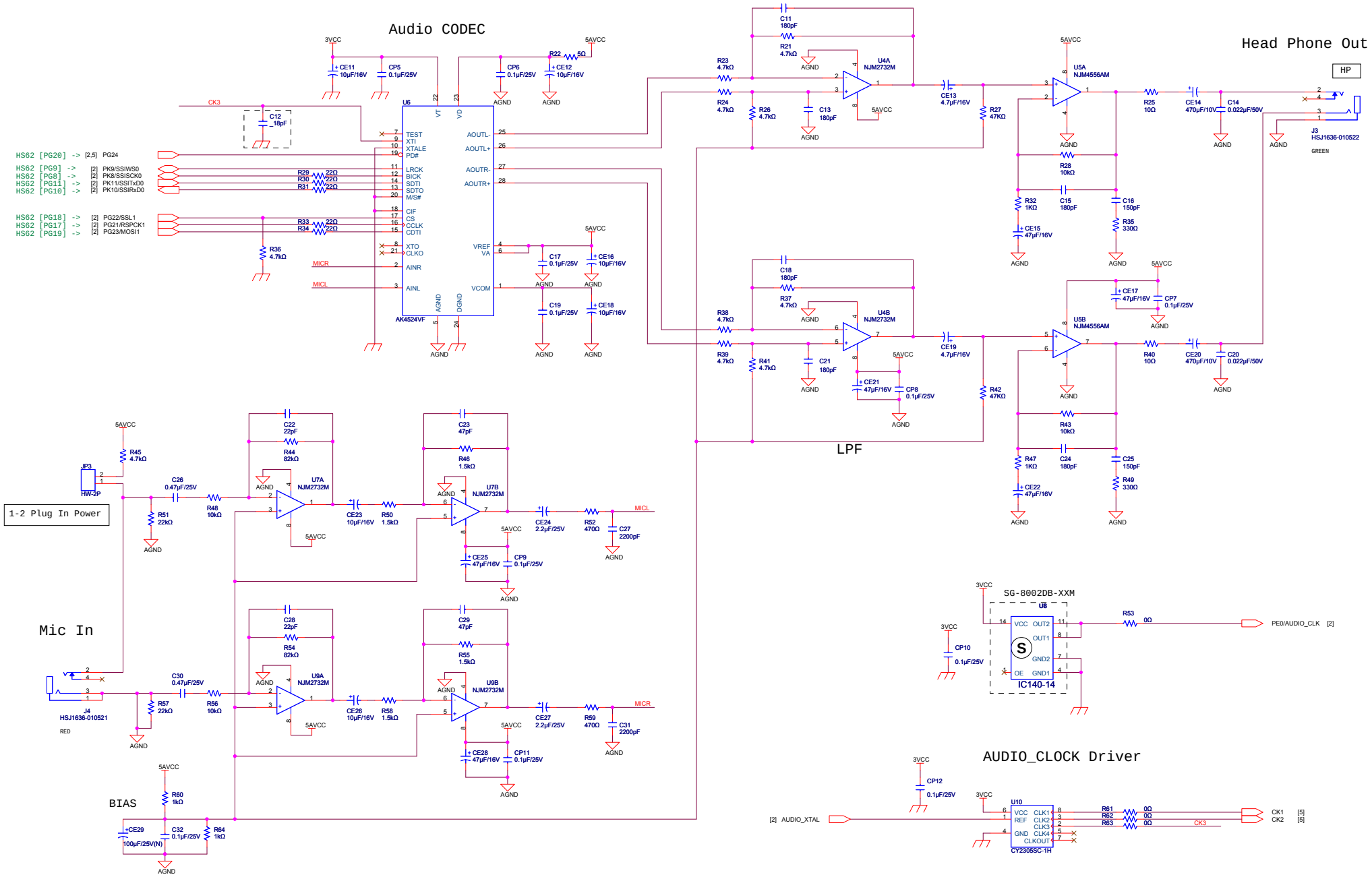


CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64G01
			DRAWN	CHECKED	DESIGNED	APPROVED	CPU Board Stack Connector (2 / 10)
Ver. 1.00A		SCALE					DK30759
		DATE	09-03-02				



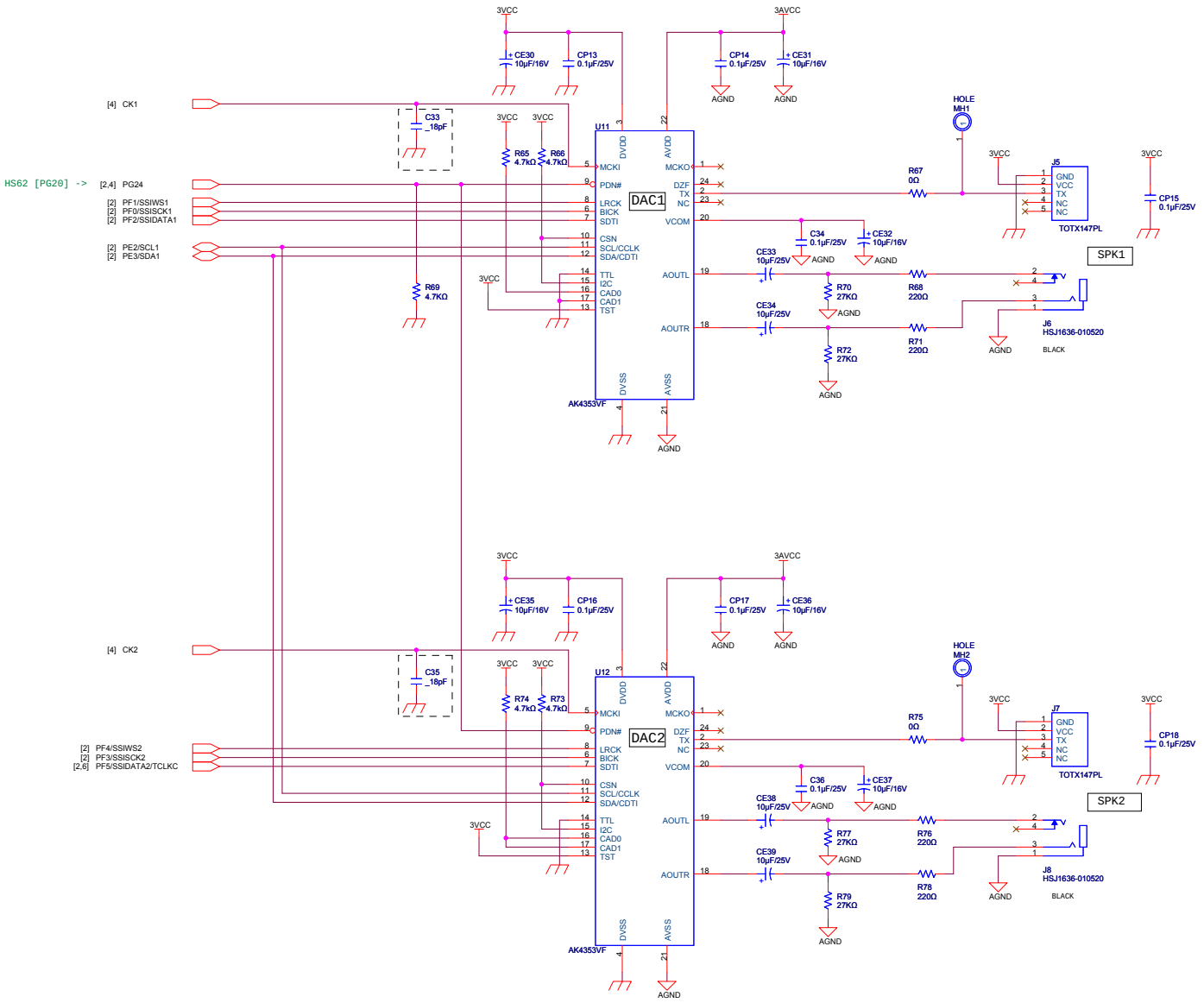
CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Character LCD/SD Card Slot (3 / 10)
Ver. 1.00A		SCALE			DK30759
		DATE	09-03-02		

Audio Interface



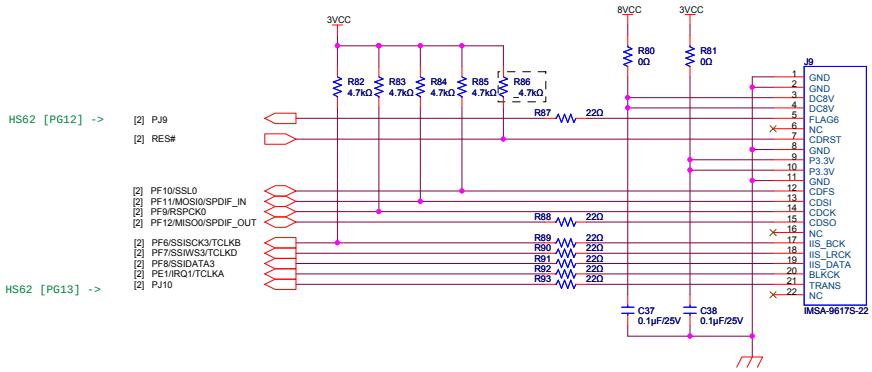
CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Audio CODEC (4 / 10)
Ver. 1.00A		SCALE			DK30759
		DATE	09-03-02		

Audio DAC

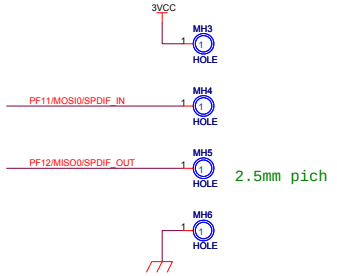


CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64G01
			DRAWN	CHECKED	DESIGNED	APPROVED	Audio D/A Converter (5 / 10)
Ver. 1.00A		SCALE					DK30759
		DATE	09-03-02				

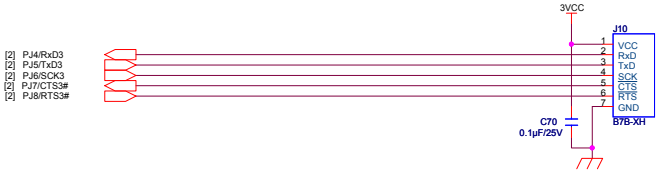
CD deck Interface



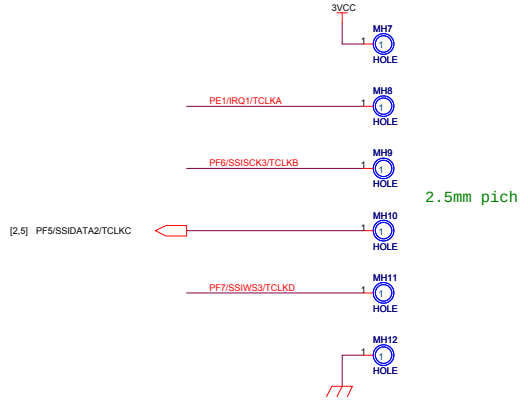
RSPDIF Through Hole.



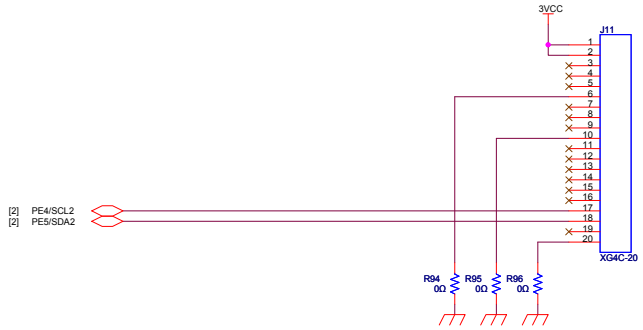
UART Interface



Rotary Encoder Through Hole.

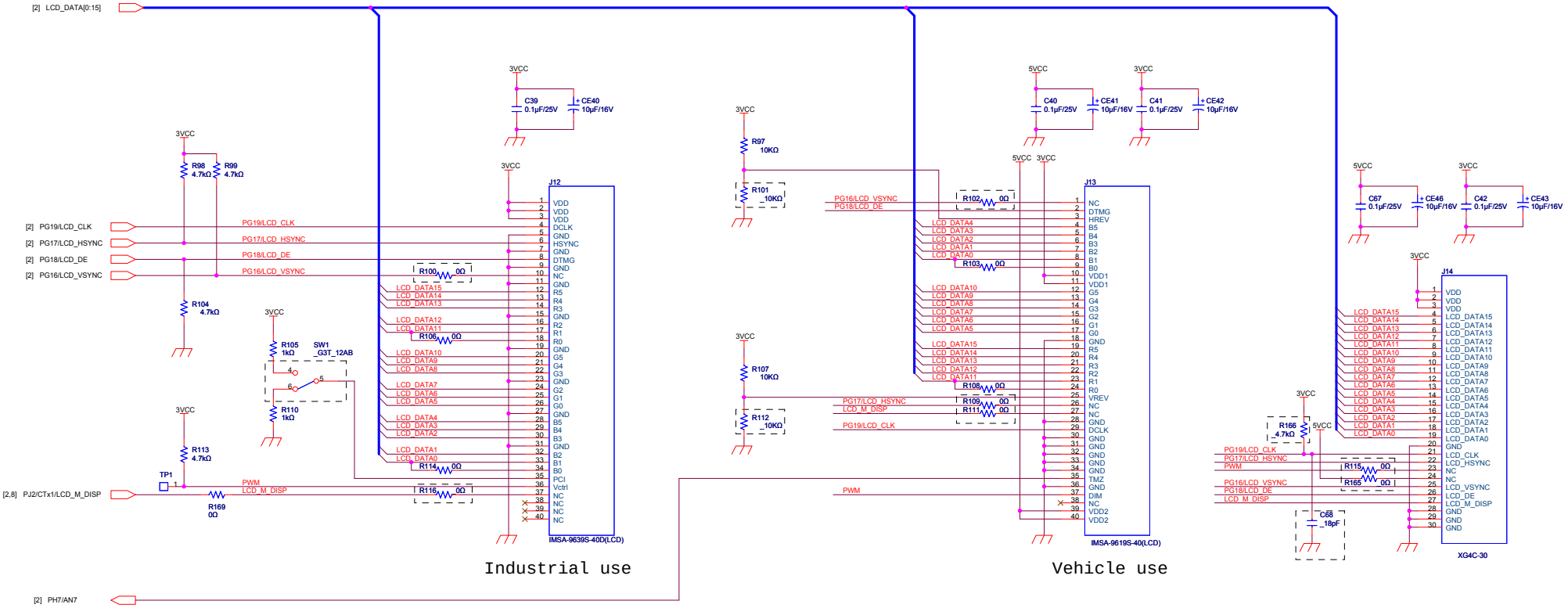


IIC Interface

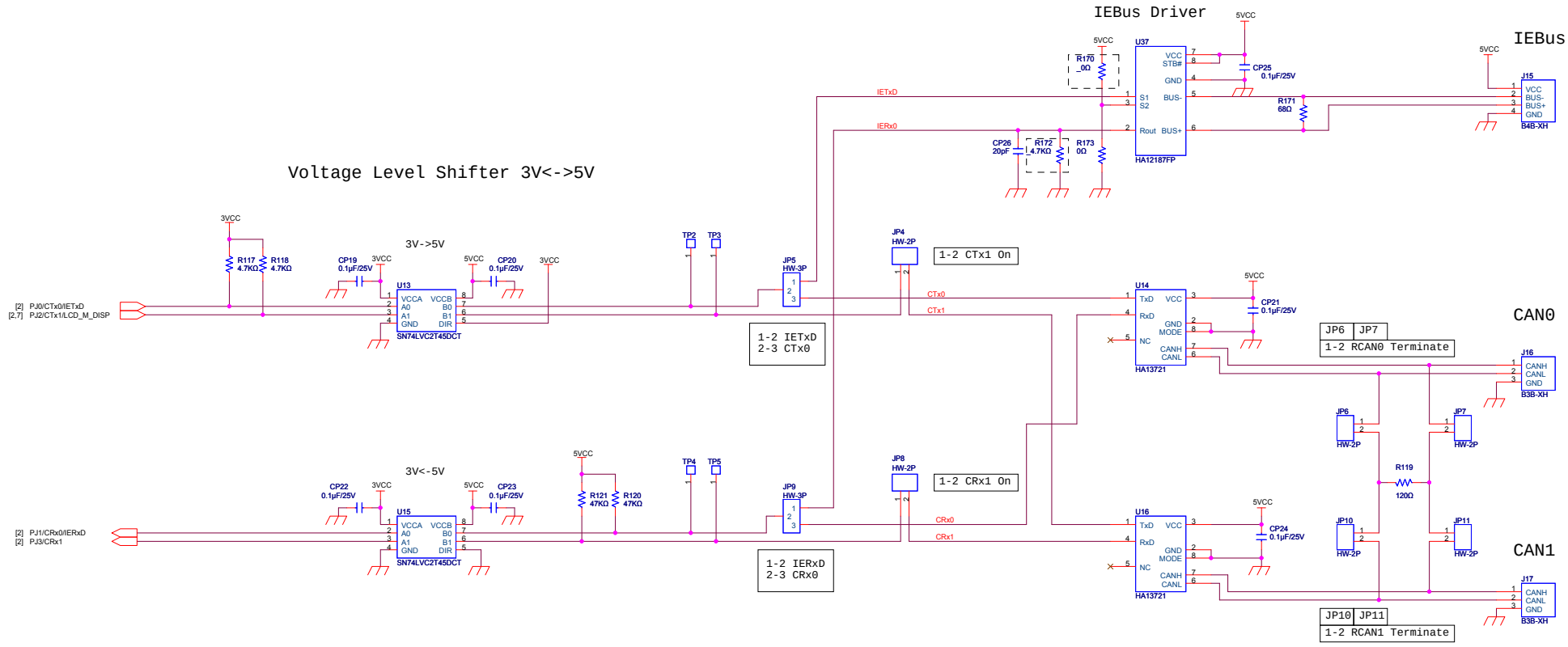


CHANGE						
Ver. 1.00A		SCALE		RENESAS SOLUTIONS CORPORATION		M3A-HS64G01
		DATE	09-03-02	DRAWN / CHECKED / DESIGNED / APPROVED		CD/UART/IIC/RSPDIF/Rotary Enc. (6 / 10)
						DK30759

TFT LCD Module Interface

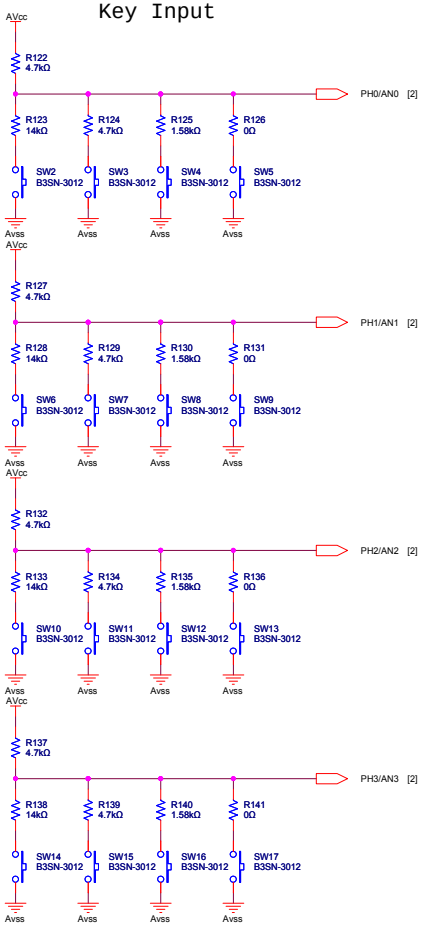


CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		LCD Module Connector
Ver. 1.00A		SCALE			(7 / 10)
		DATE 09-03-02			DK30759

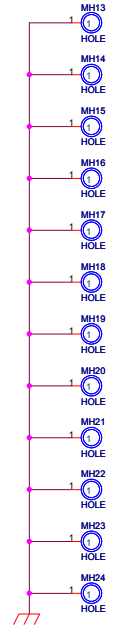


CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64G01
			DRAWN	CHECKED	DESIGNED	APPROVED	CAN/IEBus (8 / 10)
	Ver. 1.00A	SCALE					DK30759
		DATE	09-03-02				

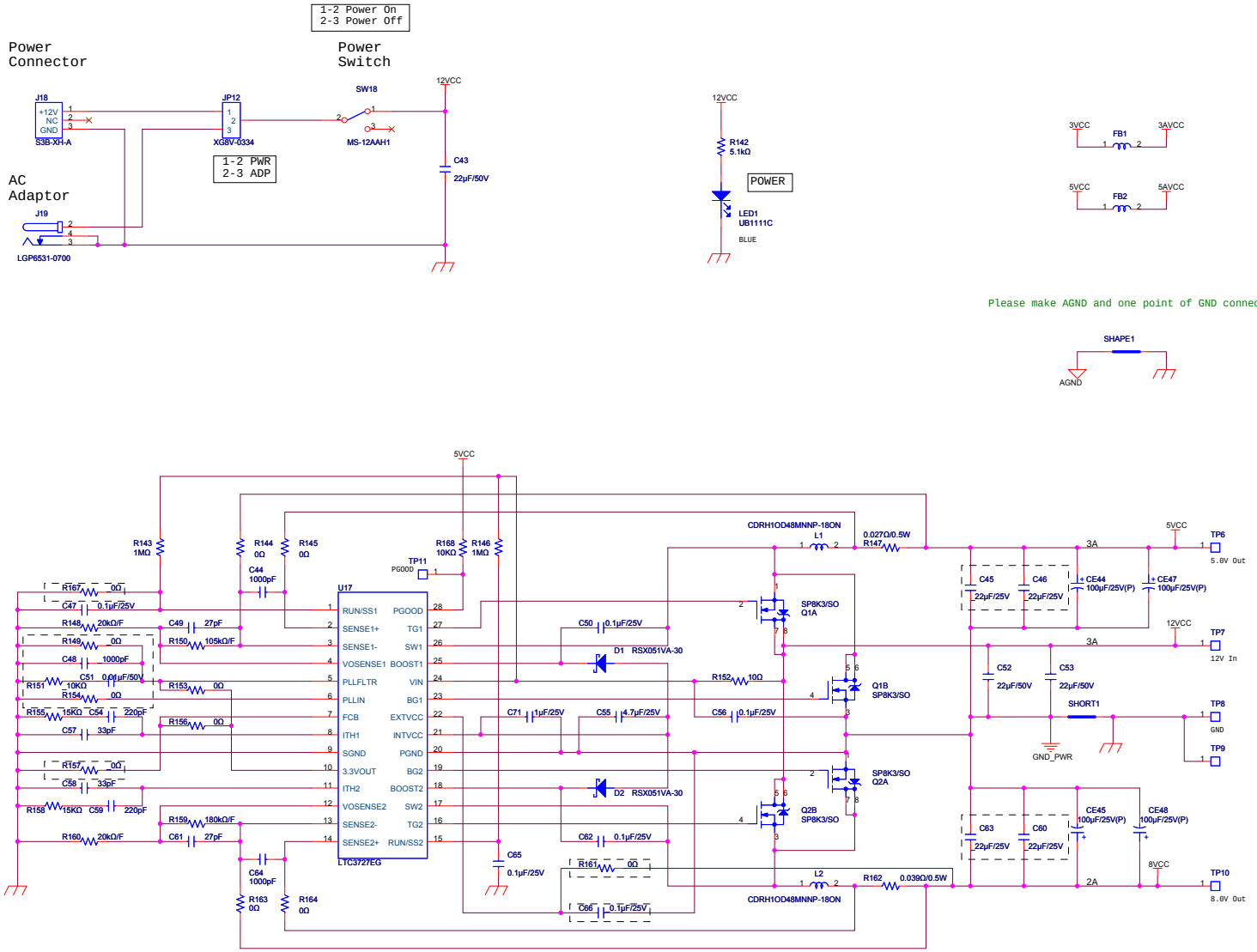
Key Input



Board fixed hole.



CHANGE						
Ver. 1.00A					RENESAS SOLUTIONS CORPORATION	M3A-HS64G01
	SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	Key Input (9 / 10)
	DATE	09-03-02					DK30759



CHANGE	Ver. 1.00A	SCALE		RENESAS SOLUTIONS CORPORATION	M3A-HS64G01
		DATE	09-03-02	DRAWN / CHECKED / DESIGNED / APPROVED	Power Generate (10 / 10)
					DK30759

SH7264 Optional board M3A-HS64G02 SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVSS)

Analog GND (AGND1,AGND2)

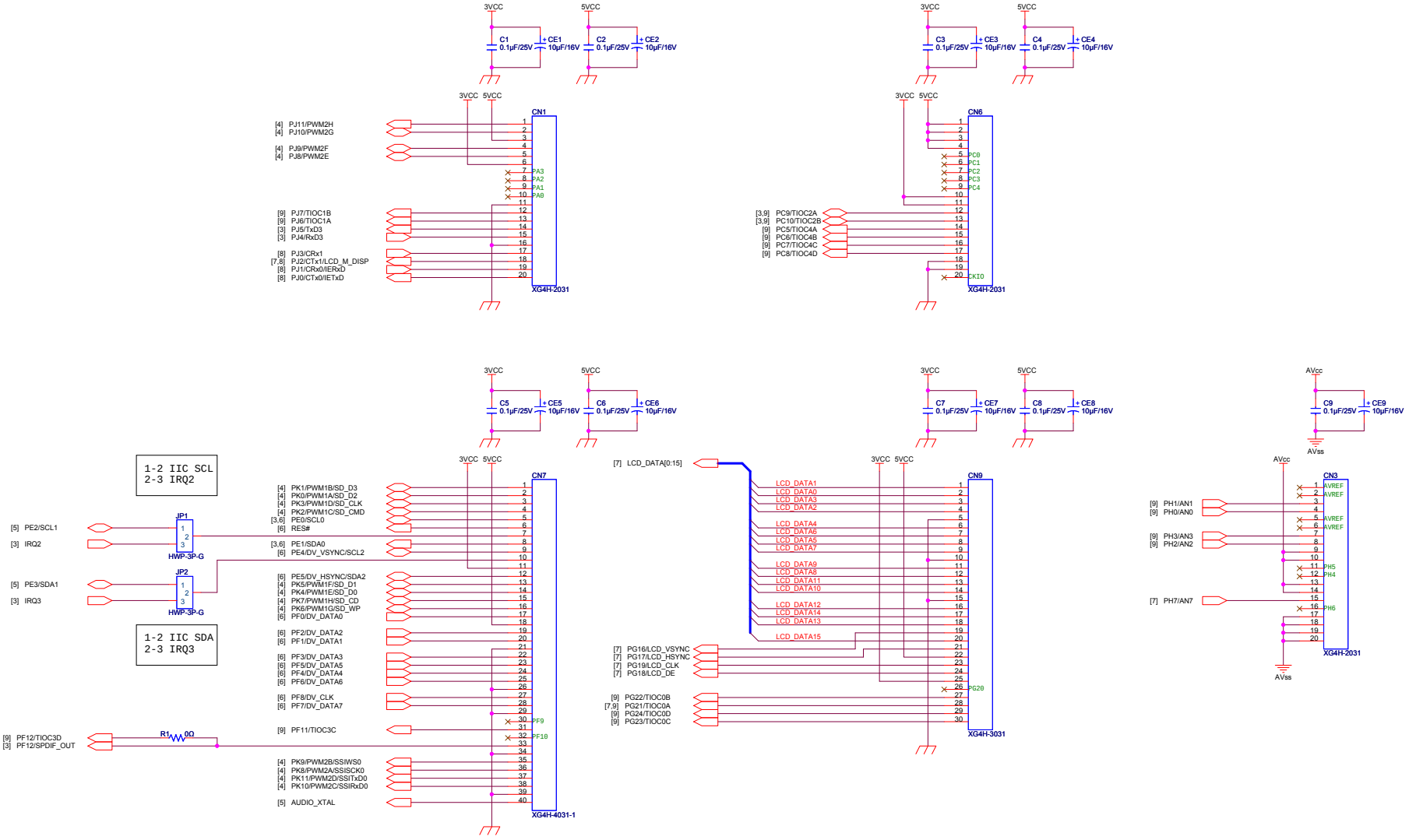
Not mounted

12VCC = Digital 12V Power in
8VCC = Digital 8V for CD
5VCC = Digital 5V
3VCC = Digital 3.3V
3AVCC1 = Analog 3.3V for Audio DAC
3AVCC2 = Analog 3.3V for Video Decoder
AVcc = Analog 3.3V for Key Input
MCVCC = Digital 3.3V / 5V for SD

R = Fixed Resistors
C = Ceramic Caps
CP = Decoupling Caps
CE = Electrolytic Caps (Tantal / Electric)

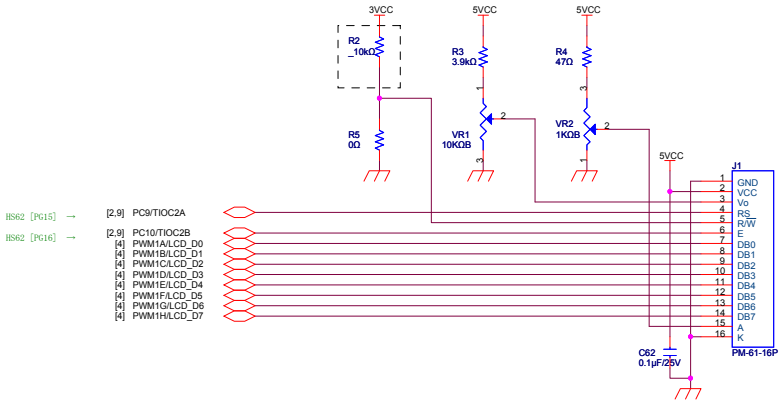
CHANGE						
Ver. 1.00A	SCALE		RENESAS SOLUTIONS CORPORATION			M3A-HS64G02
	DATE	09-03-02	DRAWN	CHECKED	DESIGNED	APPROVED
						INDEX (1 / 10)
						DK30762

SH7264 Extension Connector



CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	CPU Board Stack Connector (2 / 10)
	Ver. 1.00A	SCALE					DK30762
		DATE	09-03-02				

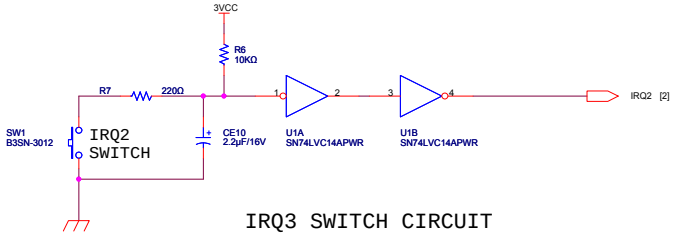
Character Type LCD Connector



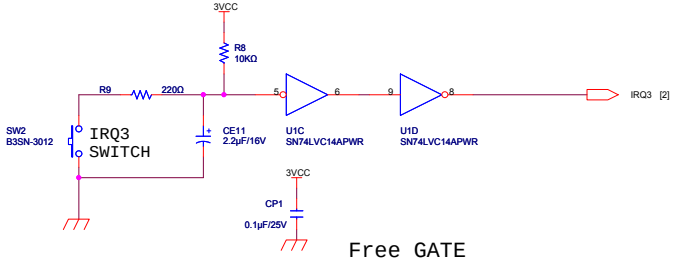
RSPDIF Through Hole.

UART Interface

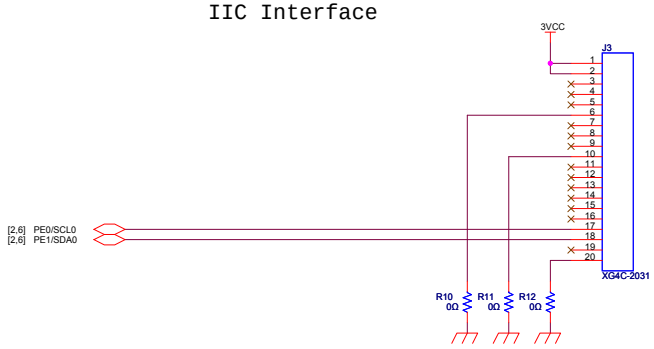
IRQ2 SWITCH CIRCUIT



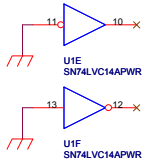
IRQ3 SWITCH CIRCUIT



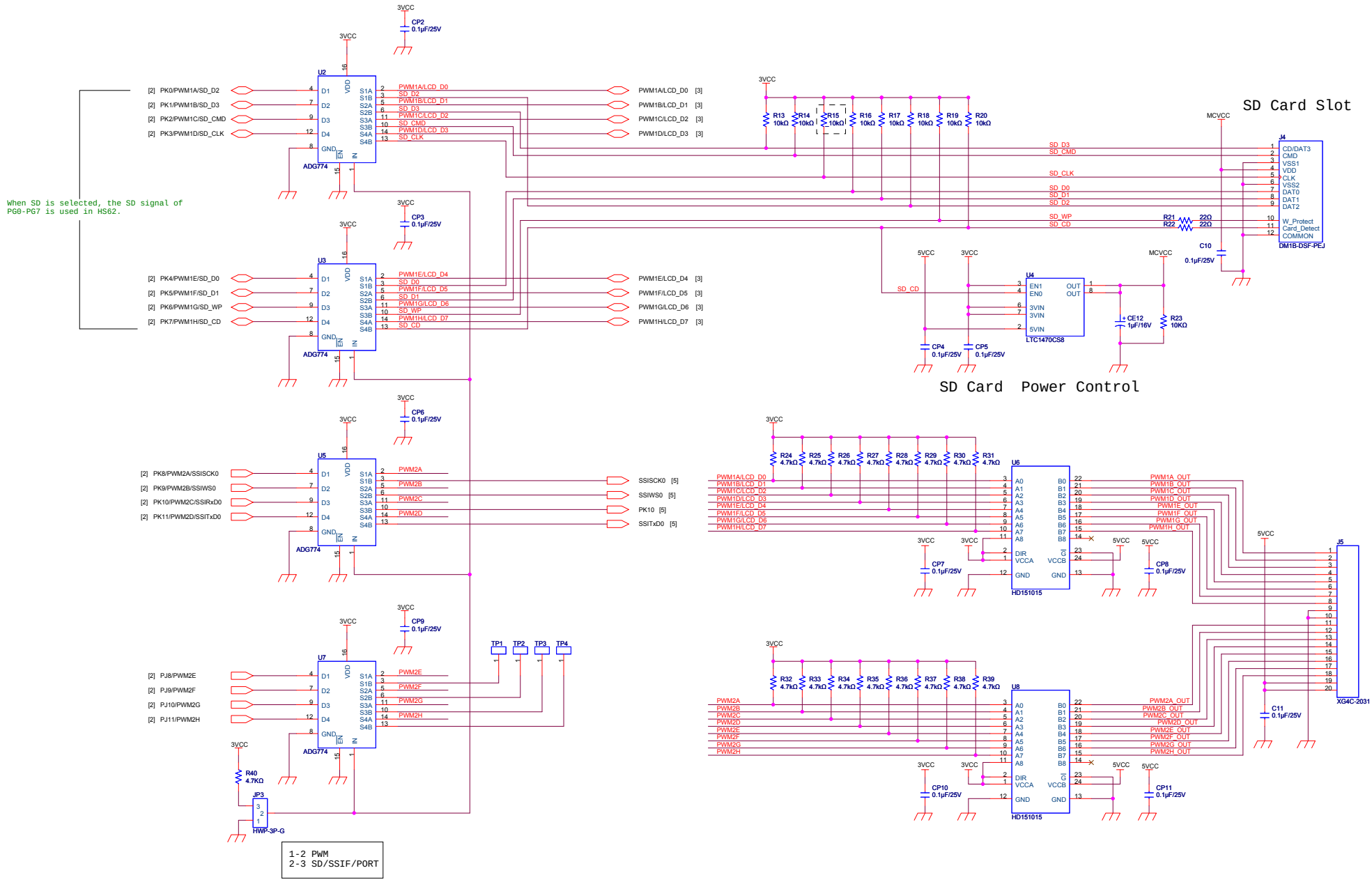
IIC Interface



Free GATE

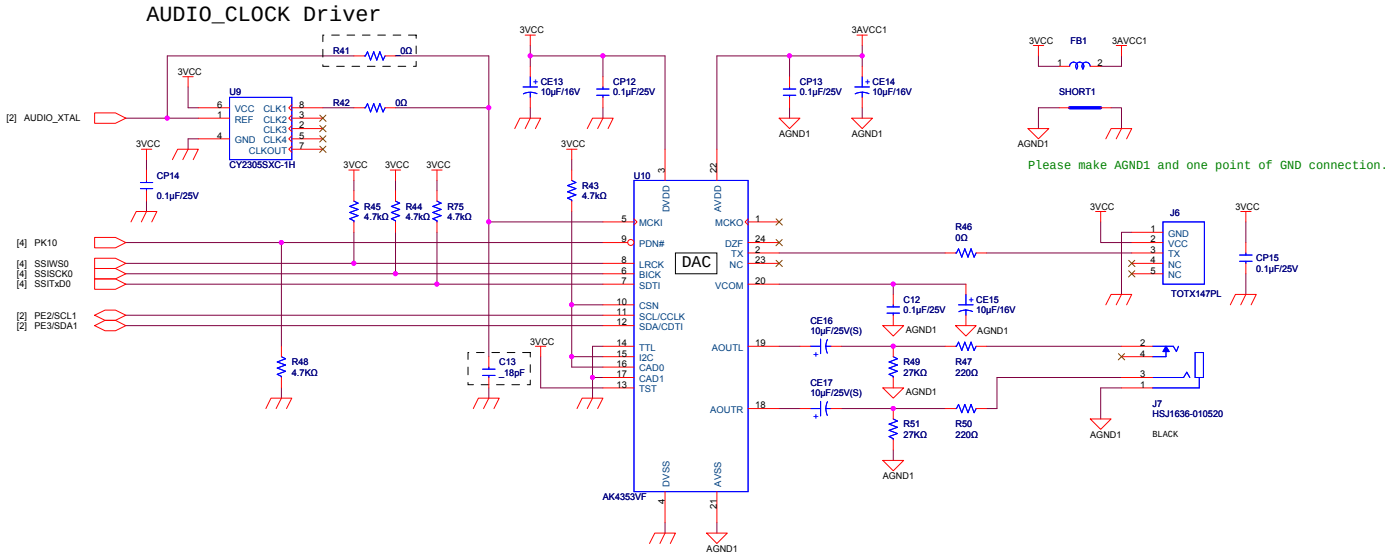


CHANGE				RENESAS SOLUTIONS CORPORATION				M3A-HS64G02
				DRAWN	CHECKED	DESIGNED	APPROVED	Character LCD/UART/IIC/IRQ (3 / 10)
Ver. 1.00A		SCALE						DK30762
		DATE	09-03-02					

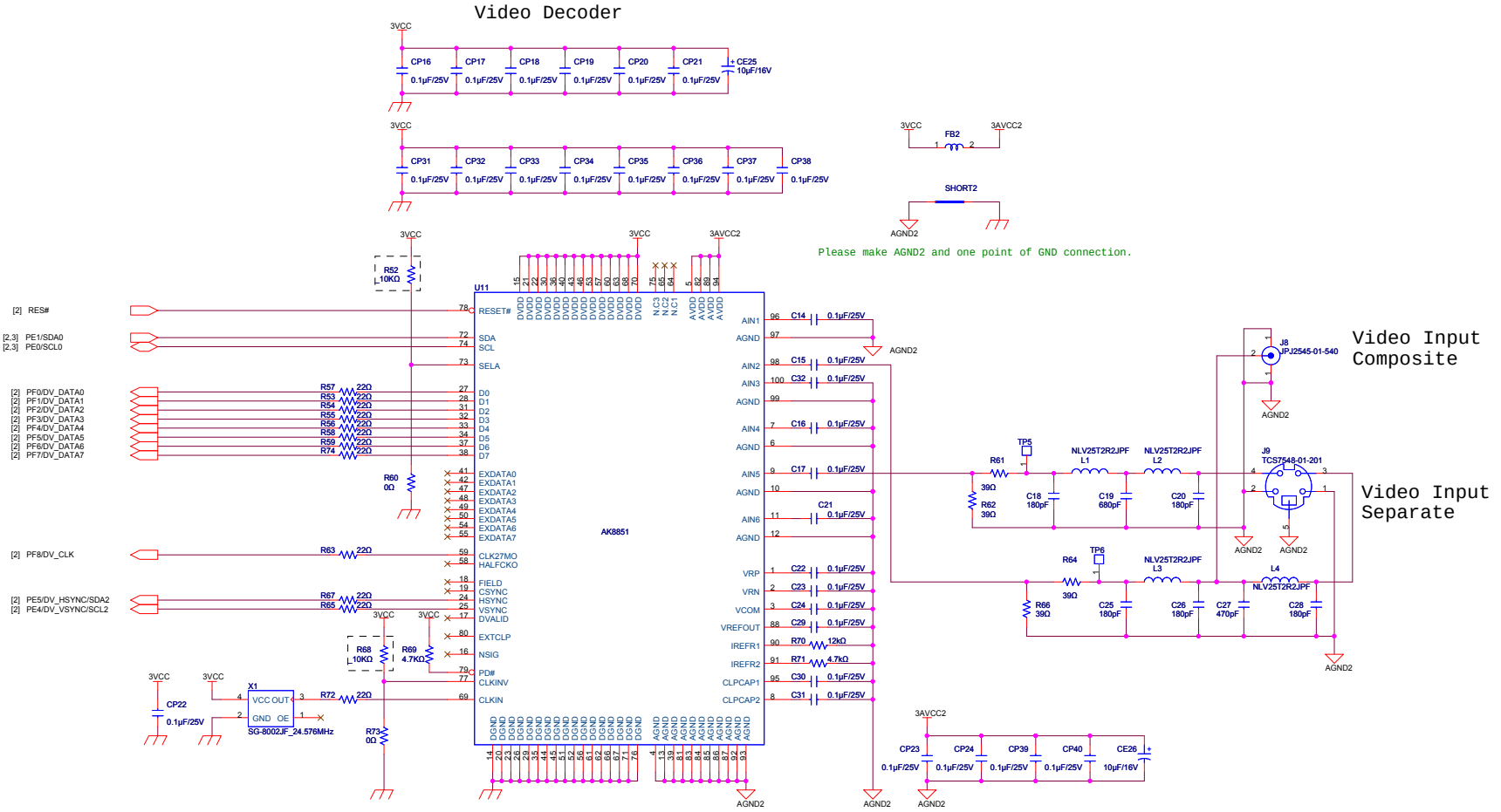


CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	SD Card Slot/PWM (4 / 10)
Ver. 1.00A		SCALE					DK30762
		DATE	09-03-02				

Audio Interface

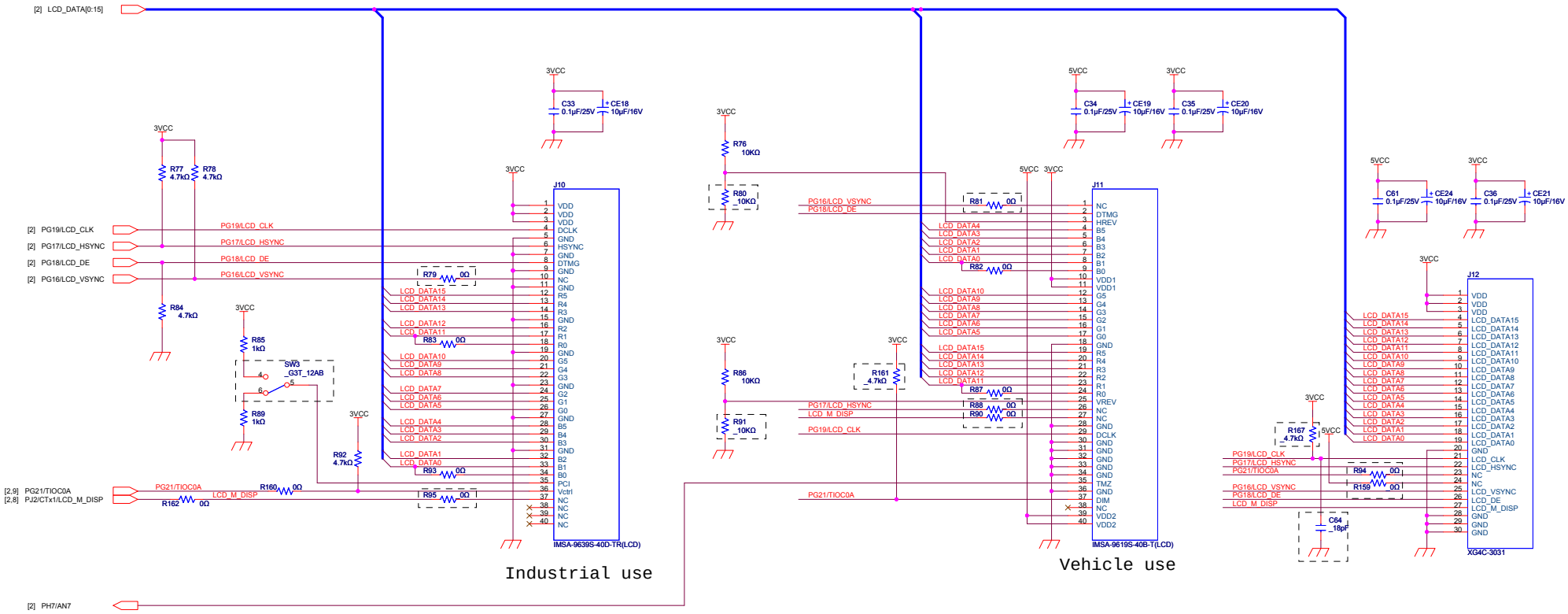


CHANGE		SCALE		RENESAS SOLUTIONS CORPORATION				M3A-HS64G02	
				DRAWN	CHECKED	DESIGNED	APPROVED	Audio D/A Converter	(5 / 10)
	Ver. 1.00A	DATE	09-03-02					DK30762	

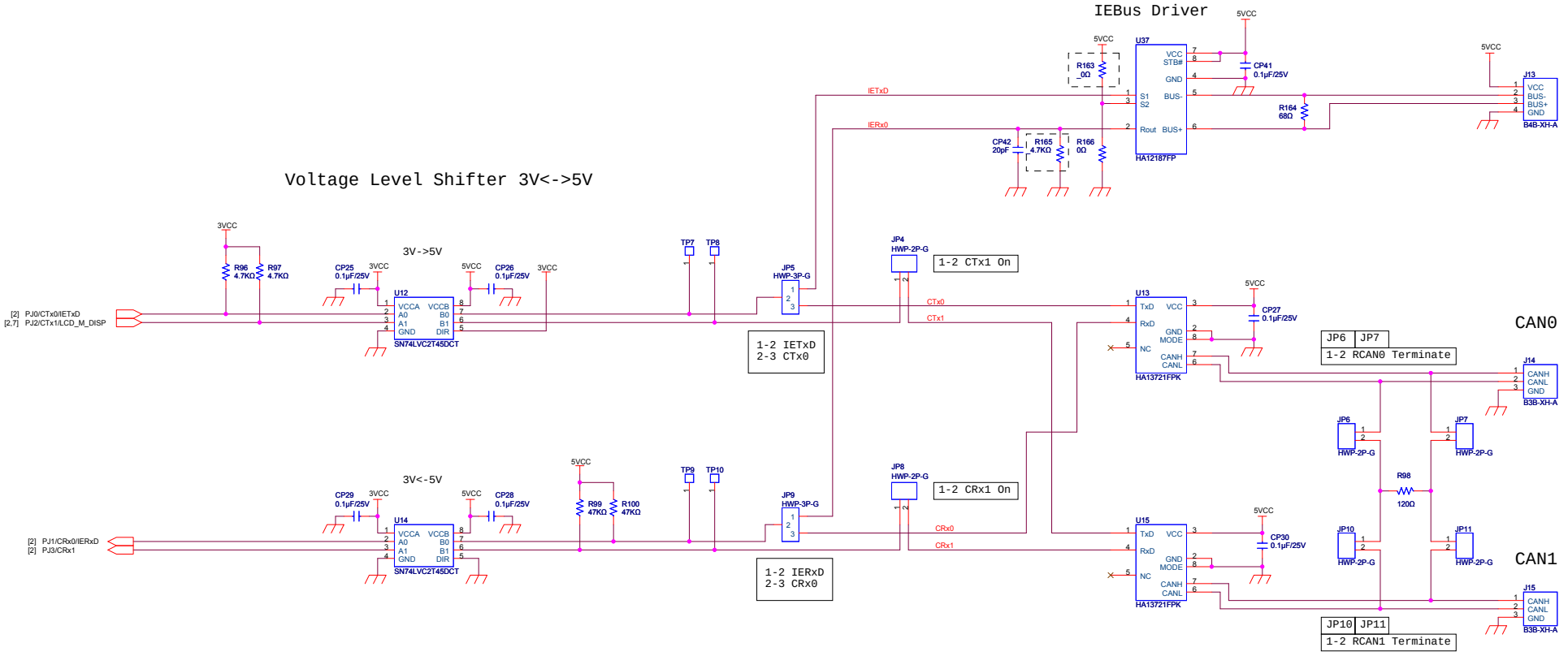


CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64G02
			DRAWN	CHECKED / DESIGNED / APPROVED	Video Decoder (6 / 10)
Ver. 1.00A		SCALE			DK30762
		DATE	09-03-02		

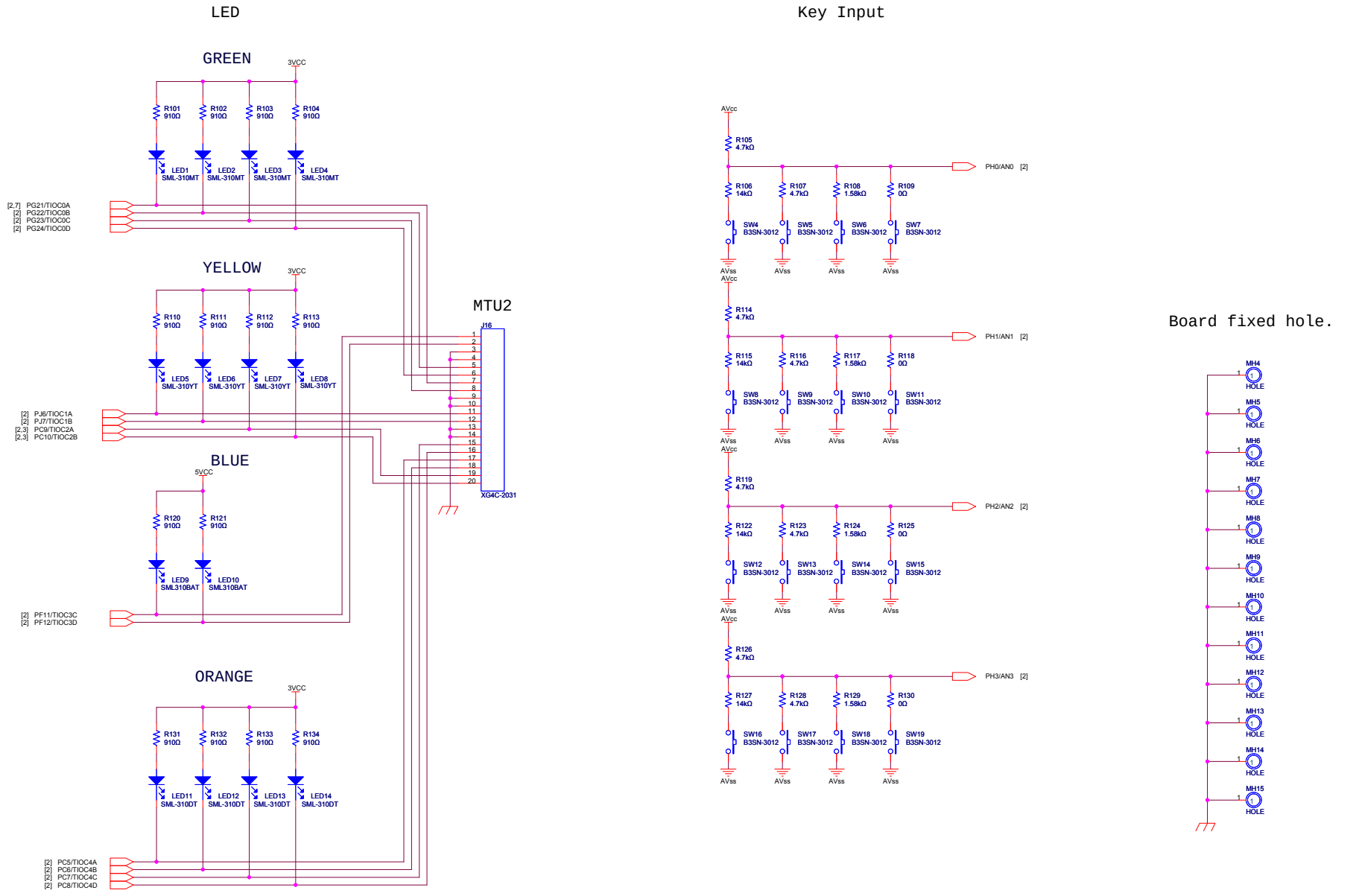
TFT LCD Module Interface



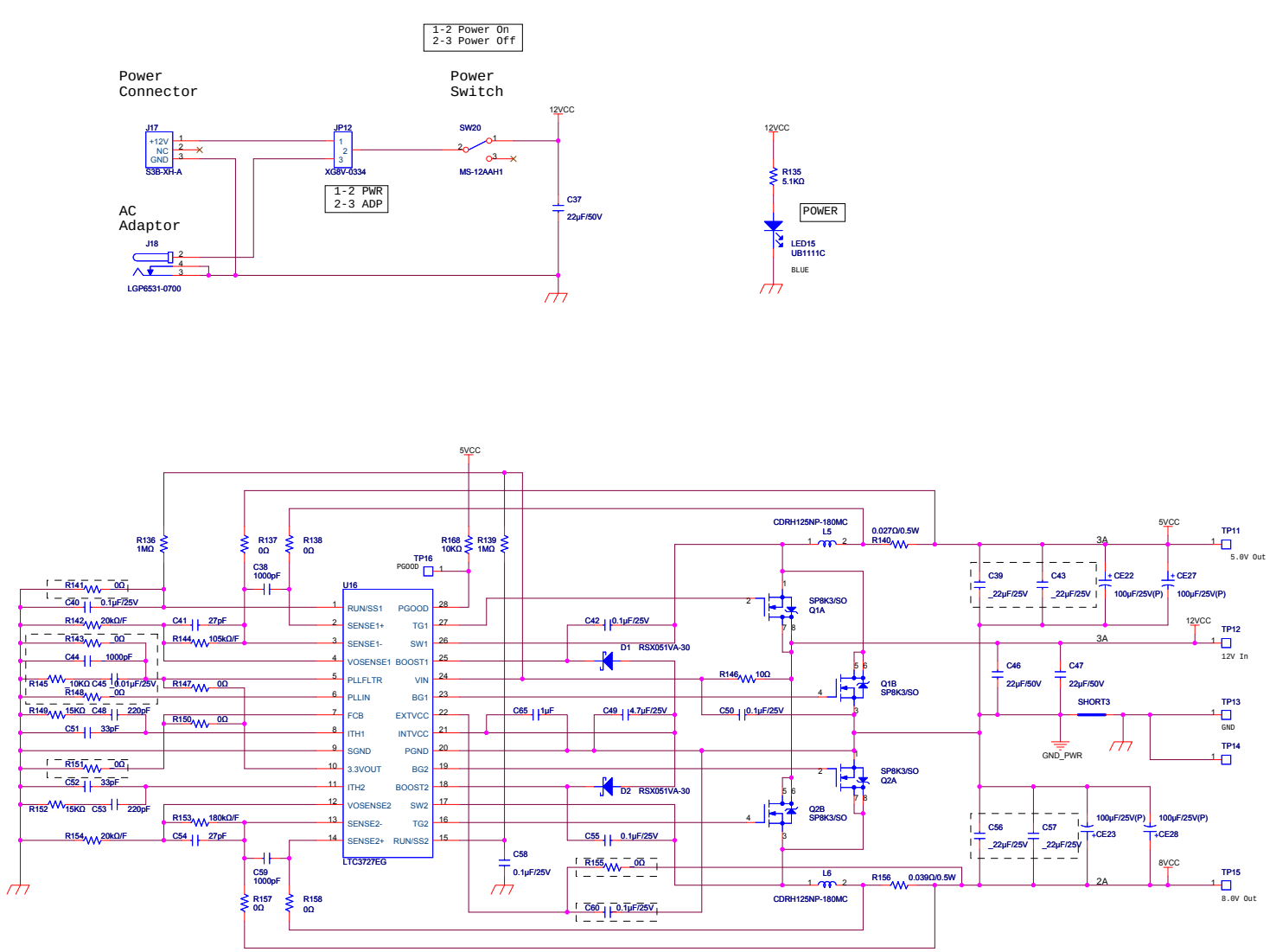
CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	LCD Module Connector
							(7 / 10)
Ver. 1.00A		SCALE					DK30762
		DATE	09-03-02				



CHANGE		SCALE		RENESAS SOLUTIONS CORPORATION				M3A-HS64G02	
	Ver. 1.00A	DATE	09-03-02	DRAWN	CHECKED	DESIGNED	APPROVED	CAN/IEBus	(8 / 10)
								DK30762	



CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS64G02
Ver. 1.00A	SCALE		DRAWN / CHECKED / DESIGNED / APPROVED		LED/Key Input (9 / 10)
	DATE	09-03-02			DK30762



CHANGE		SCALE		RENESAS SOLUTIONS CORPORATION				M3A-HS64G02	
	Ver. 1.00A	DATE	09-03-02	DRAWN	CHECKED	DESIGNED	APPROVED	Power Generate	(10 / 10)
								DK30762	

Revision History	M3A-HS64 User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Apr 30, 2009	-	First edition issued

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SH7264 CPU board
User's Manual
M3A-HS64

Publication Date Apr 30, 2009 Rev. 1.00

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Renesas Solutions Corp.

SH7264 CPU Board
M3A-HS64
User's Manual

Renesas Electronics Corporation
1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan

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