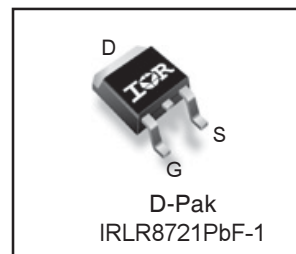
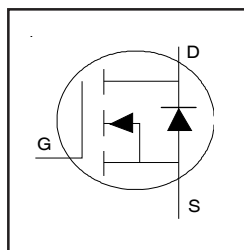


HEXFET® Power MOSFET

V_{DS}	30	V
$R_{DS(on) max}$ (@ $V_{GS} = 10V$)	8.4	mΩ
Q_g (typical)	8.5	nC
I_D (@ $T_C = 25^\circ C$)	65 ④	A



Features

Industry-standard pinout D-Pak
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Industrial qualification



Benefits

Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base Part Number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRLR8721PbF-1	D-Pak	Tape and Reel	2000	IRLR8721TRPbF-1

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	65④	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	46④	
I_{DM}	Pulsed Drain Current ①	260	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	65	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	33	
	Linear Derating Factor	0.43	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)⑤	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes ① through ⑤ are on page 12

Static @ T_J = 25°C (unless otherwise specified)

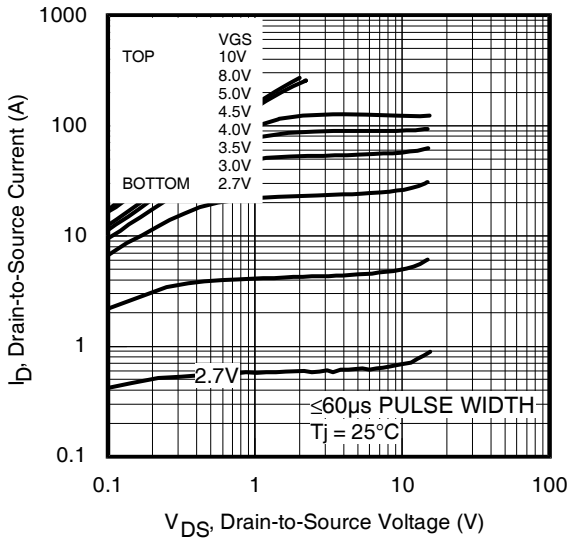
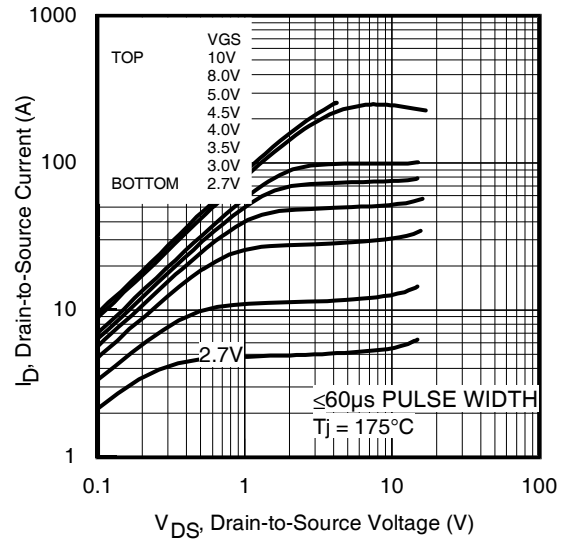
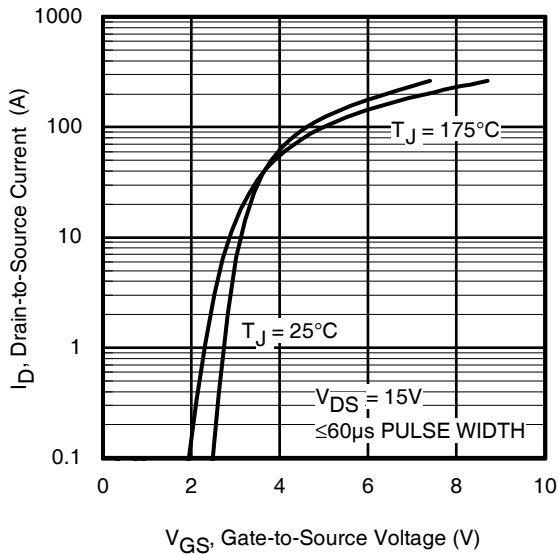
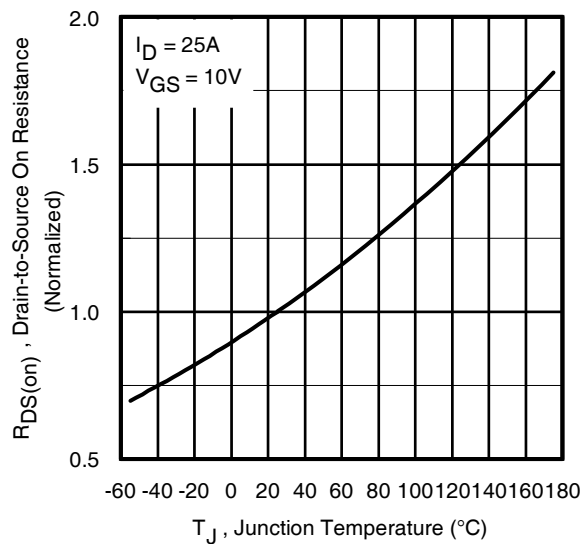
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	6.3	8.4	mΩ	V _{GS} = 10V, I _D = 25A ④
		—	10.1	11.8		V _{GS} = 4.5V, I _D = 20A ④
V _{GS(th)}	Gate Threshold Voltage	1.35	1.9	2.35	V	V _{DS} = V _{GS} , I _D = 25μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-6.8	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	46	—	—	S	V _{DS} = 15V, I _D = 20A
Q _g	Total Gate Charge	—	8.5	13	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 20A See Fig. 16
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	1.9	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	1.2	—		
Q _{gd}	Gate-to-Drain Charge	—	3.4	—		
Q _{godr}	Gate Charge Overdrive	—	2.0	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	4.6	—		
Q _{oss}	Output Charge	—	7.9	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	2.3	3.8	Ω	
t _{d(on)}	Turn-On Delay Time	—	8.8	—	ns	V _{DD} = 15V, V _{GS} = 4.5V ④ I _D = 20A R _G = 1.8Ω See Fig. 14
t _r	Rise Time	—	30	—		
t _{d(off)}	Turn-Off Delay Time	—	9.4	—		
t _f	Fall Time	—	6.5	—		
C _{iss}	Input Capacitance	—	1030	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	350	—		
C _{rss}	Reverse Transfer Capacitance	—	110	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②⑥	—	93	mJ
I _{AR}	Avalanche Current ①	—	20	A
E _{AR}	Repetitive Avalanche Energy ①	—	6.5	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	65④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	260		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	17	26	ns	T _J = 25°C, I _F = 20A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	24	36	nC	di/dt = 300A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

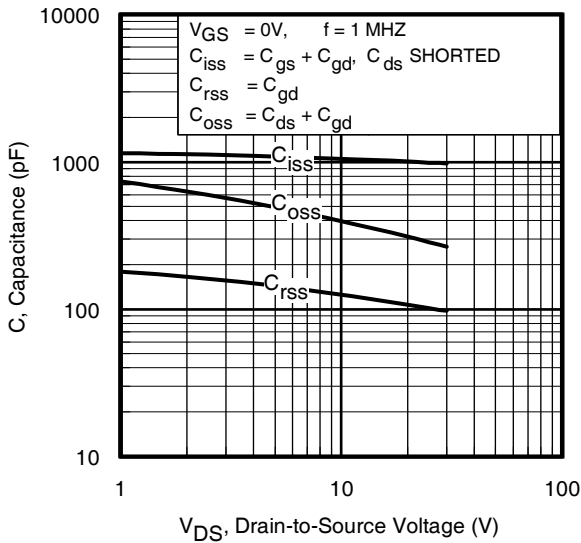


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

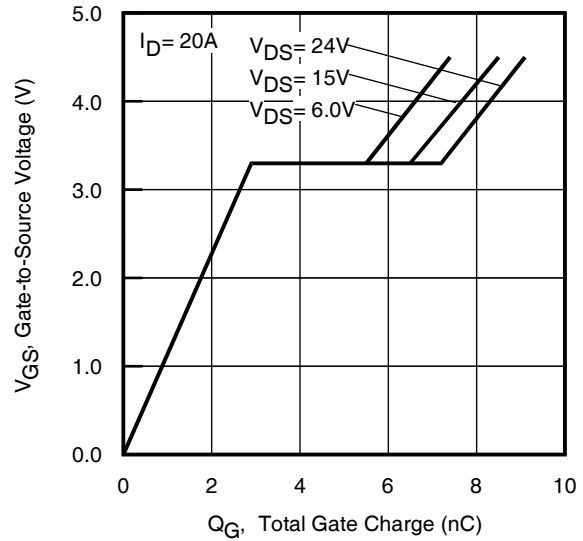


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

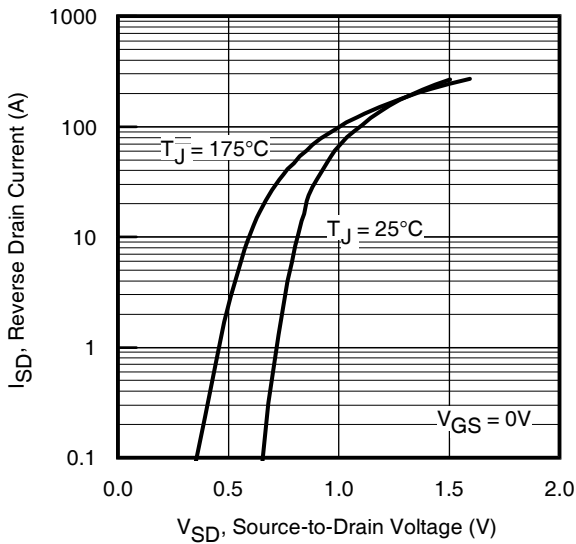


Fig 7. Typical Source-Drain Diode Forward Voltage

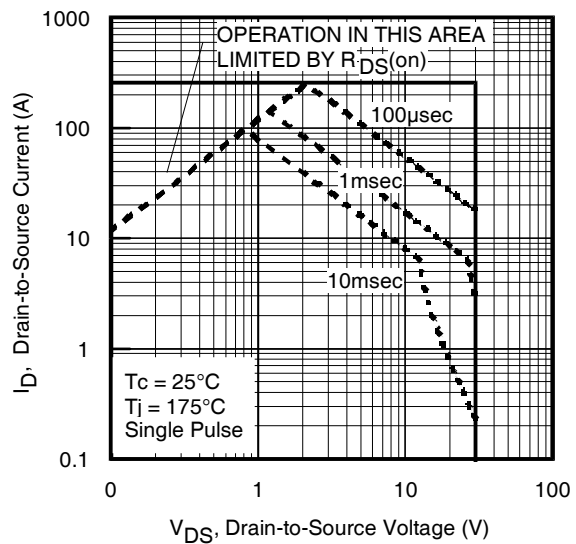
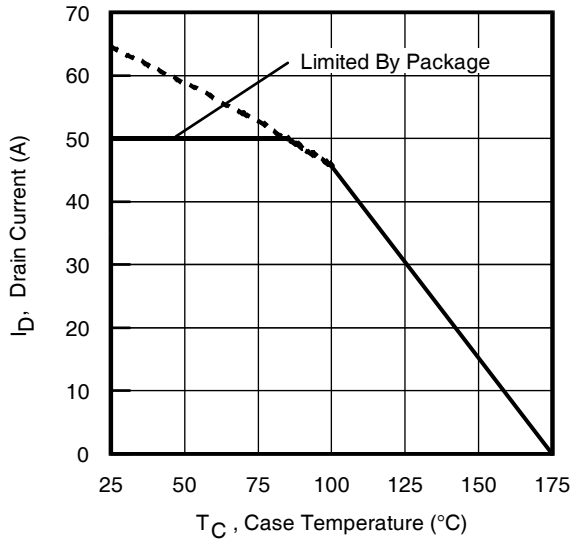
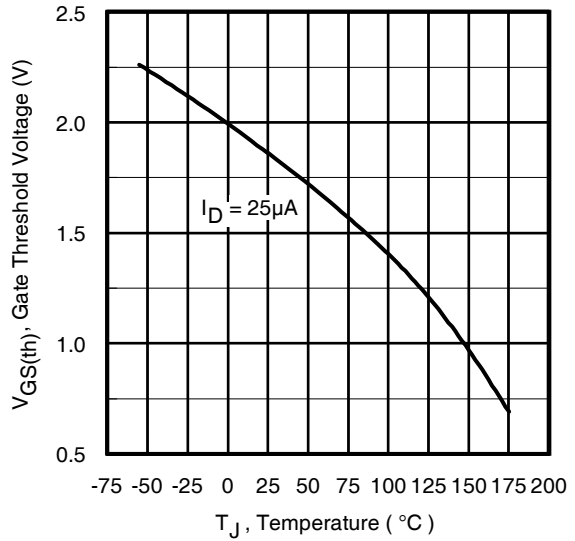
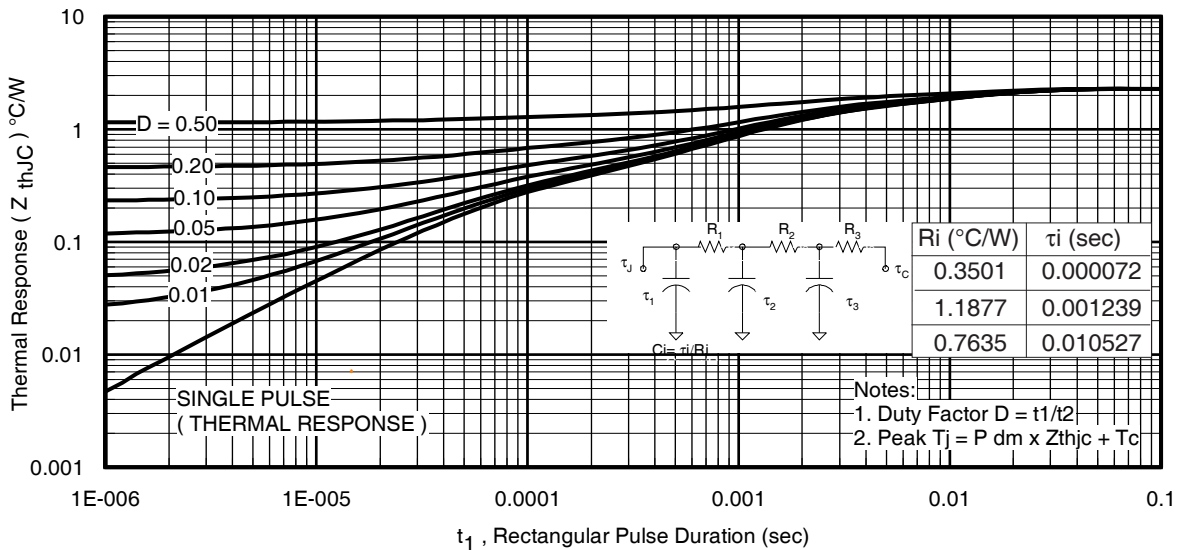
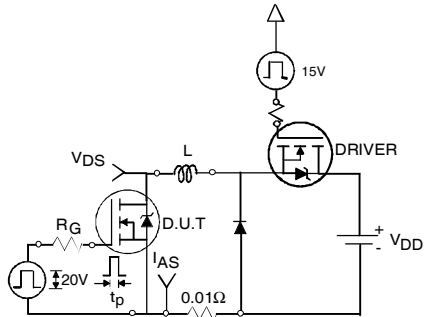
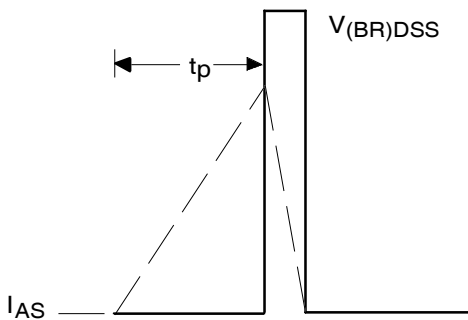
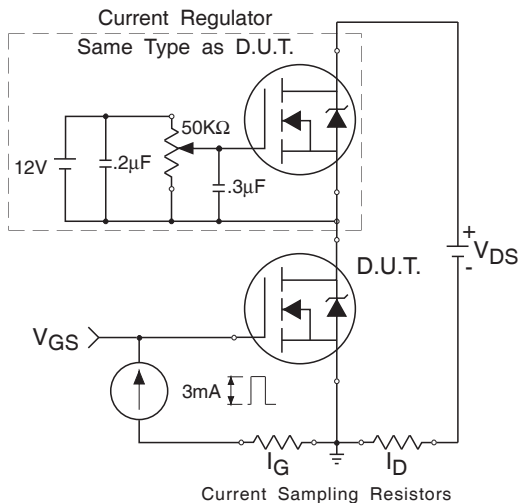
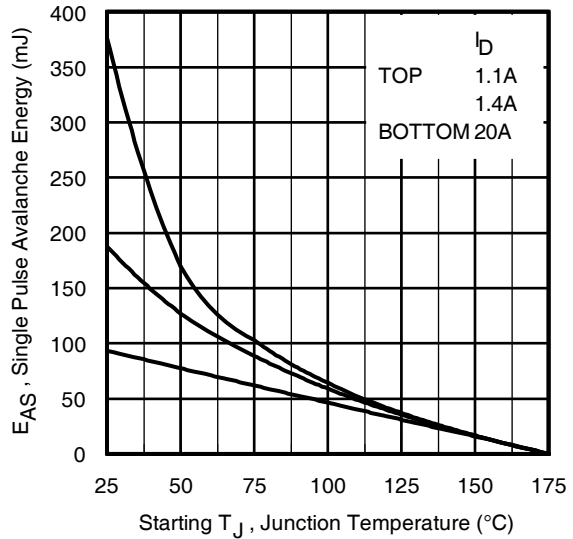
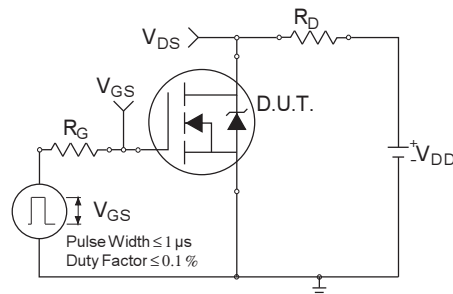
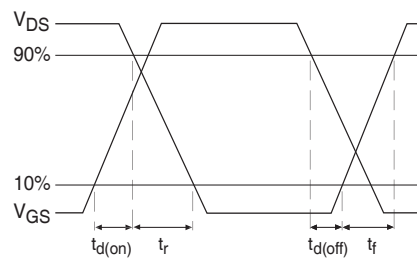


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13. Gate Charge Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 14a. Switching Time Test Circuit

Fig 14b. Switching Time Waveforms

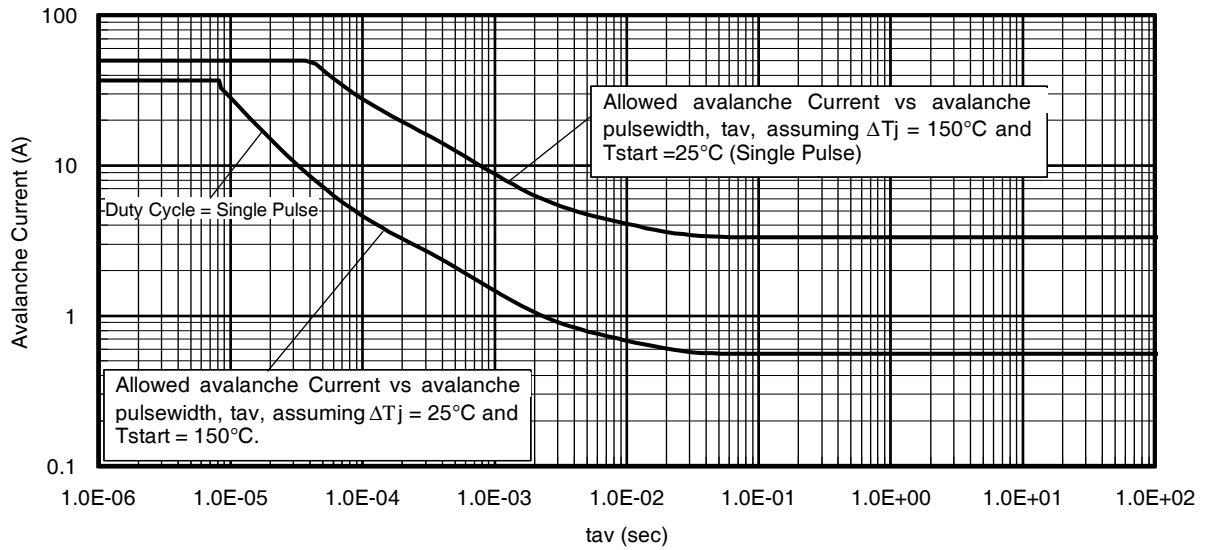


Fig 15. Typical Avalanche Current vs. Pulsewidth

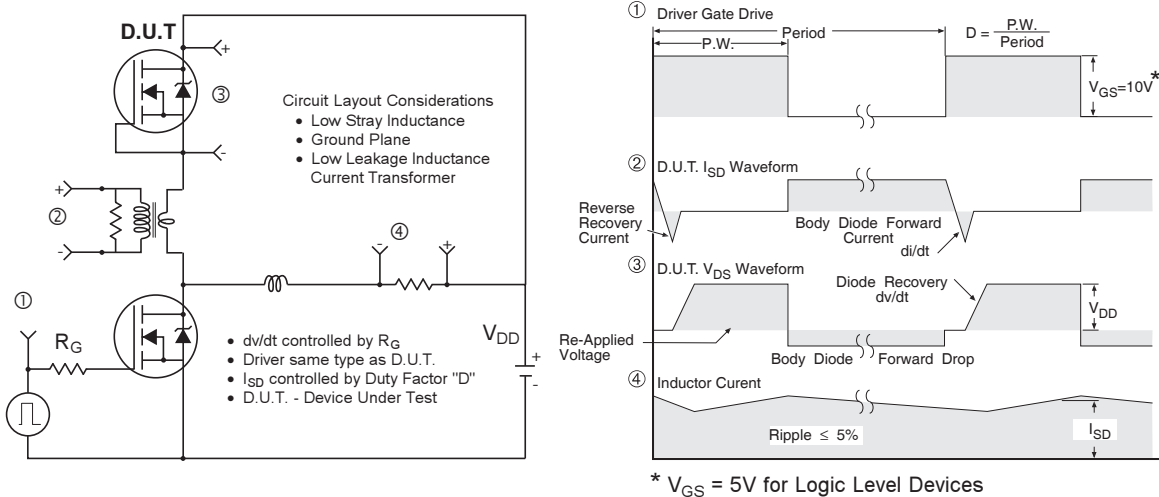


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

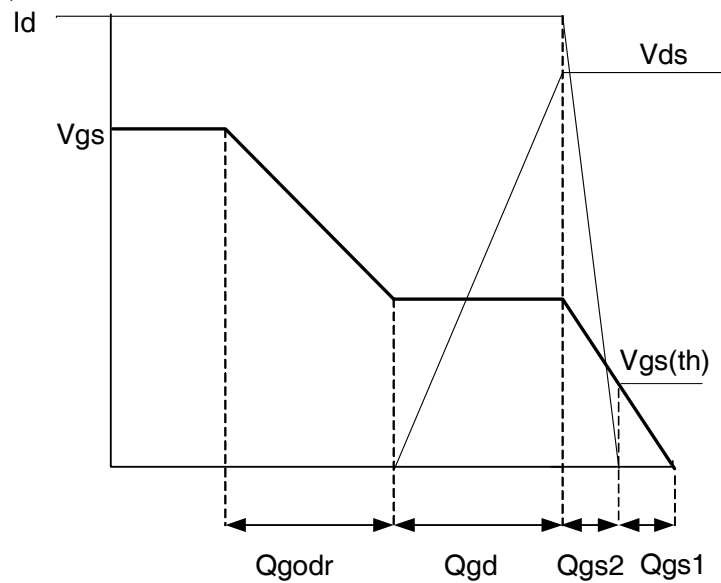


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + (Q_{rr} \times V_{in} \times f)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

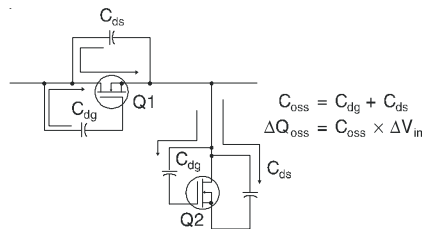
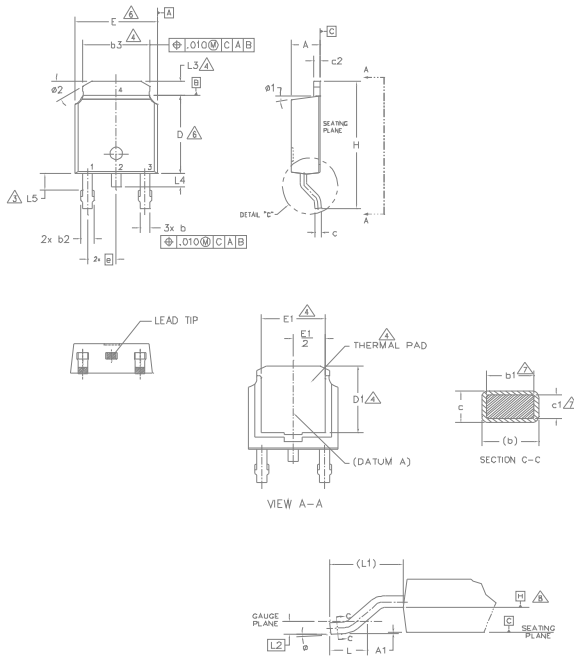


Figure A: Q_{oss} Characteristic

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE WELD FLASH. WELD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.75	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
phi	0"	10"	0"	10"	
phi 1	0"	15"	0"	15"	
phi 2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

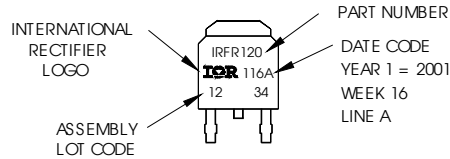
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

"P̄" in assembly line position indicates
"Lead-Free" qualification to the consumer-level

OR

INTERNATIONAL
RECTIFIER
LOGO



PART NUMBER

DATE CODE

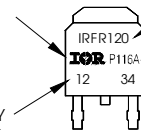
YEAR 1 = 2001

WEEK 16

LINE A

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE



PART NUMBER

DATE CODE

P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)

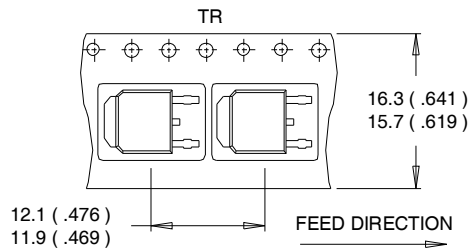
P̄ = DESIGNATES LEAD-FREE
PRODUCT QUALIFIED TO THE
CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001

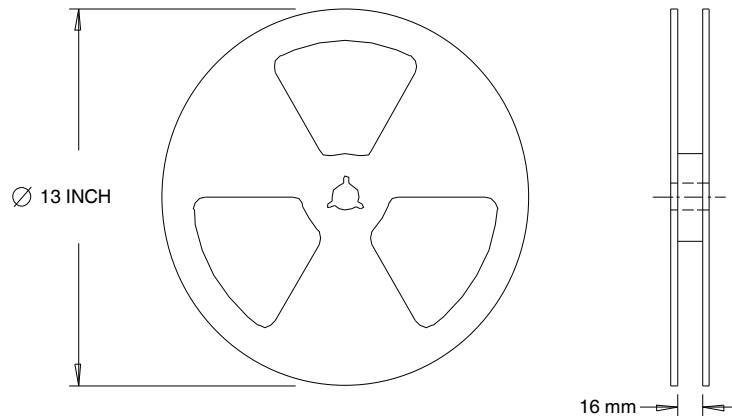
WEEK 16

A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))

NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industriid (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	D-Pak	MSL1
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

^{††} Applicable version of JEDEC standard at the time of product release

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.47\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 20\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 50A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>