LUMINARY MICRO™

Stellaris® Family Development Board

USER'S MANUAL

DM-LM3SFAM-04

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Revision History

This table provides a summary of the document revisions.

Date	Revision	Description
March 2006	00	Initial release of doc to customers.
May 2006	01	Release of DB48 daughterboard and documentation.
May 2006	02	Added missing DB48 schematics to board manual PDF.
July 2006	03	Switched DB48 Layout 1 and Layout 2 figures so most current board is first. Added QEI text to Headers paragraph in Chapter 1.
February 2007	04	Release of revision 3 of motherboard, which adds two headers: JP34 and JP35.

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CHAPTER 1

Stellaris® Family Development Board

The Stellaris® Family Development Board provides a platform for product development. Hardware and software engineers use this board for evaluation of Stellaris™ family microcontroller features and functionality, and for software development.

The development board includes the Stellaris motherboard and a daughterboard with a Stellaris family microcontroller. The DB28 daughterboard is available for 28-pin SOIC devices, and the DB48 daughterboard is available for 48-pin LQFP devices. These daughterboards are described in Chapter 2, “DB28 Daughterboard” on page 21 and Chapter 3, “DB48 Daughterboard” on page 27.

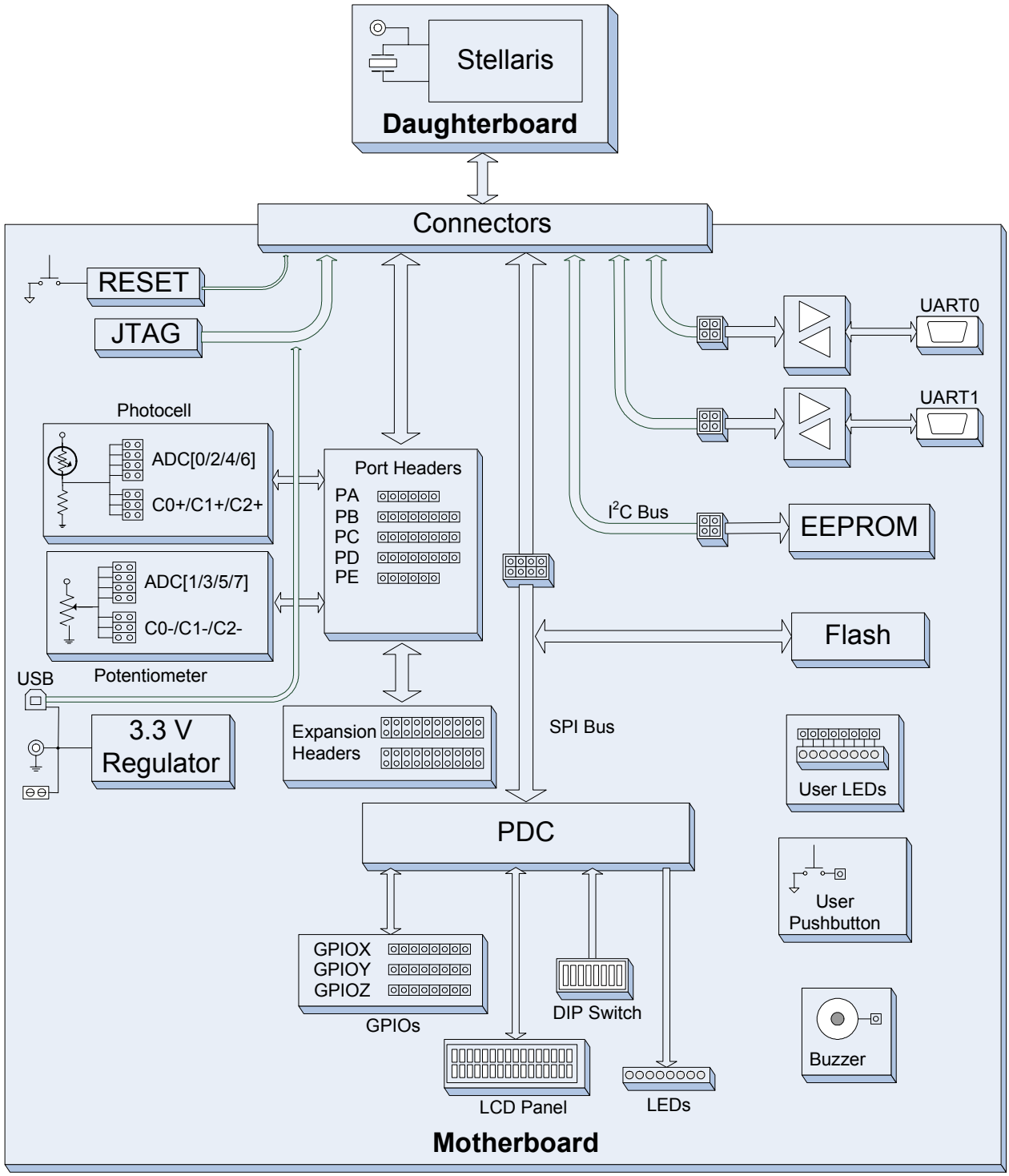
Features

The Stellaris® Family Development Board includes the following features. Note that not all features are implemented on all Stellaris microcontrollers.

- Daughterboards enable support for multiple package/pin-out options
- Two UART transceivers and DB9 male connectors
- All I/O available on headers
- One potentiometer and one photocell for driving the Analog-to-Digital Converter (ADC) and comparator inputs
- Eight user LEDs and one pushbutton for use with the Stellaris GPIOs
- Standard ARM® 20-pin JTAG debug connector
- USB 2.0 full speed interface allows JTAG/SWD debug without in-circuit emulator (ICE)
- 8-Kbit I^2C EEPROM memory
- 1-Mbit SPI-based flash memory
- One buzzer for PWM use
- 32.768-KHz oscillator for real-time clock
- External reset switch and power-on reset supervisor
- 5-V and 3.3-V LED power indicators
- User-prototype area
- Peripheral Device Controller (PDC) CPLD for interface with the following:
  - 16 character by 2-line LCD display
  - 8 status LEDs
  - 8-position dual-inline package (DIP) switch
  - 24 GPIOs

Block Diagram

Figure 1-1. Stellaris® Family Development Board Block Diagram



Functional Description

Daughterboard

The daughterboard contains the Stellaris microcontroller and connects to the motherboard with four 21-pin connectors. The Stellaris PLL clock is generated from a 6-MHz crystal provided on pin sockets for easy crystal changes. An optional SMA connector can be used to drive an external clock source.

UART

Two UART transceivers and DB9 connectors are provided to connect with the Stellaris microcontroller UART peripherals. The UART0 peripheral (TX, RX) is included in all Stellaris microcontrollers; UART1 is available in all 48-pin microcontrollers except the LM3S301. On the LM3S101, LM3S102 and LM3S301, UART1 is available for external use.

Headers

All Stellaris I/O signals are available on five 8-pin GPIO headers labeled Port A through Port E to match the Stellaris microcontroller GPIO ports. For each port header, pin 1 is bit 0 and pin 8 is bit 7 of the corresponding Stellaris GPIO. For example, Port B pin 1 is PB0 and Port B pin 8 is PB7 of the Stellaris microcontroller. Note that ports A and E have only six I/O signals, with the remaining two header pins connected to ground. Jumper shunts are used to connect Stellaris signals to on-board devices to allow connect/disconnect. Stellaris signals can be rewired with the included fly-wires.

There are also two 20-pin expansion headers (J9 and J22). Header J9 is intended primarily as an interface for a motor driver board, and includes all the Stellaris PWM outputs, QEI inputs, analog comparator inputs, and three ADC inputs. Header J22 has the remaining Stellaris signals, and includes UART, SSI, I^2C, JTAG, and timer CCP input signals.

NOTE: PWM, QEI, ADC, I^2C, and analog comparators are available on select Stellaris microcontrollers.

Potentiometer

One potentiometer is included to drive selected Analog-to-Digital Converter (ADC) inputs and/or analog comparator inputs. The voltage range is 0 to 3.0. Shunt headers are used for signal selection.

NOTE: ADC and analog comparators are available on select Stellaris microcontrollers.

Photocell

One photocell is included to drive selected ADC inputs and/or analog comparator inputs. The voltage range is 0 to 3.0. Shunt headers are used for signal selection.

NOTE: ADC and analog comparators are available on select Stellaris microcontrollers.

User LEDs

Eight user LEDs (ULED0-ULED7) are provided for general use. Headers are provided for connectivity.

User Pushbutton

One user pushbutton (SW3) is provided for general use. A header is provided for connectivity.

JTAG Debug Connector

A standard 20-pin connector for JTAG debug is provided. This port is also used to access the Serial-Wire Debug (SWD) interface of the Stellaris microcontroller. When using this connector, the USB interface cannot be used for JTAG/SWD debug (USB can still be used for providing board power). A shunt jumper at location JP31 may be required when using this port.

USB Debug

A USB 2.0 full-speed interface provides debug capability via JTAG or SWD without the need for an ICE. Note that use of this interface requires installation of the corresponding USB drivers. When using this interface, the 20-pin JTAG connector cannot be used for JTAG/SWD debug. Ensure that no shunt jumper is present at location JP31.

I^2C EEPROM Memory

An 8-Kbit I^2C memory is included for use with the Inter-Integrated Circuit (I^2C) bus interface. A jumper block is provided for connecting this memory.

NOTE: The I^2C interface is available on select Stellaris microcontrollers.

SPI Flash Memory

A 1-Mbit SPI flash memory is included for use with the Serial Port Interface (SPI) port. A jumper block is provided for connecting this memory.

Buzzer

A buzzer is provided for use with one of the PWM outputs.

Real-Time Clock

A 32.768-KHz crystal oscillator generates a clock signal that can be used to drive the Stellaris real-time clock. Shunt jumpers on the daughterboard can be used to connect this clock source.

External Reset

The external reset is implemented with a reset switch SW2 connected to a reset supervisor circuit, and provides a system reset signal.

Prototype Area

A prototype area is provided for implementing user circuits. To supply power, there are power and ground rows. The prototype area is indicated on the board with a Luminary Micro logo (see Figure 1-2 on page 13).

Peripheral Device Controller (PDC)

A Peripheral Device Controller (PDC) implemented with a CPLD is accessible via the SPI interface and provides access to several devices including a 16-character by 2-line LCD display, an 8-bit DIP switch, 8 general-purpose user LEDs, and 24 GPIOs.

Power Supply

The Stellaris® Family Development Board requires 5 volts at 500 mA for operation, and three options are provided for supply connection.

1. A USB connector can be used when connected to a high-power (500-mA) USB hub port.
2. A 5-V jack can be used with an external power supply.
3. A terminal block can be wired to a 5-V external bench supply.

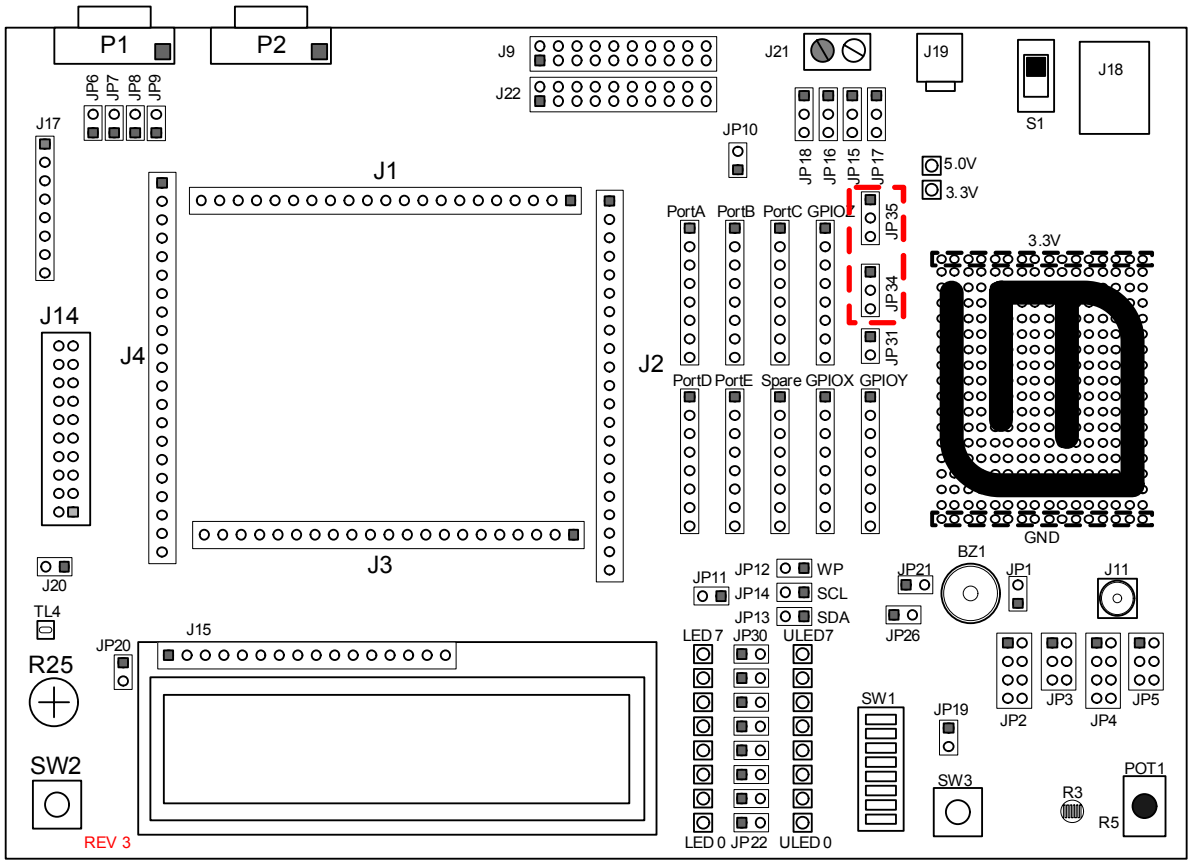
A slide switch selects between USB power and the other two options (see Figure 1-2 on page 13). Table 1-1 on page 16 describes how to select the power supply.

Motherboard Layout

The Stellaris™ family motherboard layout is shown in Figure 1-2. The gray squares show the location of pin 1 for all connectors and headers. (On the board silk-screen, white arrows indicate pin 1.) There are four ground test loops: TL1-TL4. TL5 is 5.0 V, and TL6 is 3.3 V.

NOTE: Two motherboard revisions are in production, Rev 2 and Rev 3. The revision is marked in the lower left corner of the board, as indicated in the figure. The only functional difference between these revisions is the addition in Rev 3 of headers JP34 and JP35 next to the GPIOZ headers to allow source selection for signals IDX (PD7 or PB2) and FAULT (PD6 or PB3). JP34 and JP35 are highlighted in the figure with a red box.

Figure 1-2. Stellaris Family Motherboard Layout



NOTE: The gray squares indicate the location of pin 1 for all connectors and headers.

Development Board Configuration

NOTE: In the descriptions that follow, reference designators are used to indicate locations on the board layout (as shown in Figure 1-2). In addition, reference designators in parenthesis refer to parts in the schematics in Appendix B, “Schematics.

Daughterboard Installation

The daughterboard connects to the motherboard header connectors J1-J4. With no power applied to the motherboard, place the daughterboard and align each connector of the motherboard with the corresponding daughterboard connector. Press the daughterboard down until the daughterboard is firmly seated, and visually inspect all four connectors to ensure proper connection before proceeding.

UART

To connect the UART0 transceiver, connect shunt jumpers on headers JP6 and JP7. To connect UART1, connect shunt jumpers on headers JP8 and JP9.

SPI Port (On-Board Peripherals)

To connect the Serial Peripheral Interface port, which is used to communicate with the PDC and the on-board flash memory, connect shunt jumpers to pins 1-2 of headers JP15, JP16, JP17, and JP18. To write-protect the SPI flash memory, place a shunt jumper on JP10.

NOTE: The Stellaris microcontroller’s SSI port can be programmed for one of three serial modes: Freescale SPI, National Semiconductor MICROWIRE™, or Texas Instruments synchronous serial. (The mode is set with the `FRF` bit in the **SSI Control0 (SSICR0)** register.) The Stellaris Family Development Board is designed for use with SPI mode although MICROWIRE and TI synchronous serial modes can be used when implementing user circuits in the prototype area. SPI mode must be set to use the board’s LCD, DIP switch, LEDs, and GPIOX, GPIOY, and GPIOZ ports.

I^2C Port

To connect the I^2C port for access to the on-board EEPROM, place shunt jumpers on JP13 and JP14. To write-protect the EEPROM memory, place a shunt jumper on JP12. Address line A2 for the EEPROM memory can be set to 0 by placing a shunt jumper on JP11. Removing the jumper sets A2 to 1.

NOTE: The I^2C interface is available on select Stellaris microcontrollers.

Buzzer

To enable the buzzer BZ1, connect a shunt jumper to JP21. To connect the buzzer power driver to the Stellaris microcontroller PB0 port, place a shunt jumper on JP26. To use a different port to drive the buzzer, remove the shunt at JP26 and connect a fly-wire from the desired port to JP26-2.

LCD Panel, DIP Switch, LEDs, and GPIOs

To use the LCD panel, DIP switch, LEDs LED0-LED7 (D1-D8), and the GPIOs, the SPI port must be connected as described above. The SPI port connects to the PDC to control these devices.

The potentiometer R25 is used to adjust the contrast of the LCD panel. The LCD panel, DIP switch, LEDs, and GPIOs are controlled with the PDC registers (see Table 1-4 on page 18).

User Pushbutton

Pushbutton SW3 is available for general use. To connect this switch to PB4, place a shunt jumper on JP19. To use a different port, remove shunt at JP19 and connect a fly-wire from the desired port to JP19-2.

User LEDs

User LEDs ULED0-ULED7 (D9, D10, D12, D13-D17) are available for general use. Each user LED has an associated header for connection to a Stellaris GPIO, PDC GPIO, or external circuitry.

To connect a user LED to its associated Stellaris GPIO, place a shunt jumper on the corresponding header (ULED0-ULED3 => PB0-PB3, ULED4-ULED7 => PD0-PD3). To use a different port, remove the shunt jumper from the header and connect a fly-wire from the desired port to pin 2 of the header.

Photocell

Photocell R3 can be used to provide an analog signal to drive the ADC (analog-to-digital converter) and the analog comparator using headers JP2 (ADC0,ADC2,ADC4,ADC6) => (PE5,PE3,PD7,PD5), and JP3 (C0+,C1+,C2+) => (PB6,PC5,PC6). To connect the photocell to an ADC channel, place a shunt jumper on the corresponding JP2 header. To connect the photocell to a comparator channel, place a shunt jumper on the corresponding JP3 header.

NOTE: ADC and analog comparators are available on select Stellaris microcontrollers.

Potentiometer

Potentiometer R5 can be used to provide an analog signal to drive the ADC (analog-to-digital converter) and the analog comparator using headers JP4 (ADC1,ADC3,ADC5,ADC7) => (PE4,PE2,PD6,PD4), and JP5 (C0-,C1-,C2-) => (PB4,PB5,PC7). To connect the potentiometer to an ADC channel, place a shunt jumper on the corresponding JP4 header. To connect the potentiometer to a comparator channel, place a shunt jumper on the corresponding JP5 header.

NOTE: ADC and analog comparators are available on select Stellaris microcontrollers.

JTAG Debug Connector

For JTAG debug with an external ICE, connect the ICE to connector J14 with a standard 20-pin JTAG debug cable. To link the motherboard reset to the JTAG emulator reset, place a shunt jumper on JP20. Depending on the ICE, a shunt jumper at location JP31 may be required if a USB driver conflict occurs.

USB Debug

For debug with USB, connect the USB cable to the USB device connector. Ensure that no shunt jumper is present at location JP31. Note that a corresponding USB driver must be installed on the host computer. The USB driver selects the mode of operation by controlling the USB_MOD signal from the FTDI part (ADBUS7). If USB_MOD is 1, JTAG mode is selected. If USB_MOD is 0, SWD mode is selected. JTAG/SWD signals are driven to the Stellaris microcontroller when the USB driver sets USB_DEN (ADBUS6) to 0.

32.768-KHz Clock Oscillator

An on-board 32.768-KHz oscillator can be used to drive the Stellaris real-time clock. To enable this oscillator, remove the shunt jumper on JP1. To disable the oscillator output, place a shunt jumper on JP1.

Reset Switch

Reset switch SW2 generates a 140-ms (minimum) system reset signal. Powering up the board also generates a 140-ms system reset signal. A shunt jumper can be placed on JP20 to link the JTAG emulator reset with the system reset.

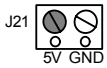
GPIO Headers

All Stellaris GPIO ports are available on 8-pin headers labeled PortA (J5), PortB (J6), PortC (J7), PortD (J10), and PortE (J12). The 20-pin headers J9 and J22 include all the GPIOs and provide a convenient connection for expansion to another board. The 8-pin headers labeled GPIOX (J26), GPIOY (J27), and GPIOZ (J16) provide a connection to the GPIOs implemented in the PDC.

Power

Three options are available for board power, and only one should be connected to the board. These are described in Table 1-1. The two power indicators light once there is power to the board.

Table 1-1. Possible Board Power Sources

Power Source	Configuration
USB high-power hub (500 mA)	Slide switch S1 towards the board edge. Connect a USB cable from the USB hub to the USB-B receptacle J18. Slide switch S1 towards the board center to turn on power.
5-V (500-mA) supply with 2.5-mm plug	Slide switch S1 towards the center of the board. Connect a 5-V supply with a 2.5-mm plug to jack J19. Slide switch S1 towards the board edge to turn on power.
5-V (500-mA) bench supply	Slide switch S1 towards the center of the board. Connect a 5-V supply with two wires to terminal block J21. Connect the 5-V wire to J21-1 (5V) and the ground wire to J21-2 (GND). Slide switch S1 towards the board edge to turn on power. 

Peripheral Device Controller (PDC)

The PDC provides access to a common set of peripherals across all Stellaris microcontrollers, since they all include an SSI port. The Stellaris SSI port is used in SPI mode for communications with the PDC. The PDC operates at 1 MHz.

Stellaris Microcontroller to PDC Interface

The Stellaris microcontroller connects to the PDC with a SPI port using the signals shown in Table 1-2.

Table 1-2. Stellaris Microcontroller to PDC Interface

Board Signal	Direction	Description
SPI_CLK	Input	SPI clock signal, 1 MHz.
SPI_SEL	Input	SPI select signal, set high to enable SPI transfers. Set to low for reset of the PDC (minimum 200 nanoseconds). Note that with SPI_SEL low the SPI flash at location U3 is selected.
SPI_MOSI	Input	Master output, slave input data transfer signal.
SPI_MISO	Output	Master input, slave output data transfer signal.

PDC I/O

The PDC connects to supported peripherals with the following signals:

Table 1-3. Peripheral to PDC Interface

Board Signal	Direction	Description
L_RS	Out	LCD register select
L_RW	Out	LCD read/write
L_CEN	Out	LCD chip enable
L_BLIGHT	Out	LCD backlight
LD[7:0]	InOut	LCD data bus
LED[7:0]	Out	LED select outputs
DSW[7:0]	In	DIP switch inputs
GPIOX_[7:0]	InOut	GPIOX I/O ports
GPIOY_[7:0]	InOut	GPIOY I/O ports
GPIOZ_[7:0]	InOut	GPIOZ I/O ports

PDC Registers

PDC registers are 8 bits, and there are three types: Read-Only (RO), Read/Write (R/W), and Read/Write delayed (RWD). A RWD transaction requires an additional dummy transfer due to peripheral device latency.

Table 1-4. PDC Registers

Register	Address	Type	Description
VERSION	0x0	R0	The **VERSION** register contains the version of the PDC design programmed in the CPLD.
CSR	0x1	R/W	The **Command/Status (CSR)** register is used to set special configuration options and read device status. Unused bits are reserved and should be written to 0. The following bits are defined: **Bit0 - LCBL:** The LCD backlight bit controls the LCD panel backlight. Setting this bit to 1 turns on the LCD backlight. Setting this bit to 0 turns off the LCD backlight. **Bit7 - LCBSY:** The LCD busy bit reflects the value of the LCD panel busy flag. When this bit is 1, the LCD panel is busy processing a command. When this bit is 0, a new command can be written to the LCD panel.
DIPSW	0x4	R0	The **DIP Switch (DIPSW)** register contains the value of the debug DIP switch at location SW1. Bit i corresponds to switch i+1. A switch in the OFF position is read as 0. A switch in the ON position is read as 1.
LED	0x5	R/W	The **LED Output (LED)** register controls LED0-LED7. Bit i controls LEDi. Writing a bit to 1 turns on the corresponding LED. Writing a bit to 0 turns off the corresponding LED.
LCDCSR	0x6	RWD	The **LCD Command/Status (LCDCSR)** register is used to write configuration and control commands and to read status information from the LCD panel. For more information, refer to the CFAH1602B LCD panel data sheet (available from www.crystalfontz.com).
LCDRAM	0x7	RWD	The **LCD RAM (LCDRAM)** register is used to write and read the LCD display data RAM (DDRAM) and the character generator RAM (CGRAM). For more information, refer to the CFAH1602B LCD panel data sheet (available from www.crystalfontz.com).
GPXDAT	0x8	R/W	The **GPIOX Data (GPXDAT)** register is used to access the general-purpose I/O port GPIOX at location J26. Bit i corresponds with the GPIOX_i port signal. Each bit can be configured for input or output in the **GPXDIR** register. Writing a bit to 1 sets the corresponding GPIOX port signal to 1 if the port signal is configured as an output. Writing a bit to 0 sets the corresponding GPIOX port signal to 0 if the port signal is configured as an output. Reading a bit reads the value of the corresponding GPIOX port signal. If the GPIOX port is 0, the bit will read as 0. If the GPIOX port signal is 1, the bit will read as 1. Note that a read of the **GPXDAT** register always reads the GPIOX port signals, not the internal register.

Table 1-4. PDC Registers

Register	Address	Type	Description
GPXDIR	0x9	R/W	The **GPIOX Direction (GPXDIR)** register is used to select the data transfer direction for the **GPXDAT** register. Bit i corresponds to GPXDAT bit i. Writing a bit to 1 sets the corresponding **GPXDAT** bit as an output port. Writing a bit to 0 sets the corresponding **GPXDAT** bit as an input port.
GPYDAT	0xA	R/W	The **GPIOY Data (GPYDAT)** register is used to access the general-purpose I/O port GPIOY at location J27. Bit i corresponds with the GPIOY_i port signal. Each bit can be configured for input or output in the **GPYDIR** register. Writing a bit to 1 sets the corresponding GPIOY port signal to 1 if the port signal is configured as an output. Writing a bit to 0 sets the corresponding GPIOY port signal to 0 if the port signal is configured as an output. Reading a bit reads the value of the corresponding GPIOY port signal. If the GPIOY port is 0, the bit will read as 0. If the GPIOY port signal is 1, the bit will read as 1. Note that a read of the **GPYDAT** register always reads the GPIOY port signals, not the internal register.
GPYDIR	0xB	R/W	The **GPIOY Direction (GPYDIR)** register is used to select the data transfer direction for the **GPYDAT** register. Bit i corresponds with **GPYDAT** bit i. Writing a bit to 1 sets the corresponding **GPYDAT** bit as an output port. Writing a bit to 0 sets the corresponding **GPYDAT** bit as an input port.
GPZDAT	0xC	R/W	The **GPIOZ Data (GPZDAT)** register is used to access the general-purpose I/O port GPIOZ at location J16. Bit i corresponds with the GPIOZ_i port signal. Each bit can be configured for input or output in the **GPZDIR** register. Writing a bit to 1 sets the corresponding GPIOZ port signal to 1 if the port signal is configured as an output. Writing a bit to 0 sets the corresponding GPIOZ port signal to 0 if the port signal is configured as an output. Reading a bit reads the value of the corresponding GPIOZ port signal. If the GPIOZ port is 0, the bit will read as 0. If the GPIOZ port signal is 1, the bit will read as 1. Note that a read of the **GPZDAT** register always reads the GPIOZ port signals, not the internal register.
GPZDIR	0xD	R/W	The **GPIOZ Direction (GPZDIR)** register is used to select the data transfer direction for the **GPZDAT** register. Bit i corresponds with **GPZDAT** bit i. Writing a bit to 1 sets the corresponding **GPZDAT** bit as an output port. Writing a bit to 0 sets the corresponding **GPZDAT** bit as an input port.

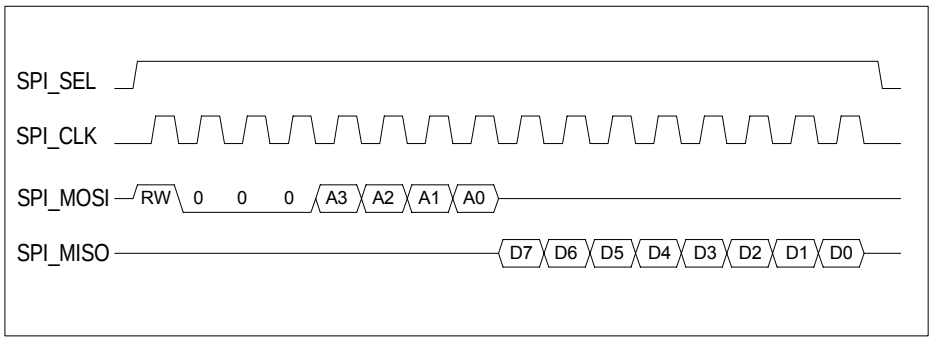
SPI Protocol

The SPI slave interface is enabled when `SPI_SEL` goes High. All SPI commands and data are received via the `SPI_MOSI` input signal, with data sampled on the rising edge of the SPI clock. All SPI output data is transmitted on the `SPI_MISO` output signal, with data shifted out on the falling edge of the SPI clock. Set `SPI_SEL` Low for 200 nanoseconds to reset the PDC.

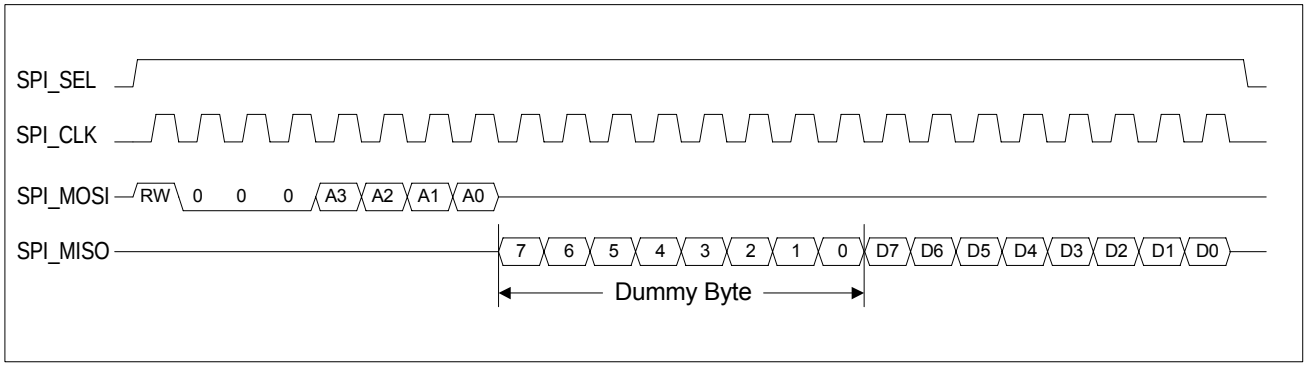
Every transaction is composed of at least two 8-bit SPI transfers. The first byte contains a 4-bit address on the lower bits (bits 3:0) and a read/write (R/W) bit to indicate transfer direction on the most significant bit (bit 7). The remaining bits (bits 6:4) are reserved and must be 0. The next byte is driven by the Stellaris microcontroller for write transfers (R/W bit=0), and by the PDC for read transfers (R/W bit=1). For read transfers to LCD registers, a dummy byte follows the first byte, with a valid data byte afterwards. Timing diagrams are shown in Figure 1-3.

Figure 1-3. PDC Timing Diagrams

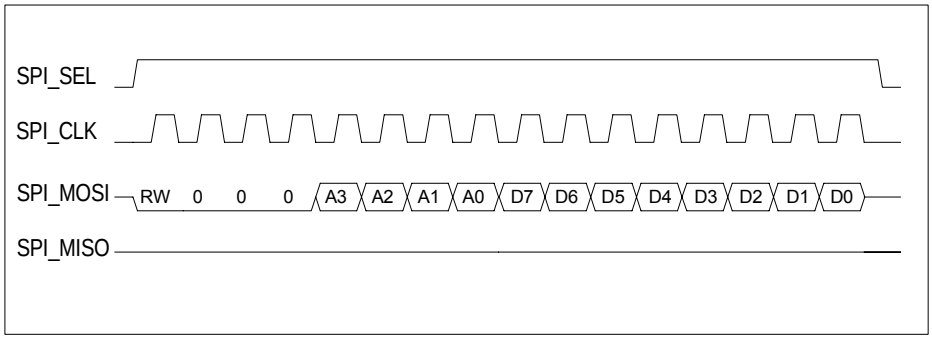
PDC Read Transfer



LCD Read Transfer



PDC/LCD Write Transfer



CHAPTER 2

DB28 Daughterboard

The DB28 daughterboard contains a 28-pin SOIC Stellaris microcontroller and connects to the motherboard with four 21-pin connectors.

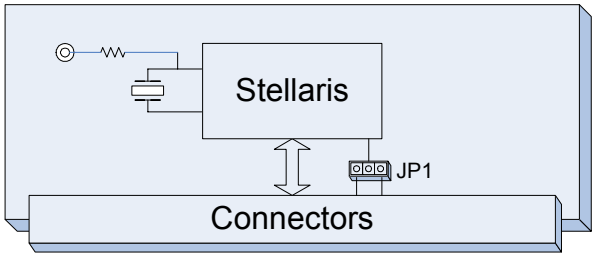
NOTE: In the descriptions that follow, reference designators are used to indicate locations on the board layout (as shown in Figure 2-2 on page 23). In addition, reference designators in parenthesis refer to parts in the schematics in Appendix B, “Schematics.

Features

- Designed for 28-pin SOIC Stellaris microcontroller
- 6-MHz crystal mounted on pin sockets for easy crystal changes
- SMA connector for external clock
- Power and ground test loops
- Jumper-selectable 32.768-KHz clock
- All daughterboard connector signals accessible via headers on the daughterboard

Block Diagram

Figure 2-1. DB28 Daughterboard Block Diagram



Daughterboard Interface

The DB28 daughterboard connects to the motherboard with four connectors: J1-J4 (see Figure 1-2 on page 13). Table 2-1 on page 22 lists the connections.

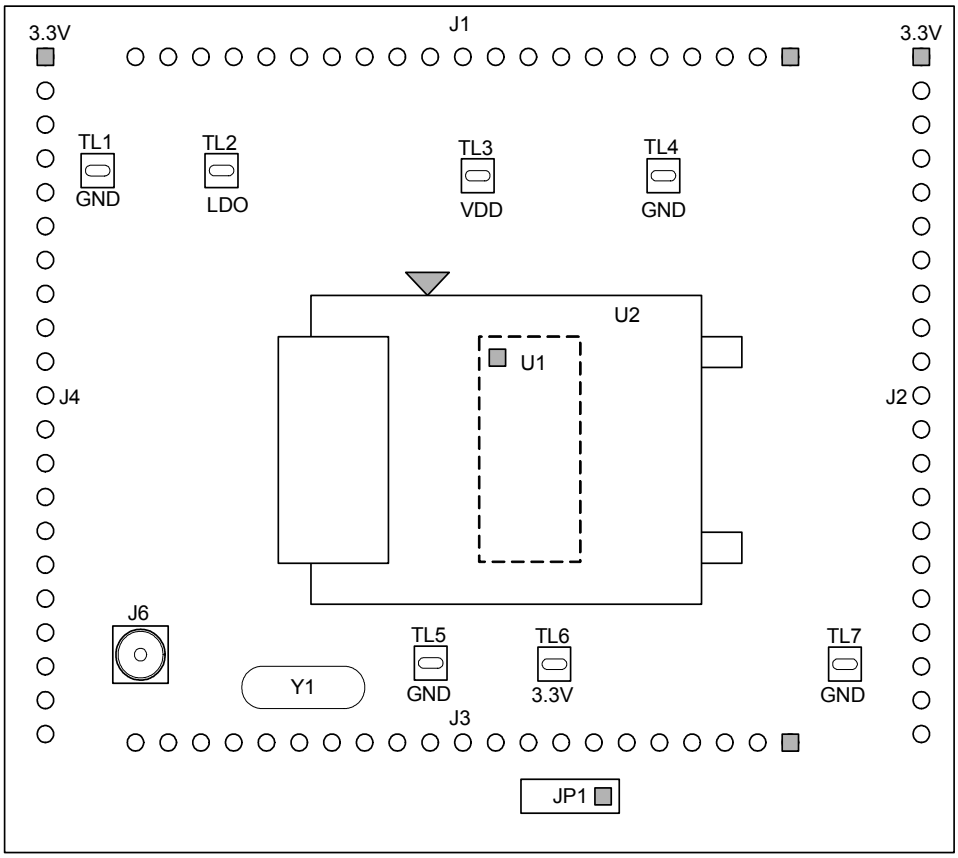
Table 2-1. DB28 Daughterboard Interface

Pin	J1	J2	J3	J4
1	GND	3.3V		3.3V
2			GND	
3				
4				
5				XPB1
6				PB0
7			CLK32K	
8			GND	
9				PB2
10				PB3
11	5V			
12	RSTn			
13				PA2
14				PA5
15				PA4
16	PC3/TDO			PA3
17				
18	PC0/TCK		PB6	
19	PC1/TMS		PB5	PA0
20	PC2/TDI		PB4	PA1
21	PB7/TRST	GND		GND

Daughterboard Layout

The DB28 daughterboard layout is shown in Figure 2-2 on page 23. A single Stellaris microcontroller is soldered at location U1. There are four ground test loops: TL1, TL4, TL5, and TL7. TL2 is connected to the LDO pin and TL3 is connected to VDD. The gray squares show the location of pin 1 for each connector. Note that TL6 and pin 1 of J2 and J4 are 3.3 V. A clock signal can be applied to SMA connector J6 after removing crystal Y1.

Figure 2-2. DB28 Daughterboard Layout



NOTE: The gray squares indicate the location of pin 1.

Shunt Jumper

There is a single shunt jumper JP1 (see Figure 2-2) used for selecting the connection of port B1 (PB1) as shown in Table 2-2.

Table 2-2. Jumper Settings for DB28 Daughterboard

Shunt	Description
No shunt	PB1 is unconnected
Shunt 1-2	PB1 is connected to 32.768-KHz clock
Shunt 2-3	PB1 is connected to daughterboard connector J4-5 (XPB1)

Development Board Signal Usage

Table 2-3 shows the signal connectivity and usage between the DB28 daughterboard and the motherboard. For the jumpers column, the numbers in brackets show the jumper position.

Table 2-3. Development Board Signals Used by DB28 Daughterboard

Stellaris Signal	DB28 Daughterboard Connection	Motherboard Jumpers	Motherboard Signal	Description
PA0	J4-19	JP7-[1][2]	U0_RX	Serial port 0 receive
PA1	J4-20	JP6-[1][2]	U0_TX	Serial port 0 transmit
PA2	J4-13	JP15-[2][1]	SPI_CLK	Serial peripheral interface clock
PA3	J4-16	JP18-[2][1]	SPI_SEL	Serial peripheral interface select
PA4	J4-15	JP17-[2][1]	SPI_MISO	Serial peripheral interface master-in/slave-out
PA5	J4-14	JP16-[2][1]	SPI_MOSI	Serial peripheral interface master-out/slave-in
PB0	J4-6	JP26[1][2]	PWM	Buzzer signal
		JP22[1][2]	ULED0	User LED
PB1	JP1-[2][1]⇨(J3-7)		CLK32K	32.768-KHz clock
	JP1-[2][3]⇨(J4-5)	JP23-[1][2]	ULED1	User LED
PB2	J4-9	J4-9	I2C_SCL	I^2C clock signal to EEPROM
		JP24[1][2]	ULED2	User LED
PB3	J4-10	J4-10	I2C_SDA	I^2C data signal to EEPROM
		JP25[1][2]	ULED3	User LED
PB4	J3-20	JP5-[2][1]	C0-	Connects to 10k potentiometer
PB5	J3-19	JP5-[4][3]	C1-	Connects to 10k potentiometer
PB6	J3-18	JP3-[2][1]	C0+	Connects to photocell
PB7	J1-21	J14-3	TRST	JTAG signal, used by emulator
PC0	J1-18	J14-9	TCK	JTAG signal, used by emulator
PC1	J1-19	J14-7	TMS	JTAG signal, used by emulator
PC2	J1-20	J14-5	TDI	JTAG signal, used by emulator
PC3	J1-16	J14-13	TDO	JTAG signal, used by emulator
$\overline{RST}$	J1-12		SYSRST_B	Connects to reset supervisor
OSC0	J7, C4			Connects to pin socket and capacitor for crystal
OSC1	J8, C5			Connects to pin socket and capacitor for crystal
VDD-(U1)	TL6, J2-1, J4-1		3.3V	Connects to 3.3-V plane

Table 2-3. Development Board Signals Used by DB28 Daughterboard

Stellaris Signal	DB28 Daughterboard Connection	Motherboard Jumpers	Motherboard Signal	Description
GND	J1-1, J2-21 J3-8, J4-21		GND	Connects to ground plane
LDO				Connects to 1.3 microfarad capacitor and to test loop 2

CHAPTER 3

DB48 Daughterboard

The DB48 daughterboard contains a 48-pin LQFP Stellaris microcontroller and connects to the motherboard with four 21-pin connectors.

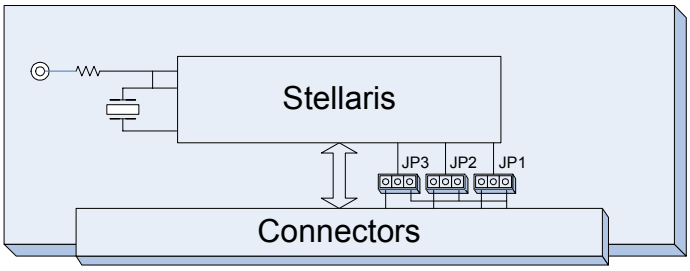
NOTE: In the descriptions that follow, reference designators are used to indicate locations on the board layout (as shown in Figure 3-2 on page 29 and Figure 3-3 on page 30). In addition, reference designators in parenthesis refer to parts in the schematics in Appendix B, “Schematics.

Features

- Designed for 48-pin LQFP Stellaris microcontroller
- 6-MHz crystal mounted on pin sockets for easy crystal changes
- SMA connector for external clock
- Power and ground test loops
- Jumper-selectable 32.768-KHz clock
- All daughterboard connector signals accessible via headers on the daughterboard

Block Diagram

Figure 3-1. DB48 Daughterboard Block Diagram



Daughterboard Interface

The DB48 daughterboard connects to the motherboard with four connectors: J1-J4 (see Figure 1-2 on page 13). Table 3-1 on page 28 lists the connections.

Table 3-1. DB48 Daughterboard Interface

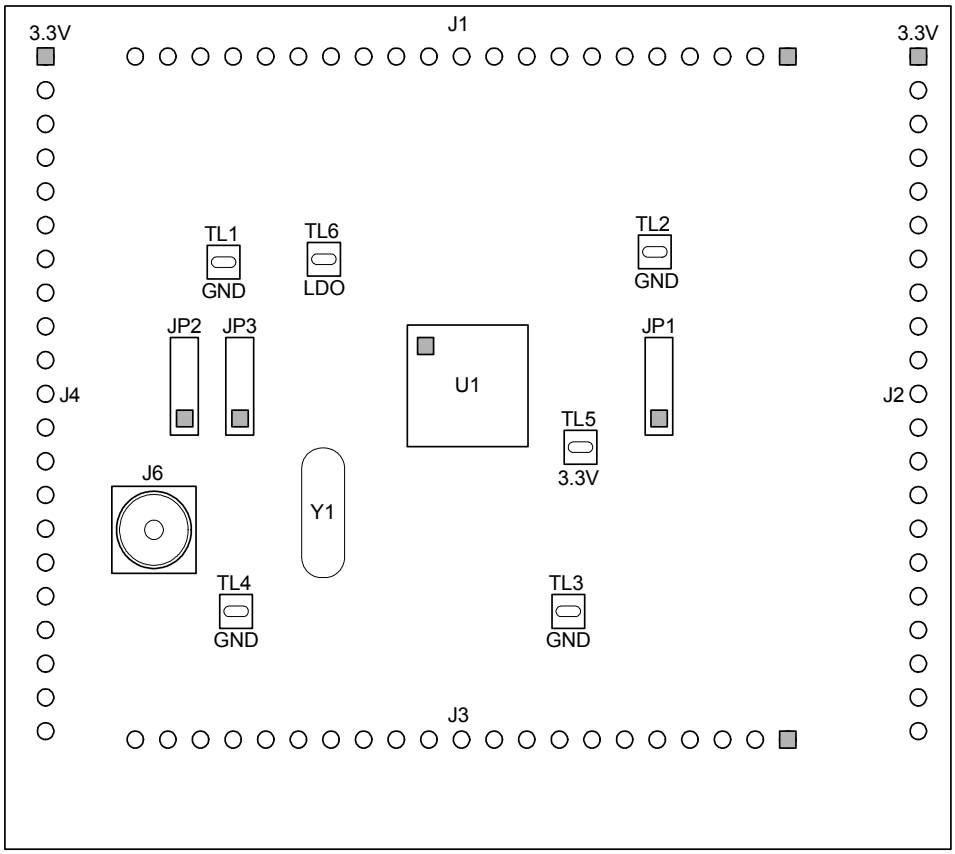
Pin	J1	J2	J3	J4
1	GND	3.3V		3.3V
2	PD7V		GND	
3	PC4	PE5		
4	PC6	PE4		
5				XPB1
6				PB0
7			CLK32K	XPE2
8			GND	
9				PB2
10		PD5		PB3
11	5V	PE3		
12	RSTn	PD4		
13				PA2
14				PA5
15		PE1		PA4
16	PC3/TDO	PE0	XPC7	PA3
17			PD6	PD2
18	PC0/TCK		PB6	PD3
19	PC1/TMS	PD1	PB5	PA0
20	PC2/TDI	PD0	PB4	PA1
21	PB7/TRST	GND	PC5	GND

Daughterboard Layout

There are two different layouts of the DB48 daughterboard. Layout 1 shown on Figure 3-2 on page 29 has the Stellaris microcontroller soldered at U1 on the center of the board. Layout 2 shown on Figure 3-3 on page 30 has the Stellaris microcontroller soldered at location U1 on the left side of the board.

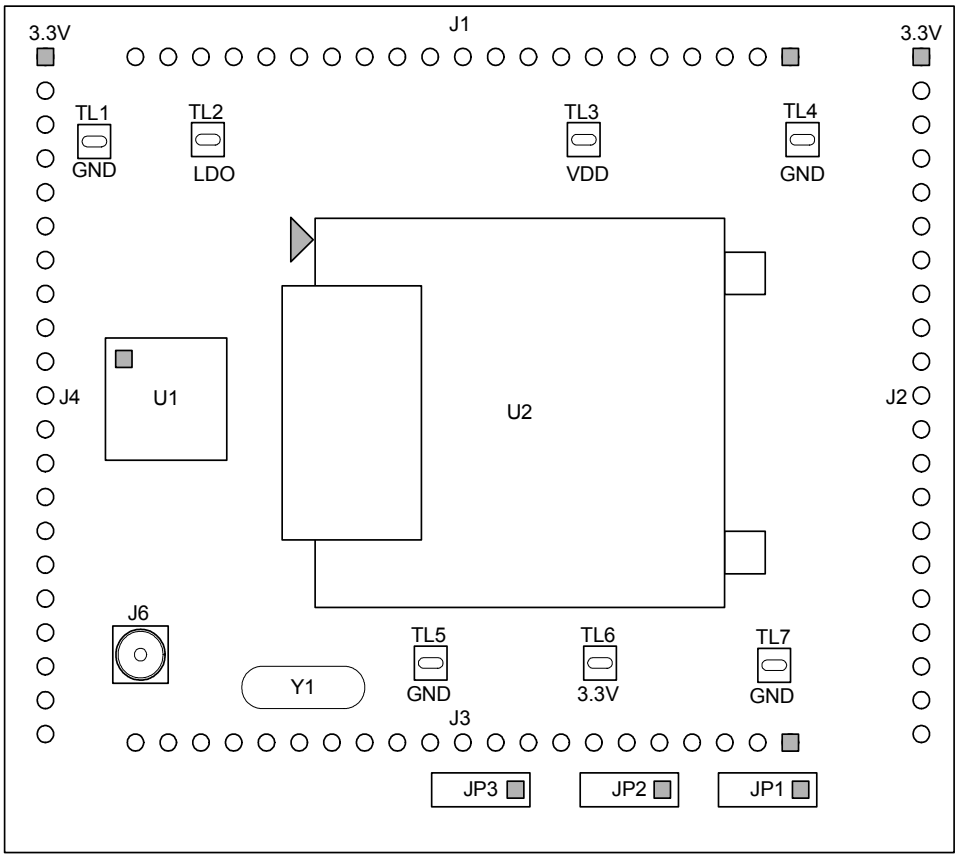
Both layouts include four ground test loops: TL1-TL4 in Layout 1 and TL1, TL4, TL5, and TL7 in Layout 2. TL6 in Layout 1 and TL2 in Layout 2 are connected to the LDO pin. The gray squares show the location of pin 1 for each connector. Note that TL5 in Layout 1 and TL6 in Layout 2 as well as pin 1 of J2 and J4 are 3.3 V. A clock signal can be applied to SMA connector J6 after removing crystal Y1.

Figure 3-2. DB48 Daughterboard Layout 1 (R3)



NOTE: The gray squares indicate the location of pin 1.

Figure 3-3. DB48 Daughterboard Layout 2 (R2)



NOTE: The gray squares indicate the location of pin 1.

Shunt Jumpers

There are three shunt jumpers for connection of a 32.768-KHz clock as shown in Table 3-2.

Table 3-2. Jumper Settings for DB48 Daughterboard

Jumper	Shunt	Description
JP1	No shunt	PB1 is unconnected
	Shunt 1-2	PB1 is connected to 32.768-KHz clock.
	Shunt 2-3	PB1 is connected to daughterboard connector J4-5 (XPB1)
JP2	No shunt	PC7 is unconnected
	Shunt 1-2	PC7 is connected to 32.768-KHz clock.
	Shunt 2-3	PC7 is connected to daughterboard connector J4-5 (XPC7)
JP3	No shunt	PE2 is unconnected
	Shunt 1-2	PE2 is connected to 32.768-KHz clock.
	Shunt 2-3	PE2 is connected to daughterboard connector J4-5 (XPE2)

Development Board Signal Usage

Table 3-3 shows the signal connectivity and usage between the DB48 daughterboard and the motherboard. For the jumpers column, the numbers in brackets show the jumper position.

Table 3-3. Development Board Signals Used by DB48 Daughterboard

Stellaris Signal	DB48 Daughterboard Connection	Motherboard Jumpers	Motherboard Signal	Description
PA0	J4-19	JP7-[1][2]	U0_RX	Serial port 0 receive
PA1	J4-20	JP6-[1][2]	U0_TX	Serial port 0 transmit
PA2	J4-13	JP15-[2][1]	SPI_CLK	Serial peripheral interface clock
PA3	J4-16	JP18-[2][1]	SPI_SEL	Serial peripheral interface select
PA4	J4-15	JP17-[2][1]	SPI_MISO	Serial peripheral interface master-in/slave-out
PA5	J4-14	JP16-[2][1]	SPI_MOSI	Serial peripheral interface master-out/slave-in
PB0	J4-6	JP26-[1][2]	PWM	Buzzer signal
		JP22-[1][2]	ULED0	User LED
PB1	JP1-[2][1]⇨(J3-7)		CLK32K	32.768-KHz clock
	JP1-[2][3]⇨(J4-5)	JP23-[1][2]	ULED1	User LED
PB2	J4-9	JP14-[1][2]	I2C_SCL	I^2C clock signal to EEPROM
		JP24-[1][2]	ULED2	User LED
		JP34-[2][3][a]	IDX	Motor index signal
PB3	J4-10	JP13-[1][2]	I2C_SDA	I^2C data signal to EEPROM
		JP25-[1][2]	ULED3	User LED
		JP35-[2][3][a]	FAULT	Motor fault signal
PB4	J3-20	JP5-[2][1]	C0-	Connects to 10k potentiometer
PB5	J3-19	JP5-[4][3]	C1-	Connects to 10k potentiometer
PB6	J3-18	JP3-[2][1]	C0+	Connects to photocell
PB7	J1-21	J14-3	TRST	JTAG signal, used by emulator
PC0	J1-18	J14-9	TCK	JTAG signal, used by emulator
PC1	J1-19	J14-7	TMS	JTAG signal, used by emulator
PC2	J1-20	J14-5	TDI	JTAG signal, used by emulator
PC3	J1-16	J14-13	TDO	JTAG signal, used by emulator
PC4	J1-3		PC4	Not used
PC5	J3-21	JP3-[4][3]	C1+	Connects to photocell
PC6	J1-4	JP3-[6][5]	C2+	Connects to photocell

Table 3-3. Development Board Signals Used by DB48 Daughterboard

Stellaris Signal	DB48 Daughterboard Connection	Motherboard Jumpers	Motherboard Signal	Description
PC7	JP2-[2][1]⇨(J3-7)	JP5-[6][5]	C2-	32.768-KHz clock
	JP2-[2][3]⇨(J3-16)	JP5-[6][5]	C2-	Connects to 10k potentiometer
PD0	J2-20	JP27-[1][2]	ULED4	User LED
PD1	J2-19	JP28-[1][2]	ULED5	User LED
PD2	J4-17	JP9-[1][2]	U1_RX	Serial port 1 receive
		JP29-[1][2]	ULED6	User LED
PD3	J4-18	JP8-[1][2]	U1_TX	Serial port 1 transmit
		JP30-[1][2]	ULED7	User LED
PD4	J2-12	JP4-[8][7]	ADC7	Connects to 10k potentiometer
PD5	J2-10	JP2-[8][7]	ADC6	Connects to photocell
PD6	J3-17	JP4-[6][5]	ADC5	Connects to 10k potentiometer
		JP35-[1][2][a]	FAULT	Motor fault signal
PD7	J1-2	JP2-[6][5]	ADC4	Connects to photocell
		JP34-[1][2][a]	IDX	Motor index signal
PE0	J2-16		PE0	Not used
PE1	J2-15		PE1	Not used
PE2	JP3-[2][1]⇨(J3-7)		CLK32K	32.768-KHz clock
	JP3-[2][3]⇨(J4-7)	JP4-[4][3]	ADC3	Connects to 10k potentiometer
PE3	J2-11	JP2-[4][3]	ADC2	Connects to photocell
PE4	J2-4	JP4-[2][1]	ADC1	Connects to 10k potentiometer
PE5	J2-3	JP2-[2][1]	ADC0	Connects to photocell
$\overline{\text{RST}}$	J1-12		SYSRST_B	Connects to reset supervisor
OSC0	J7,C4			Connects to pin socket and capacitor for crystal
OSC1	J8,C5			Connects to pin socket and capacitor for crystal
VDD-(U1)	TL5 (Layout 1), TL6 (Layout 2), J2-1, J4-1		3.3V	Connects to 3.3-V plane
GND	J1-1,J2-21 J3-8,J4-21		GND	Connects to ground plane

Table 3-3. Development Board Signals Used by DB48 Daughterboard

Stellaris Signal	DB48 Daughterboard Connection	Motherboard Jumpers	Motherboard Signal	Description
LDO				Connects to 1.3 microfarad capacitor and to test loop 2

a. Jumpers 34 and 35 are only available on Rev3 or later boards.

APPENDIX A

Contact Information

Company Information

Founded in 2004, Luminary Micro, Inc. designs, markets, and sells ARM Cortex-M3-based microcontrollers (MCUs). Austin, Texas-based Luminary Micro is the lead partner for the Cortex-M3 processor, delivering the world's first silicon implementation of the Cortex-M3 processor. Luminary Micro's introduction of the Stellaris® family of products provides 32-bit performance for the same price as current 8- and 16-bit microcontroller designs. With entry-level pricing at $1.00 for an ARM technology-based MCU, Luminary Micro's Stellaris product line allows for standardization that eliminates future architectural upgrades or software tool changes.

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http://www.luminarymicro.com
sales@luminarymicro.com

Support Information

For support on Luminary Micro products, contact:

support@luminarymicro.com
+1-512-279-8800, ext. 3

A P P E N D I X B

Schematics

Schematics for the development board follow:

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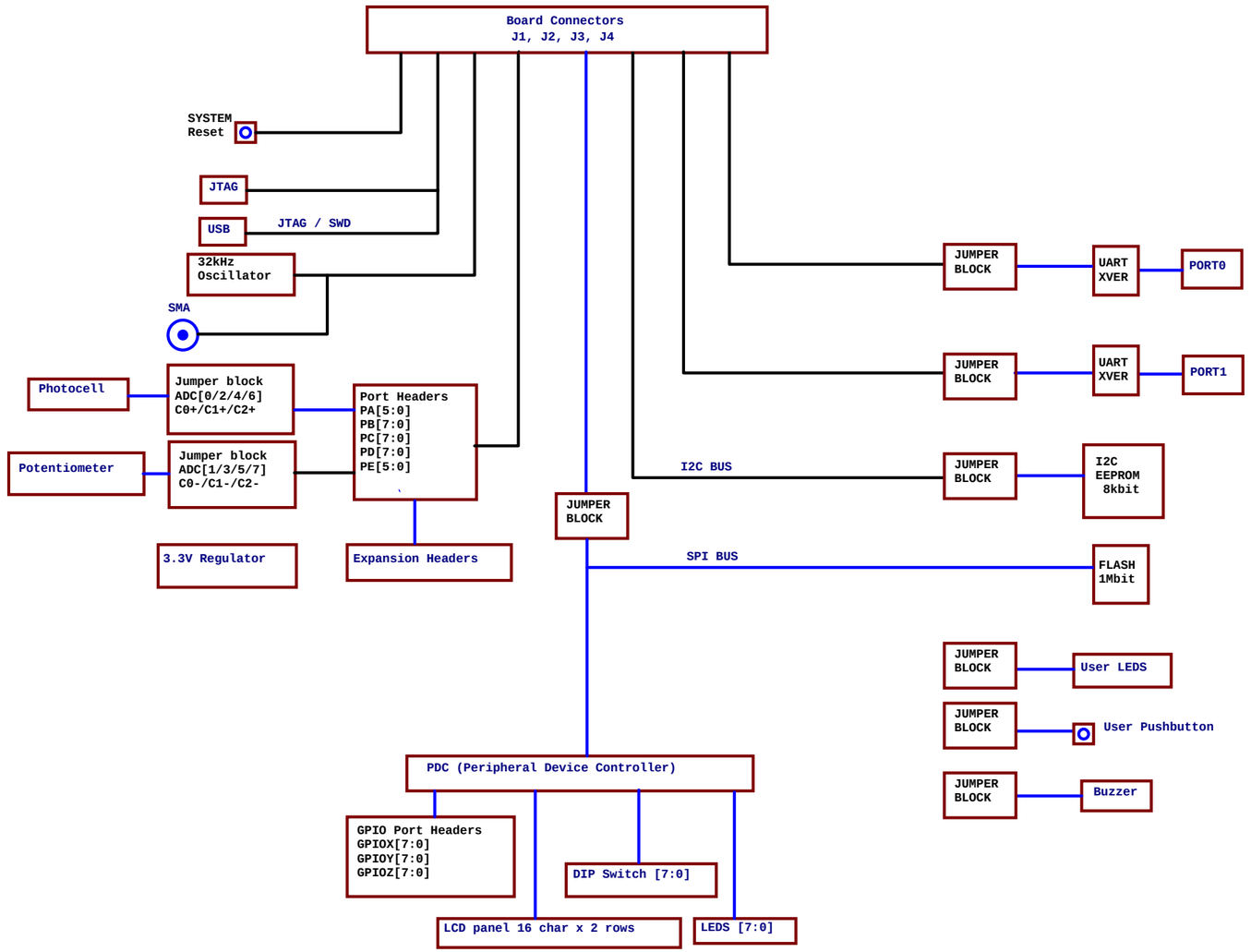
Luminary Micro, Inc.
108 Wild Basin Rd.
Two Wild Basin Suite 350
Austin, TX 78746

Designer: Arnaldo Cruz	Drawing Title: **Stellaris Development Board**
Drawn by: Arnaldo Cruz	Page Title: **Table of Contents**
Approved: *	Size: C; Document Number: 0001; Rev: R3
	Date: 2/5/2007; Sheet 1 of 7



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Drawing Title: Stellaris Development Board

Page Title: Block Diagram

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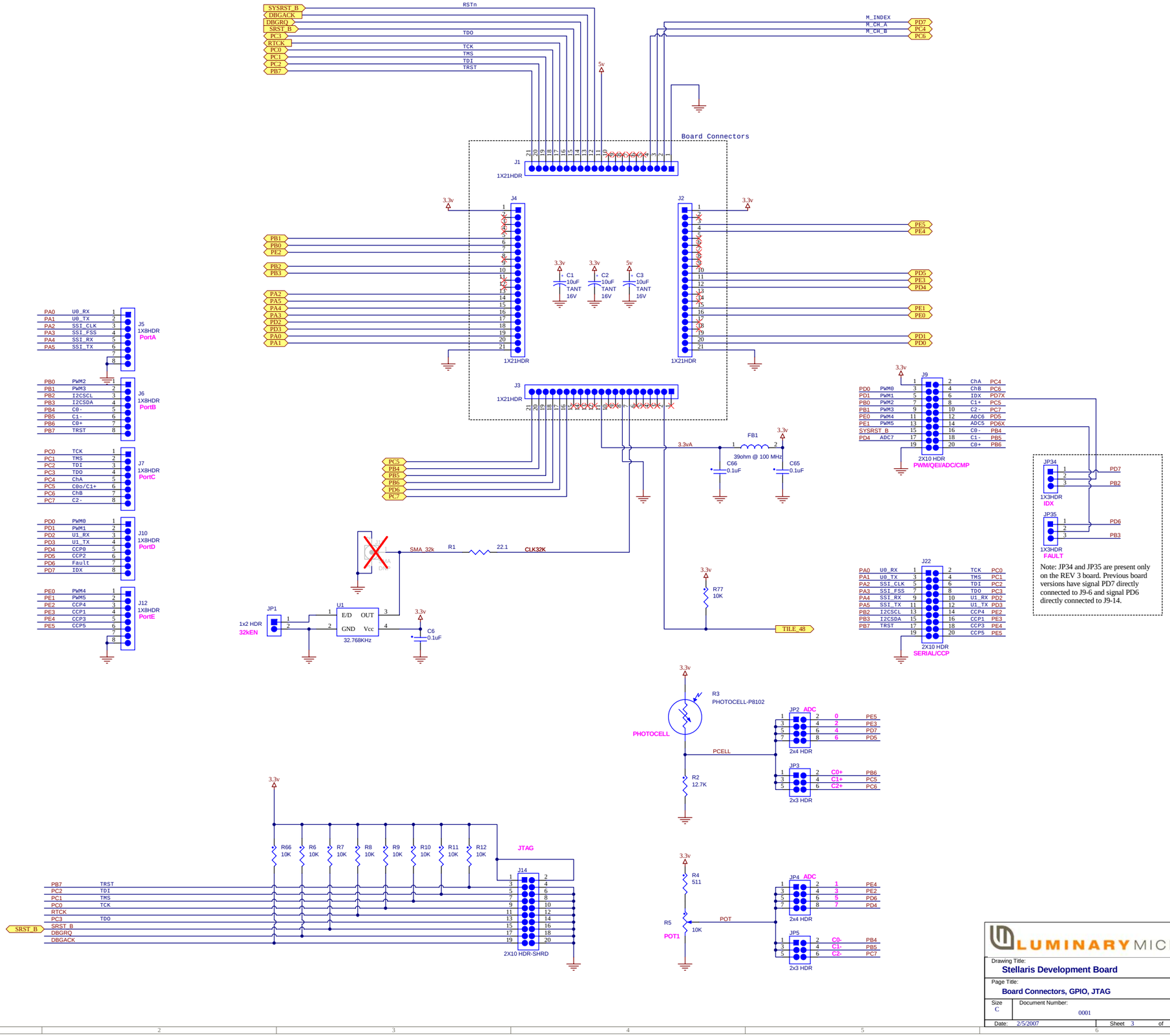
C	0001	R3

Date: 2/5/2007 Sheet 2 of 7


SYSRST_B
DBGACK
DBGRQ
SRST_B
PC3
RTCK
PC0
PC1
PC2
PB7
RSTn
TDO
TCK
TMS
TDI
TRST
5v
M_INDEX
M_CH_A
M_CH_B
PD7
PC4
PC6
Board Connectors
J1
1X21HDR
3.3v
J4
J2
PB1
PB0
PE2
PB2
PB3
PA2
PA5
PA4
PA3
PD2
PD3
PA0
PA1
PE5
PE4
PD5
PE3
PD4
PE1
PE0
PD1
PD0
C1
C2
C3
10uF
TANT
16V
J3
PC5
PB4
PB5
PB6
PD6
PC7
3.3vA
FB1
39ohm @ 100 MHz
C66
C65
0.1uF
J9
PD0 PWM0
PD1 PWM1
PB0 PWM2
PB1 PWM3
PE0 PWM4
PE1 PWM5
SYSRST_B
PD4 ADC7
ChA PC4
ChB PC6
IDX PD7X
C1+ PC5
C2- PC7
ADC6 PD5
ADC5 PD6X
C0- PB4
C1- PB5
C0+ PB6
2X10 HDR
PWM/QEI/ADC/CMP
JP34
JP35
1X3HDR
IDX
FAULT
PD7
PB2
PD6
PB3
Note: JP34 and JP35 are present only on the REV 3 board. Previous board versions have signal PD7 directly connected to J9-6 and signal PD6 directly connected to J9-14.
SMA_32k
R1
22.1
CLK32K
JP1
1x2 HDR
32kEN
U1
E/D
OUT
GND
Vcc
32.768KHz
C6
0.1uF
R77
10K
TILE_48
J22
PA0 U0_RX
PA1 U0_TX
PA2 SSI_CLK
PA3 SSI_FSS
PA4 SSI_RX
PA5 SSI_TX
PB2 I2CSCL
PB3 I2CSDA
PB7 TRST
TCK PC0
TMS PC1
TDI PC2
TDO PC3
U1_RX PD2
U1_TX PD3
CCP4 PE2
CCP1 PE3
CCP3 PE4
CCP5 PE5
2X10 HDR
SERIAL/CCP
J5
1X8HDR
PortA
PA0 U0_RX
PA1 U0_TX
PA2 SSI_CLK
PA3 SSI_FSS
PA4 SSI_RX
PA5 SSI_TX
J6
1X8HDR
PortB
PB0 PWM2
PB1 PWM3
PB2 I2CSCL
PB3 I2CSDA
PB4 C0-
PB5 C1-
PB6 C0+
PB7 TRST
J7
1X8HDR
PortC
PC0 TCK
PC1 TMS
PC2 TDI
PC3 TDO
PC4 ChA
PC5 C0o/C1+
PC6 ChB
PC7 C2-
J10
1X8HDR
PortD
PD0 PWM0
PD1 PWM1
PD2 U1_RX
PD3 U1_TX
PD4 CCP0
PD5 CCP2
PD6 Fault
PD7 IDX
J12
1X8HDR
PortE
PE0 PWM4
PE1 PWM5
PE2 CCP4
PE3 CCP1
PE4 CCP3
PE5 CCP5
R3
PHOTOCELL-P8102
PHOTOCELL
PCELL
R2
12.7K
JP2 ADC
JP3
2x4 HDR
2x3 HDR
0
2
4
6
C0+ PB6
C1+ PC5
C2+ PC6
R4
511
R5
10K
POT
POT1
JP4 ADC
JP5
1
3
5
7
C0- PB4
C1- PB5
C2- PC7
R66
R6
R7
R8
R9
R10
R11
R12
10K
JTAG
J14
2X10 HDR-SHRD
PB7 TRST
PC2 TDI
PC1 TMS
PC0 TCK
RTCK
PC3 TDO
SRST_B
DBGRQ
DBGACK
LUMINARY MICRO
Drawing Title:
Stellaris Development Board
Page Title:
Board Connectors, GPIO, JTAG
Size
C
Document Number:
0001
Rev
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Date:
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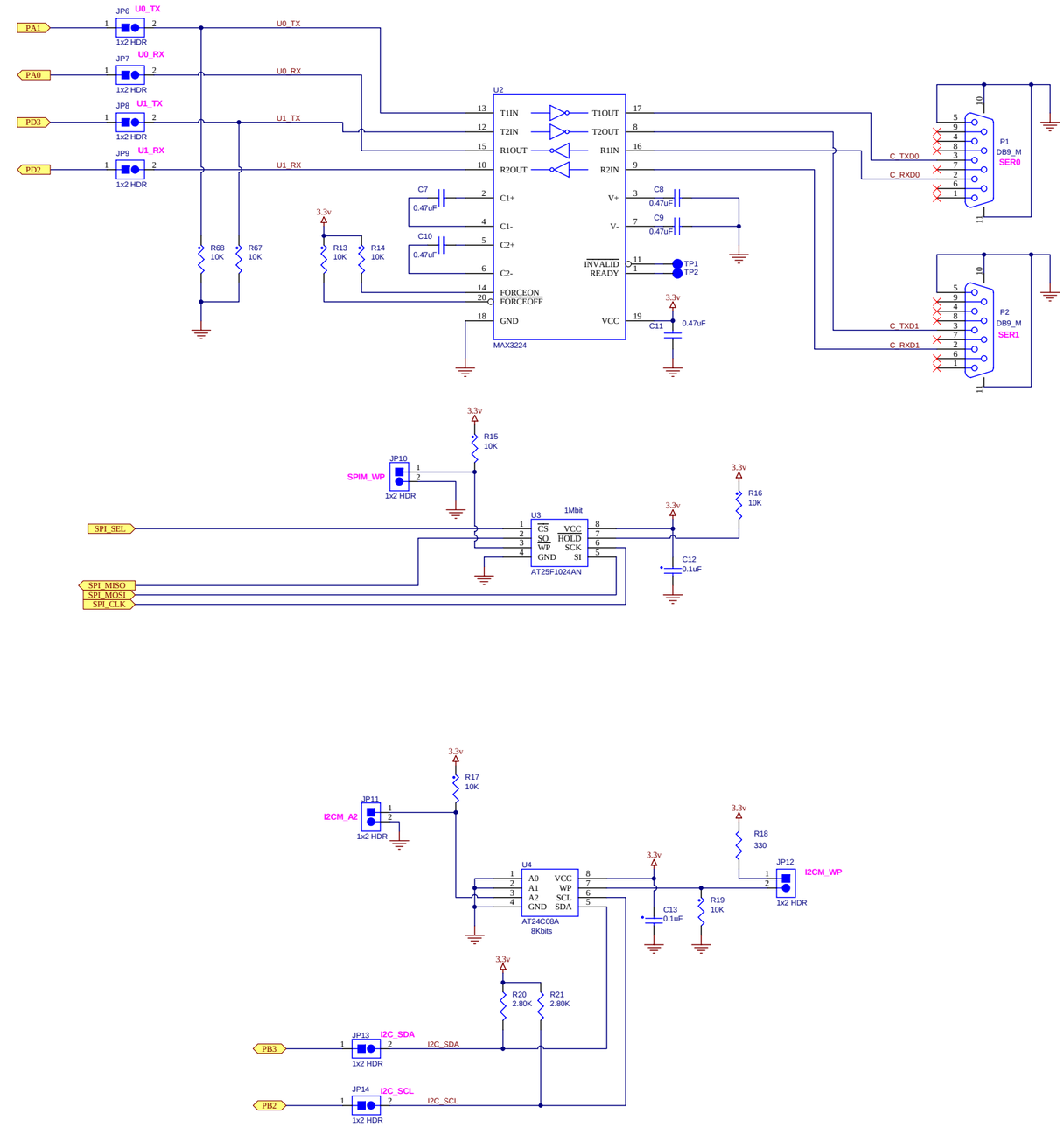
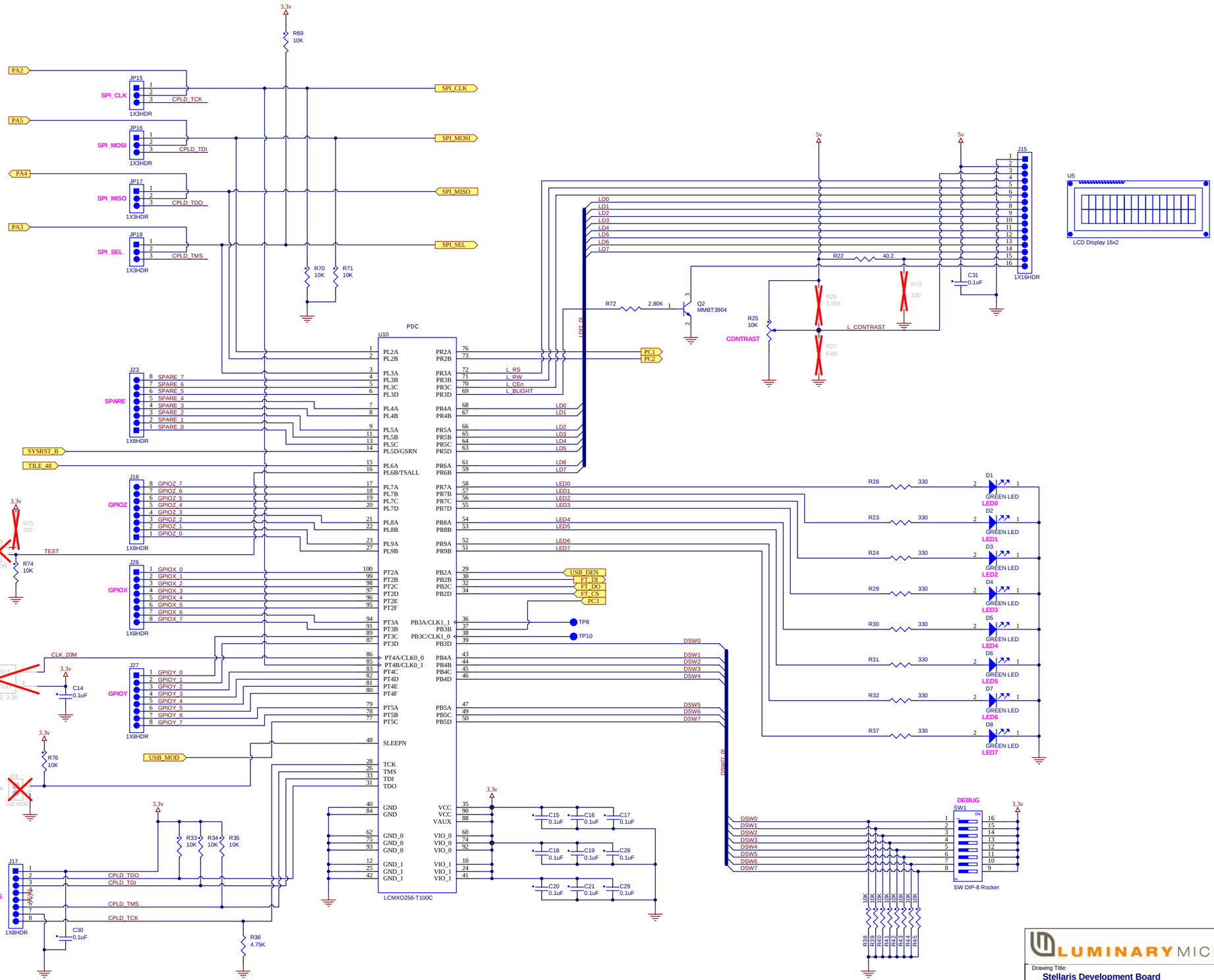


LUMINARY MICRO			
Drawing Title: Stellaris Development Board			
Page Title: UART/SPI/I2C			
Size: C	Document Number: 0001		Rev: R3
Date: 2/5/2007	Sheet 4 of 7		



LUMINARY MICRO

Drawing Title: **Stellaris Development Board**

Page Title: **PDC, LCD Display, LEDs, DIP Switch**

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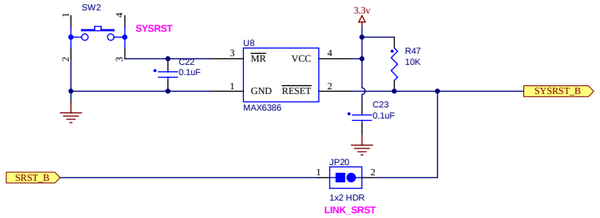
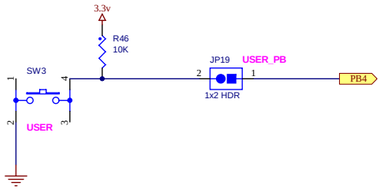
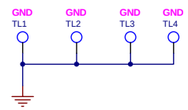
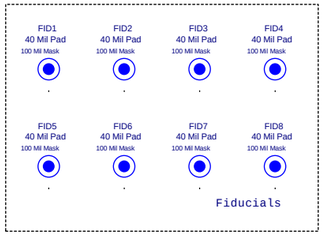
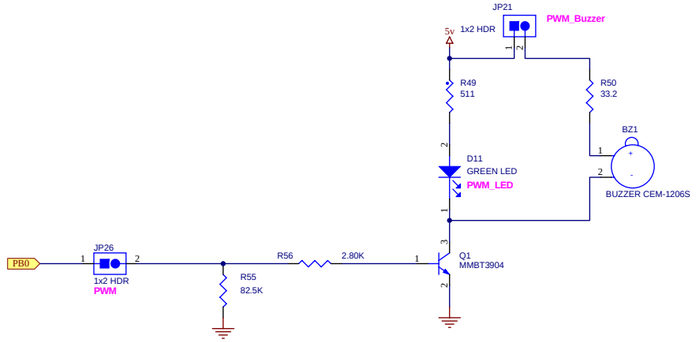
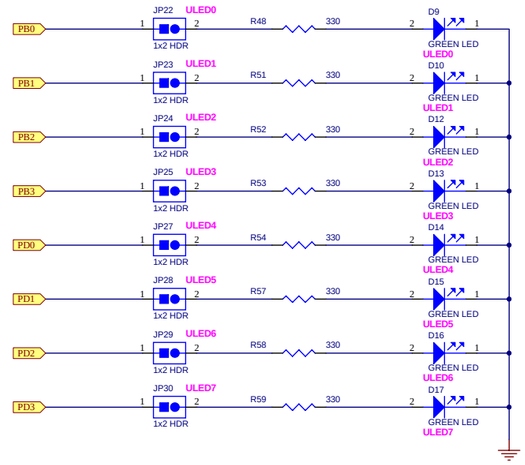




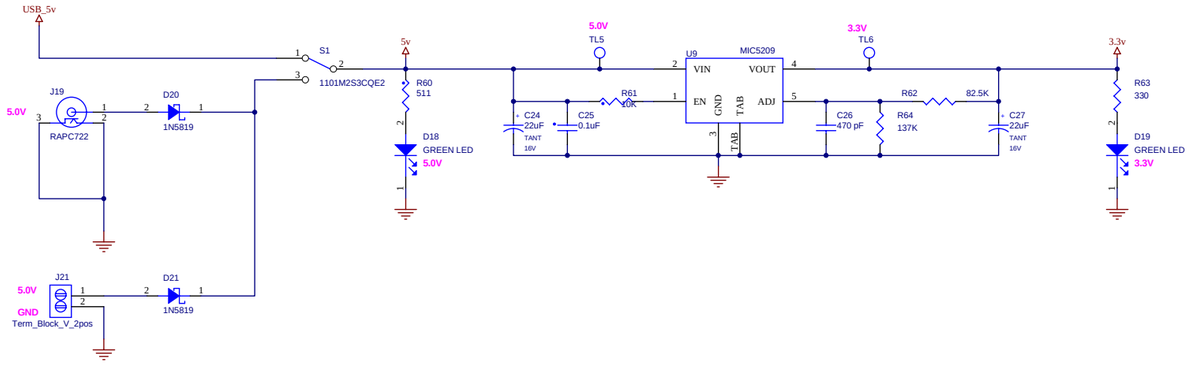




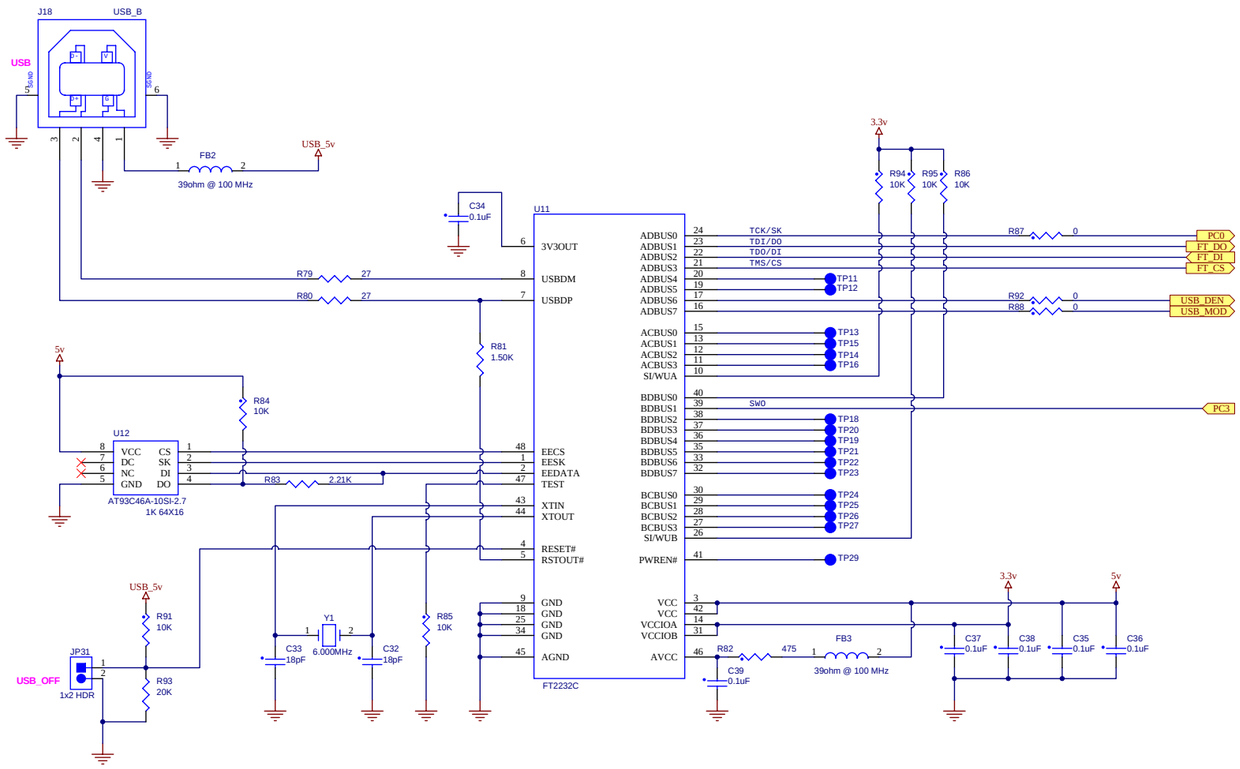




Notes:
1. Power provided by external 5v DC supply or USB port, as selected by switch
2. Use of USB power requires a high power port (500mA).



LUMINARY MICRO		
Drawing Title: Stellaris Development Board		
Page Title: Power, Reset		
Size: C	Document Number: 0001	Rev: R3
Date: 2/5/2007	Sheet 6 of 7	



LUMINARY MICRO

Drawing Title:
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USB to JTAG / SWD

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2499 S. Capital of Texas Hwy
Austin, TX 78746

Designer: Arnaldo Cruz	Drawing Title: **Stellaris DB28 Daughterboard**
Drawn by: Arnaldo Cruz	Page Title: **Table of Contents**
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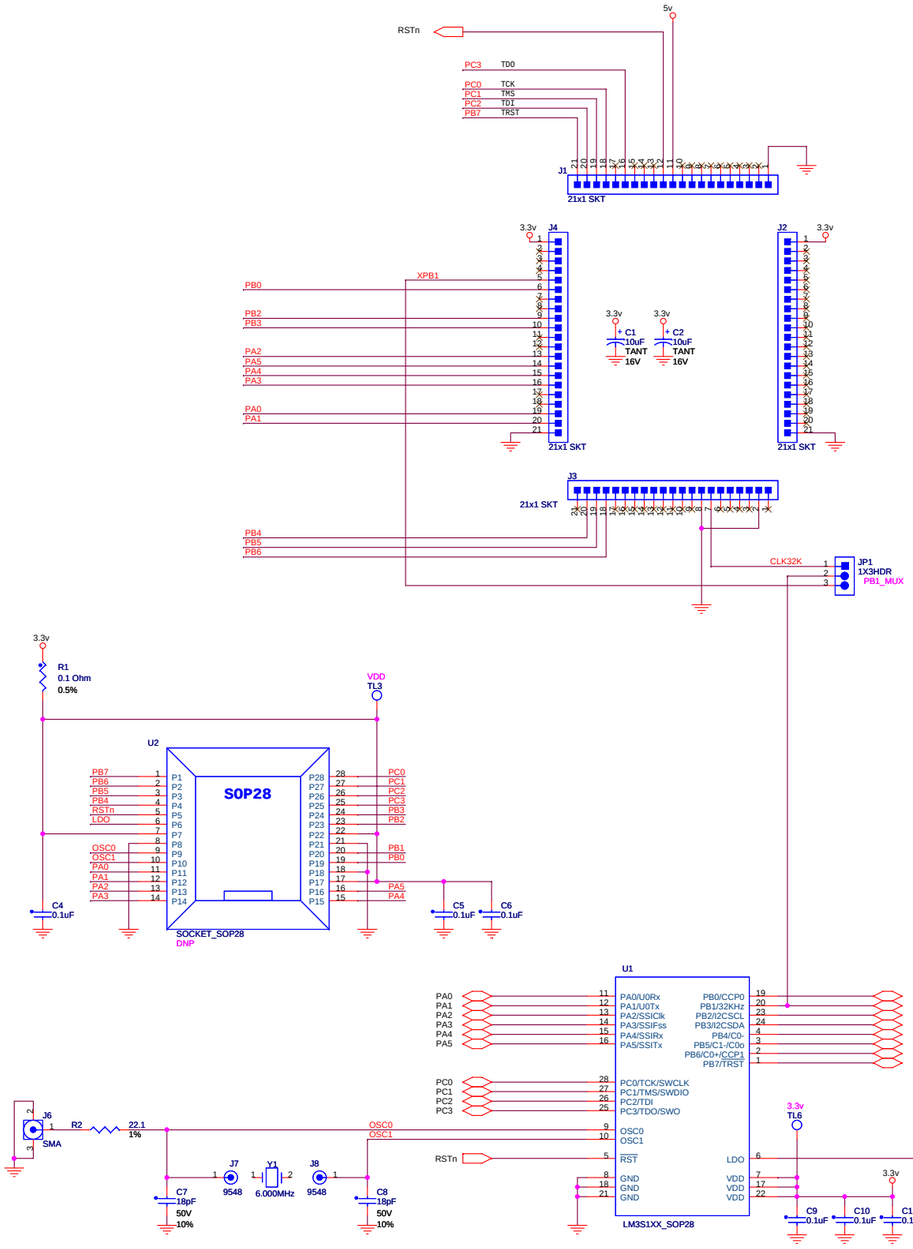
5v
RSTn
PC3 TD0
PC0 TCK
PC1 TMS
PC2 TDI
PB7 TRST
J1
21x1 SKT
3.3v
J4
XPB1
PB0
PB2
PB3
PA2
PA5
PA4
PA3
PA0
PA1
21x1 SKT
C1
10uF
TANT
16V
C2
10uF
TANT
16V
J2
21x1 SKT
J3
21x1 SKT
PB4
PB5
PB6
CLK32K
JP1
1X3HDR
PB1_MUX
3.3v
R1
0.1 Ohm
0.5%
VDD
TL3
U2
SOP28
PB7
PB6
PB5
PB4
RSTn
LDO
OSC0
OSC1
PA0
PA1
PA2
PA3
PC0
PC1
PC2
PC3
PB1
PB0
PA5
PA4
C4
0.1uF
C5
0.1uF
C6
0.1uF
SOCKET_SOP28
DNP
U1
PA0/U0Rx
PA1/U0Tx
PA2/SSIClk
PA3/SSIFss
PA4/SSIRx
PA5/SSITx
PB0/CCP0
PB1/32KHz
PB2/I2CSCL
PB3/I2CSDA
PB4/C0-
PB5/C1-/C0o
PB6/C0+/CCP1
PB7/TRST
PC0/TCK/SWCLK
PC1/TMS/SWDIO
PC2/TDI
PC3/TDO/SWO
OSC0
OSC1
RST
LDO
VDD
VDD
VDD
GND
GND
GND
LM3S1XX_SOP28
J6
SMA
R2
22.1
1%
J7
9548
Y1
6.000MHz
J8
9548
C7
18pF
50V
10%
C8
18pF
50V
10%
3.3v
TL6
LDO
TL2
C9
0.1uF
C10
0.1uF
C11
0.1uF
C12
1uF
C13
0.33uF
16V
10%
GND TL1
GND TL4
GND TL5
GND TL7
FID1
40 Mil Pad
100 Mil Mask
FID2
40 Mil Pad
100 Mil Mask
FID3
40 Mil Pad
100 Mil Mask
FID4
40 Mil Pad
100 Mil Mask
Fiducials
LUMINARY MICRO
Drawing Title:
Stellaris DB28 Daughterboard
Page Title:
LM3S1XX, Socket, Connectors
Size C
Document Number 0001
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2499 S. Capital of Texas Hwy
Austin, TX 78746

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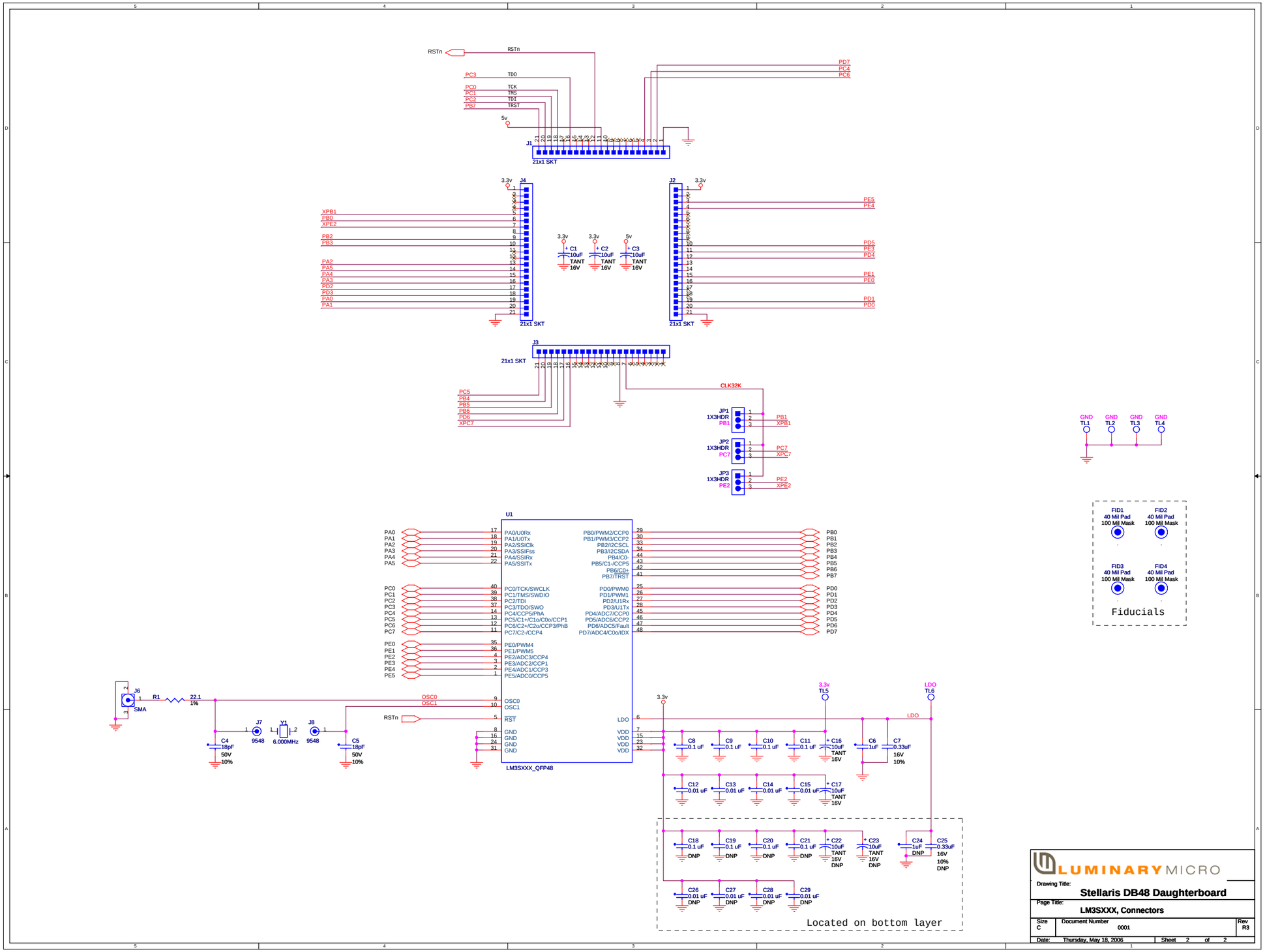
RSTn
PC3
PC0
PC1
PC2
PB7
TD0
TCK
TMS
TDI
TRST
5v
PD7
PC4
PC6
J1
21x1 SKT
3.3v
J4
XPB1
PB0
XPE2
PB2
PB3
PA2
PA5
PA4
PA3
PD2
PD3
PA0
PA1
21x1 SKT
C1
10uF
TANT
16V
C2
10uF
TANT
16V
5v
C3
10uF
TANT
16V
J2
PE5
PE4
PD5
PD3
PD4
PE1
PE0
PD1
PD0
21x1 SKT
J3
21x1 SKT
PC5
PB4
PB5
PB6
PD6
XPC7
CLK32K
JP1
1X3HDR
PB1
PB1
XPB1
JP2
1X3HDR
PC7
PC7
XPC7
JP3
1X3HDR
PE2
PE2
XPE2
GND
TL1
GND
TL2
GND
TL3
GND
TL4
U1
PA0
PA1
PA2
PA3
PA4
PA5
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PE0
PE1
PE2
PE3
PE4
PE5
PA0/U0Rx
PA1/U0Tx
PA2/SSI0Clk
PA3/SSI0Fss
PA4/SSI0Rx
PA5/SSI0Tx
PC0/TCK/SWCLK
PC1/TMS/SWDIO
PC2/TDI
PC3/TDO/SWO
PC4/CCP5/PhA
PC5/C1+/C1o/C0o/CCP1
PC6/C2+/C2o/CCP3/PhB
PC7/C2-/CCP4
PE0/PWM4
PE1/PWM5
PE2/ADC3/CCP4
PE3/ADC2/CCP1
PE4/ADC1/CCP3
PE5/ADC0/CCP5
PB0/PWM2/CCP0
PB1/PWM3/CCP2
PB2/I2CSCL
PB3/I2CSDA
PB4/C0-
PB5/C1-/CCP5
PB6/C0+
PB7/TRST
PD0/PWM0
PD1/PWM1
PD2/U1Rx
PD3/U1Tx
PD4/ADC7/CCP0
PD5/ADC6/CCP2
PD6/ADC5/Fault
PD7/ADC4/C0o/IDX
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
LM3SXXX_QFP48
J6
SMA
R1
22.1
1%
OSC0
OSC1
RSTn
OSC0
OSC1
RST
GND
GND
GND
GND
LDO
VDD
VDD
VDD
VDD
J7
9548
Y1
6.000MHz
J8
9548
C4
18pF
50V
10%
C5
18pF
50V
10%
3.3v
3.3v
LDO
TL5
LDO
TL6
C8
0.1 uF
C9
0.1 uF
C10
0.1 uF
C11
0.1 uF
C16
10uF
TANT
16V
C6
1uF
C7
0.33uF
16V
10%
C12
0.01 uF
C13
0.01 uF
C14
0.01 uF
C15
0.01 uF
C17
10uF
TANT
16V
C18
0.1 uF
DNP
C19
0.1 uF
DNP
C20
0.1 uF
DNP
C21
0.1 uF
DNP
C22
10uF
TANT
16V
DNP
C23
10uF
TANT
16V
DNP
C24
1uF
DNP
C25
0.33uF
16V
10%
DNP
C26
0.01 uF
DNP
C27
0.01 uF
DNP
C28
0.01 uF
DNP
C29
0.01 uF
DNP
Located on bottom layer
FID1
40 Mil Pad
100 Mil Mask
FID2
40 Mil Pad
100 Mil Mask
FID3
40 Mil Pad
100 Mil Mask
FID4
40 Mil Pad
100 Mil Mask
Fiducials
LUMINARY MICRO
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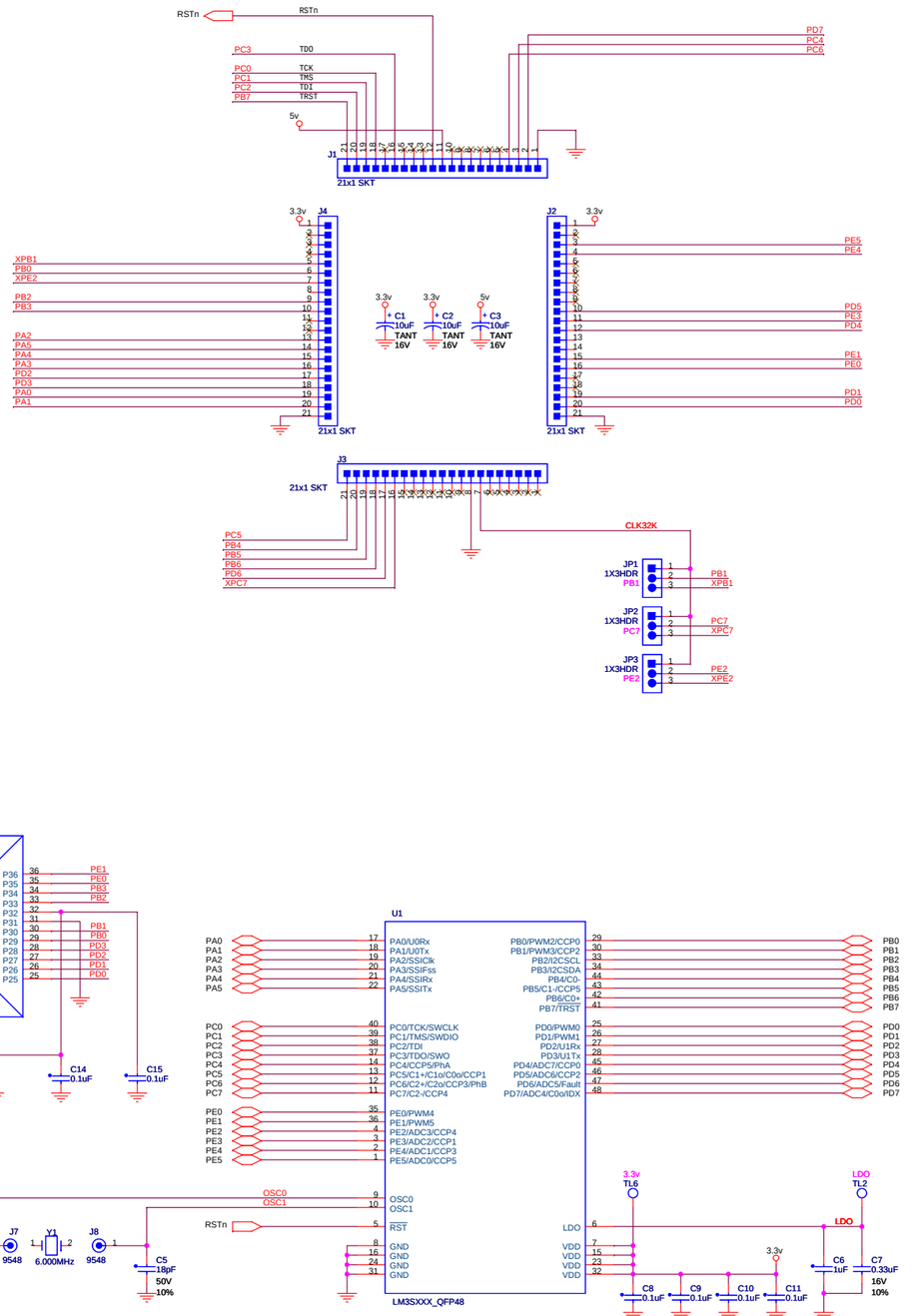

LUMINARY MICRO		
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