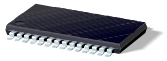


Typical Size
6,4 mm X 9,7 mm

DUAL INPUT BUS (2.5 V, 3.3 V) 9-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **Low Voltage Separate Power Bus**
- **15-mΩ MOSFET Switches for High Efficiency at 9-A Continuous Output**
- **Adjustable Output Voltage**
- **Externally Compensated With 1% Internal Reference Accuracy**
- **Fast Transient Response**
- **Wide PWM Frequency: Adjustable 280 kHz to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

APPLICATIONS

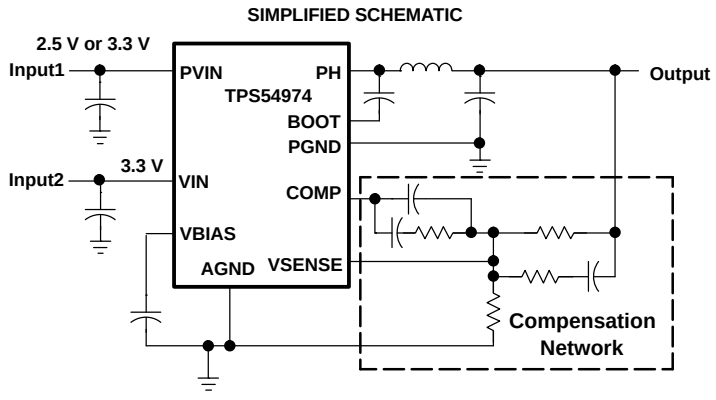
- **Low-Voltage, High-Density Systems With Power Distributed at 2.5 V, 3.3 V Available**
- **Point-of-Load Regulation for High-Performance DSPs, FPGAs, ASICs, and Microprocessors**
- **Broadband, Networking, and Optical Communications Infrastructure**
- **Portable Computing/Notebook PCs**

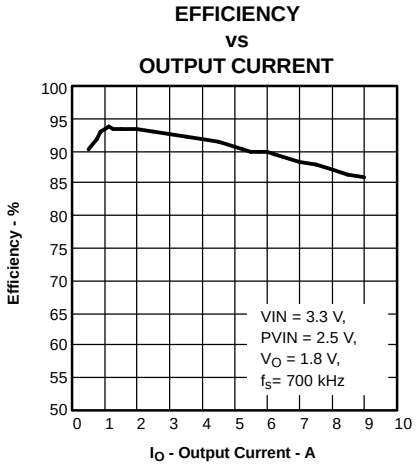
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54974 low-input voltage, high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high-performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an undervoltage-lockout circuit to prevent start-up until the VIN input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power-good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54974 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks.

SIMPLIFIED SCHEMATIC





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 85°C	Adjustable down to 0.9 V	Plastic HTSSOP (PWP)(1)	TPS54974PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54974PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS54974
V_I	Input voltage range	SS/ENA	–0.3 V to 7 V
		RT	–0.3 V to 6 V
		VSENSE	–0.3 V to 4 V
		PVIN, VIN	–0.3 V to 4.5 V
		BOOT	–0.3 V to 10 V
V_O	Output voltage range	VBIAS, COMP, PWRGD	–0.3 V to 7 V
		PH	–0.6 V to 6 V
I_O	Source current	PH	Internally limited
		COMP, VBIAS	6 mA
I_S	Sink current	PH	16 A
		COMP	6 mA
		SS/ENA, PWRGD	10 mA
	Voltage differential	AGND to PGND	±0.3 V
T_J	Operating virtual junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage, VIN	3		4	V
PVIN	Power input voltage	2.2	2.5	4.0	V
T_J	Operating junction temperature	–40		125	°C

DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28-Pin PWP with solder	14.4°C/W	6.94 W(3)	3.81 W	2.77 W
28-Pin PWP without solder	27.9°C/W	3.58 W	1.97 W	1.43 W

(1) For more information on the PWP package, see TI technical brief, literature number SLMA002.
(2) Test board conditions:
  a. 3-inch x 3-inch, 4 layers, thickness: 0.062-inch
  b. 1.5-oz. copper traces located on the top of the PCB
  c. 1.5-oz. copper ground plane on the bottom of the PCB
  d. 0.5-oz. copper ground planes on the 2 internal layers
  e. 12 thermal vias (see "Recommended Land Pattern" in applications section of this data sheet)
(3) Maximum power dissipation may be limited by overcurrent protection.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 2.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
Input voltage range, VIN			3.0		4.0	V
Supply voltage range, PVIN		Output = 1.8 V	2.2	2.5	4.0	V
$I_{(Q)}$ Quiescent current	VIN	f_s = 350 kHz, RT open, PH pin open, PVIN = 2.5 V		6.3	10.0	mA
		SHUTDOWN, SS/ENA = 0 V, PVIN = 2.5 V		1	1.4	
	PVIN	f_s = 350 kHz, RT open, PH pin open, VIN = 3.3 V		4.0	7.0	mA
		SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V		<100		µA
UNDER VOLTAGE LOCKOUT (VIN)						
Start threshold voltage, UVLO				2.95	3.0	V
Stop threshold voltage, UVLO			2.70	2.80		V
Hysteresis voltage, UVLO			0.14	0.16		V
Rising and falling edge deglitch, UVLO(1)				2.5		µs
BIAS VOLTAGE						
Output voltage, VBIAS		$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
Output current, VBIAS(2)					100	µA
CUMULATIVE REFERENCE						
V_{ref} Accuracy			0.882	0.891	0.900	V
REGULATION						
Line regulation(1)(3)		I_L = 4.5 A, f_s = 350 kHz, T_J = 85°C			0.07	%/V
Load regulation(1)(3)		I_L = 0 A to 9 A, f_s = 350 kHz, T_J = 85°C			0.03	%/A
OSCILLATOR						
Internally set—free-running frequency		RT open(1)	280	350	420	kHz
Externally set—free-running frequency range		RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)	460	500	540	
		RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
Ramp valley(1)				0.75		V
Ramp amplitude (peak-to-peak)(1)				1		V
Minimum controllable on time(1)					200	ns
Maximum duty cycle(1)			90%			

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10.

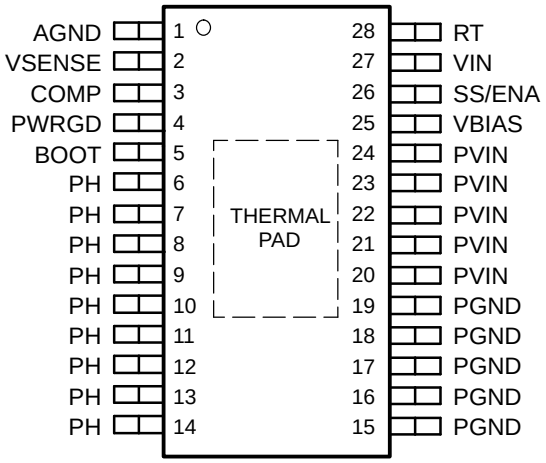
ELECTRICAL CHARACTERISTICS (CONTINUED)

T_J = –40°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 2.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open-loop voltage gain	1 kΩ COMP to AGND(1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(1)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(1)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP		1.0	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead-time)	10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
	Enable hysteresis voltage, SS/ENA(1)			0.03		V
	Falling edge deglitch, SS/ENA(1)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 0.2 V, VIN = 2.7 V, PVIN = 2.5 V	1.5	2.3	4.0	mA
POWER GOOD						
	Power-good threshold voltage	VSENSE falling		90		%V_{ref}
	Power-good hysteresis voltage(1)			3		%V_{ref}
	Power-good falling edge deglitch(1)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	VIN = 3.3 V, PVIN = 2.5 V			1	µA
CURRENT LIMIT						
	Current limit	VIN = 3.3 V, PVIN = 2.5 V(1), Output shorted	11	15		A
	Current limit leading edge blanking time(1)			100		ns
	Current limit total response time(1)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip-point(1)		135	150	165	°C
	Thermal shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	VIN = 3 V, PVIN = 2.5 V		15	30	mΩ
		VIN = 3.6 V, PVIN = 2.5 V		14	28	

(1) Specified by design

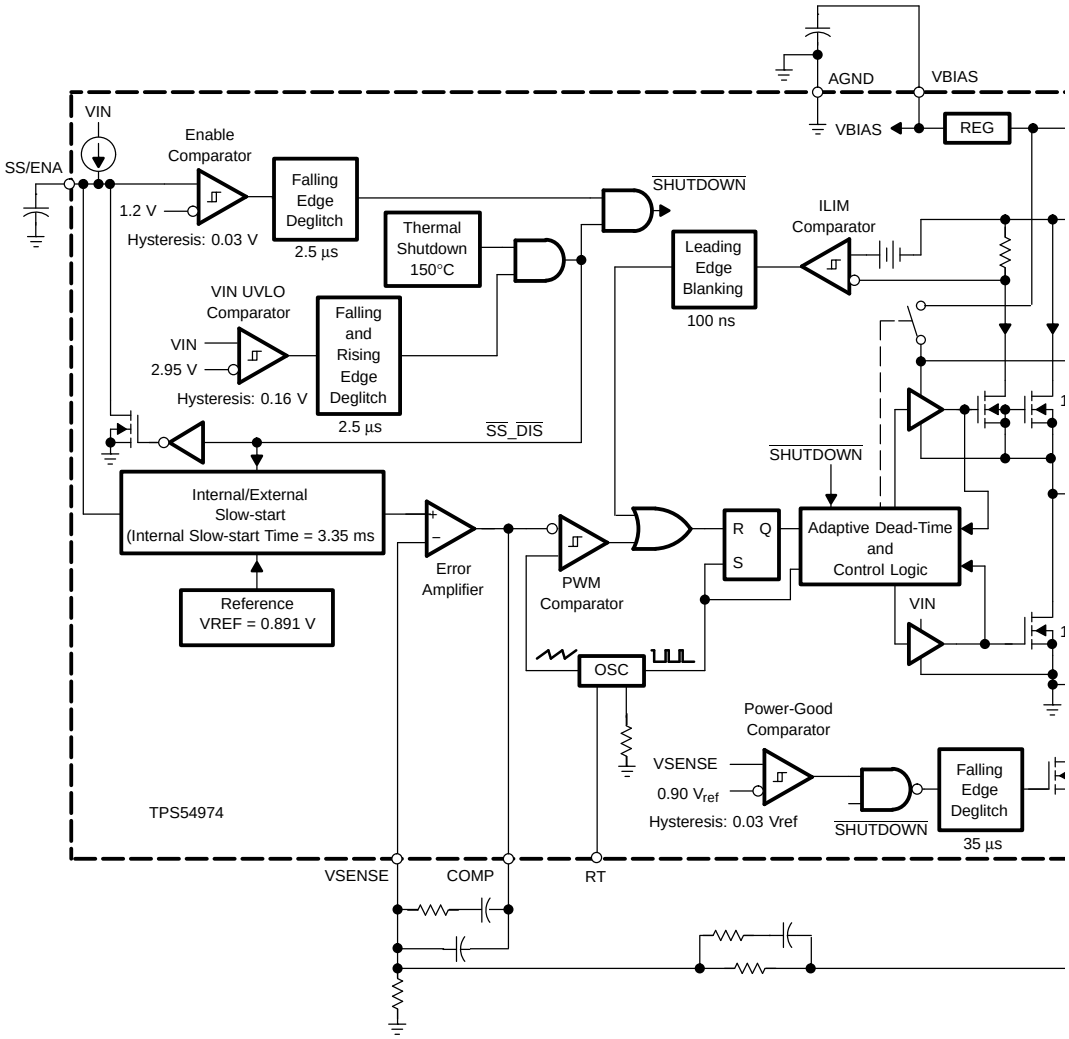
PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15-19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single-point connection to AGND is recommended.
PH	6-14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PVIN	20-24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
PWRGD	4	Power-good, open-drain output. High when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	27	Input supply for the internal bias regulator. An external capacitor of 1 µF to be connected to the VIN pin.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

INTERNAL BLOCK DIAGRAM



RELATED DC/DC PRODUCTS

- TPS40000—dc/dc controller
- TPS56300—dc/dc controller
- PT6600 series—9-A plug-in modules
- TPS54910—dc/dc converter

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

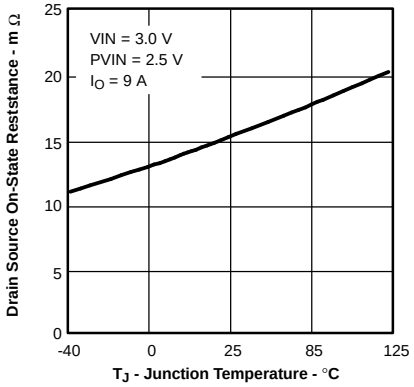


Figure 1.

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

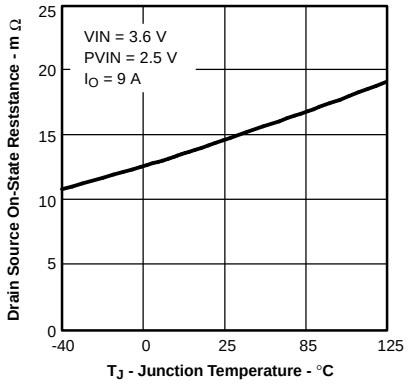


Figure 2.

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

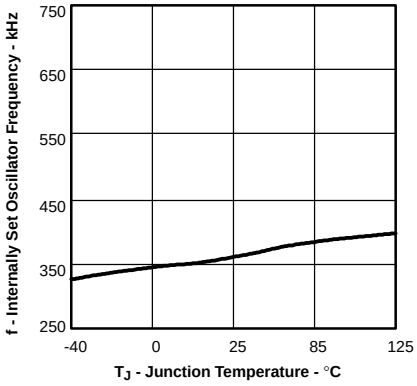


Figure 3.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

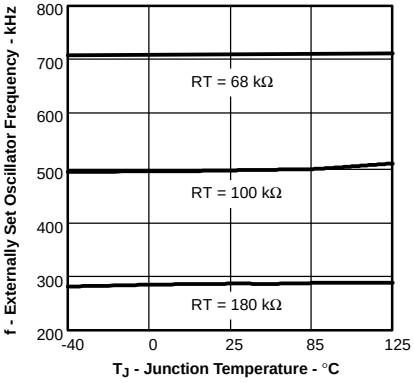


Figure 4.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

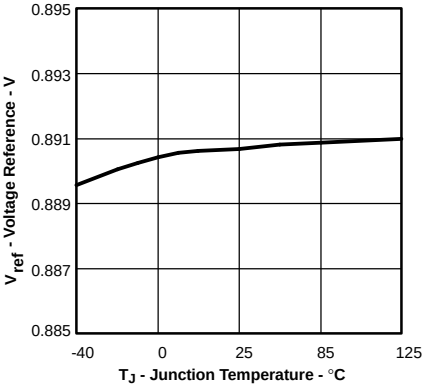


Figure 5.

DEVICE POWER LOSSES vs LOAD CURRENT

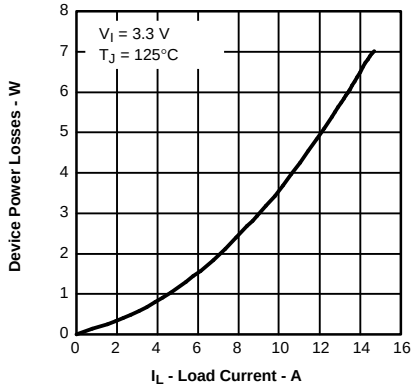


Figure 6.

REFERENCE VOLTAGE vs INPUT VOLTAGE

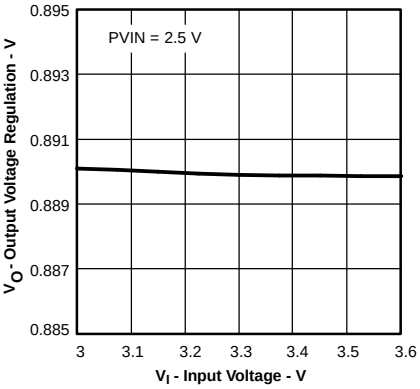


Figure 7.

ERROR AMPLIFIER OPEN-LOOP RESPONSE

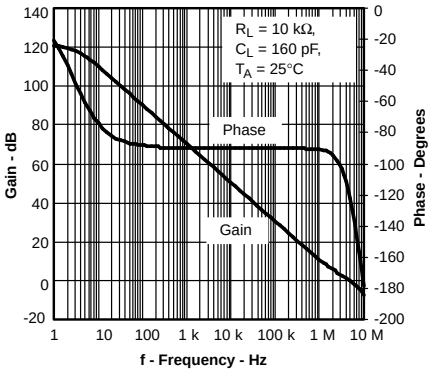


Figure 8.

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

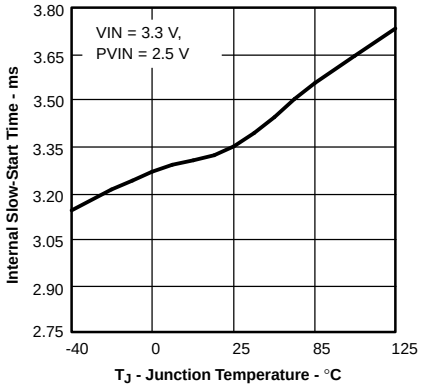
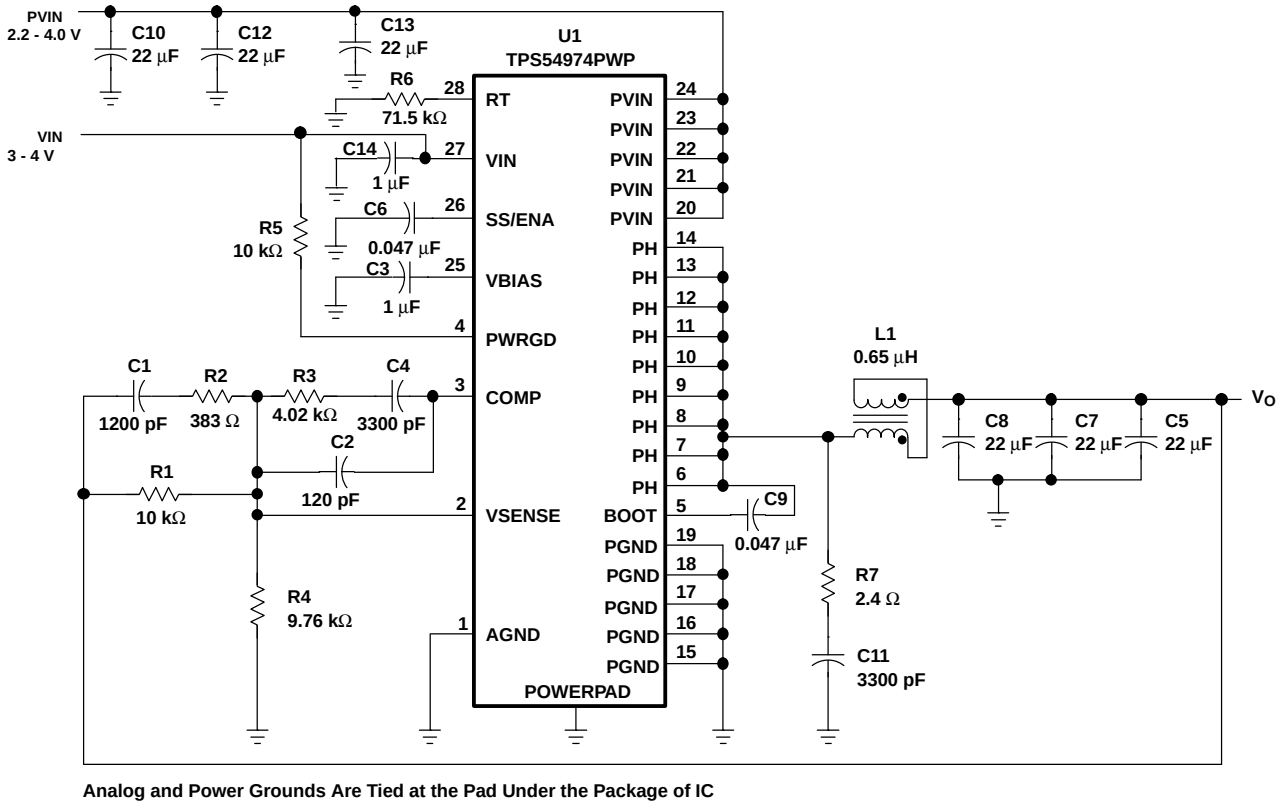


Figure 9.

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54974 application. The TPS54974 (U1) can provide up to 9 A of output current at a nominal outputvoltage of 1.8 V. For proper thermal performance, the exposed thermal PowerPAD underneath the integrated circuit, TPS54974, package must be soldered to the printed-circuit board.



Analog and Power Grounds Are Tied at the Pad Under the Package of IC

Figure 10. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example were selected for best load transient response and small PCB area. Additional design information is available at *www.ti.com*.

INPUT FILTER

The PVIN input voltage is nominally at 2.5 VDC. The input filter consists of three 22-µF ceramic capacitors (C10, C12, and C13) which must be located as close as possible to the PVIN and PGND pins or the device to provide high-frequency decoupling. Ripple current is carried in all three capacitors. The return path to PGND must be made so as to avoid introducing circulating currents in the output filter stage.

FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times.

The resistor divider network of R1 and R4 sets the output voltage for the circuit at 1.8 V. R1 along with R2, R3, C1, C2, and C4 forms the loop compensation network for the circuit. For this design, a Type-3 topology is used.

OPERATING FREQUENCY

In the application circuit, RT is grounded through a 71.5-kΩ resistor to select the operating frequency of 700 kHz. To set a different frequency, place a 68-kΩ to 180-kΩ resistor between RT (pin 28) and analog ground or leave RT floating to select the default of 350 kHz. The resistance can be approximated using the following equation:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ [\text{k}\Omega] \quad (1)$$

OPERATING WITH SEPARATE PVIN

The TPS54974 is designed to operate with the power stage (high-side and low-side MOSFETs) with the

PVIN input connected to a separate power source from VIN. The primary intended application has VIN connected to a 3.3-V bus and PVIN connected to a 2.5-V bus. The TPS54974 cannot be damaged by any sequencing of these voltages. However, the UVLO (see detailed description section) is referenced to the VIN input. Some conditions may cause undesirable operation.

If PVIN is absent when the VIN input is high, the slow-start is released, and the PWM circuit goes to maximum duty factor. When the PVN input ramps up, the output of the TPS54974 follows the PVIN input until enough voltage is present to regulate to the proper output value.

NOTE:

If the PVIN input is controlled via a fast bus switch, it results in a hard-start condition and may damage the load (i.e., whatever is connected to the regulated output of the TPS54974). If a power-good signal is not available from the 2.5-V power supply, one can be generated using a comparator and hold the SS/ENA pin low until the 2.5-V bus power is good. An example of this is shown in Figure 11. This circuit can also be used to prevent the TPS54974 output from following the PVIN input while the PVIN power supply is ramping up.

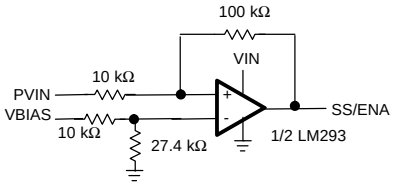


Figure 11. Undervoltage Lockout Circuit for PVIN Using Open-Collector or Open-Drain Comparator

PVIN and VIN can be tied together for 3.3-V bus operation.

OUTPUT FILTER

The output filter is composed of a 0.65-µH inductor and 3 x 22-µF capacitor. The inductor is a low dc-resistance (0.017 Ω) type, Pulse Engineering PA0277. The capacitors used are 22-µF, 6.3-V ceramic types with X5R dielectric. The feedback loop is compensated so that the unity gain frequency is approximately 75 kHz.

MAXIMUM OUTPUT VOLTAGE

The maximum attainable output voltage is limited by the minimum voltage at the PVIN pin. Nominal maximum duty cycle is limited to 90% in the TPS54974, so maximum output voltage is:

$$V_{O(max)} = PVIN_{(min)} \times 0.9 \quad (2)$$

Care must be taken while operating when nominal conditions cause duty cycles near 90%. Load transients can require momentary increases in duty cycle. If the required duty cycle exceeds 90%, the output may fall out of regulation.

PCB LAYOUT

Figure 12 shows a generalized PCB layout guide for the TPS54974.

The PVIN pins should be connected together on the printed-circuit board (PCB) and bypassed with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54974 ground pins. The minimum recommended bypass capacitance is 10 µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins. If the VIN is connected to a separate source supply, it should be bypassed with its own capacitor.

The TPS54974 has two internal grounds (analog and power). Inside the TPS54974, the analog ground ties to all of the noise-sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54974, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that should tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54974. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the voltage set-point divider, timing resistor RT, slow-start capacitor, and bias-capacitor grounds. Connect this trace directly to AGND (pin 1).

The PH pins should be tied together and routed to the output inductor. Because the PH connection is the switching node, the inductor should be located close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout, and PGND as small as practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they have to be routed somewhat close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If an RT resistor or slow-start capacitor is used, connect them to this trace as well.

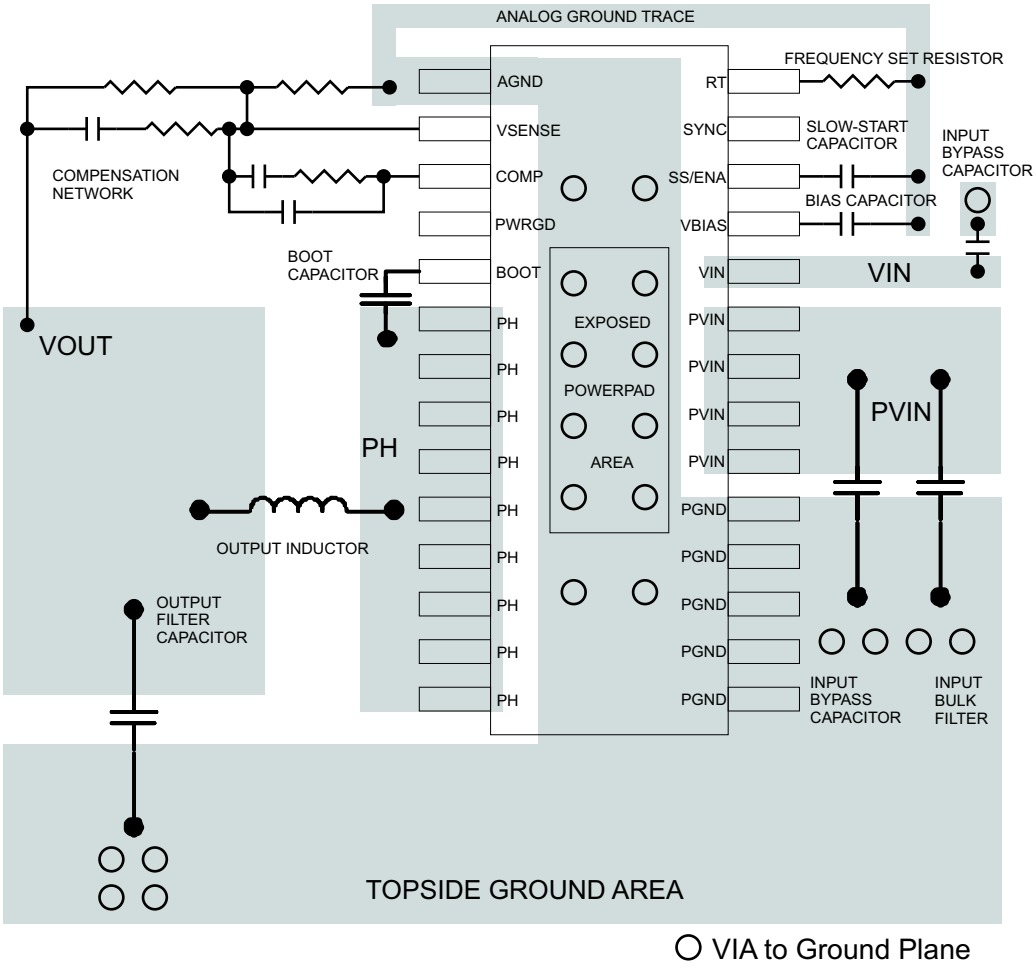


Figure 12. PCB Layout for 28-Pin PWP PowerPAD

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3-inch by 3-inch plane of 1-ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6-A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013-inch diameter vias to avoid solder wicking through the vias.

Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018-inch. Additional vias, beyond the twelve recommended that enhance thermal performance, must be included in areas not under the device package.

PERFORMANCE GRAPHS

Data shown is for the circuit of Figure 10. All data is for VIN = 3.3 V, PVIN = 2.5 V, V_{OUT} = 1.8 V, f_s = 700 kHz, and T_A = 25°C, unless otherwise specified

EFFICIENCY vs OUTPUT CURRENT

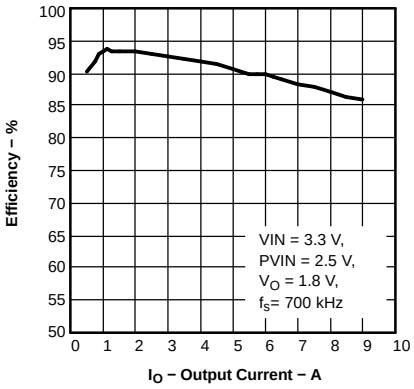


Figure 13.

OUTPUT VOLTAGE CHANGE vs OUTPUT CURRENT

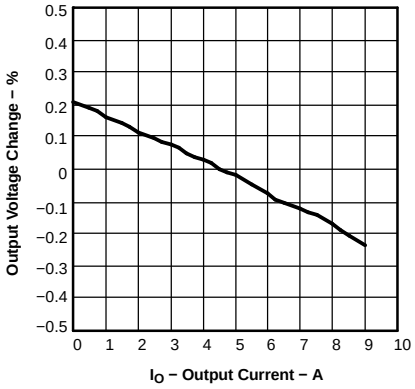


Figure 14.

OUTPUT VOLTAGE CHANGE vs VIN INPUT VOLTAGE

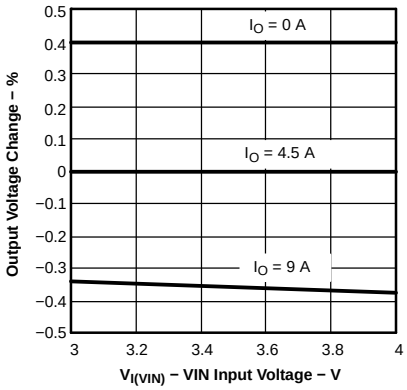


Figure 15.

OUTPUT VOLTAGE CHANGE vs PVIN INPUT VOLTAGE

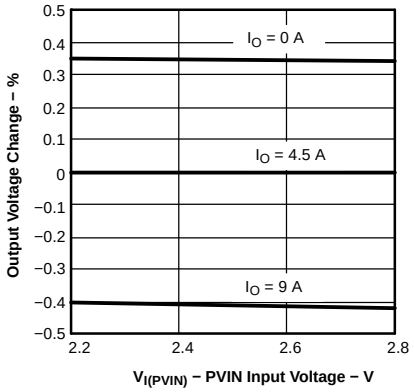


Figure 16.

AMBIENT TEMPERATURE vs LOAD CURRENT(1)

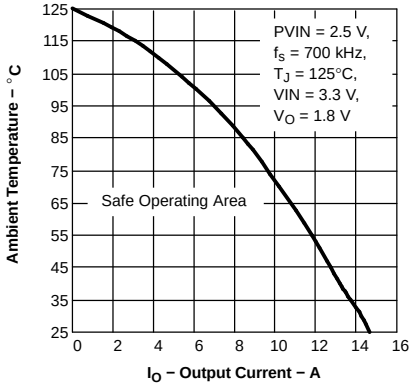


Figure 17.

OUTPUT RIPPLE VOLTAGE

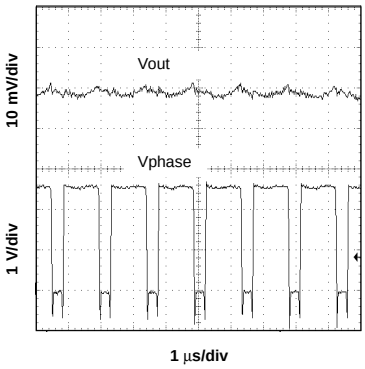


Figure 18.

PERFORMANCE GRAPHS (continued)

INPUT RIPPLE VOLTAGE

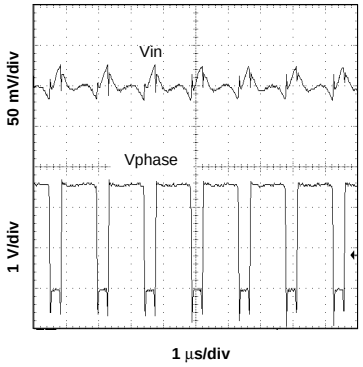


Figure 19.

LOAD TRANSIENT RESPONSE

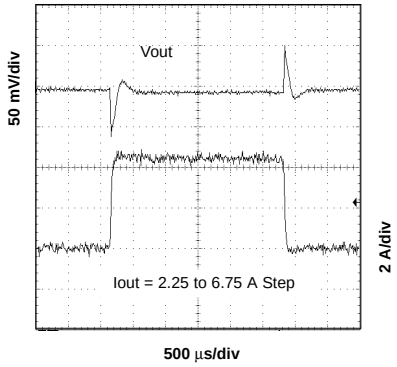


Figure 20.

START UP WAVEFORM(2)

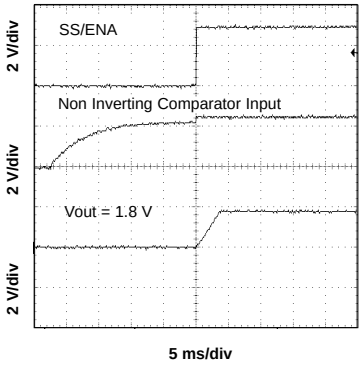


Figure 21.

1. Safe operating area is applicable to the test board conditions in the Dissipation Ratings.
2. Using the undervoltage lockout circuit of Figure 11.

DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS54974 incorporates an undervoltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-μs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. The UVLO is with respect to VIN and not PVIN; see application note.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-μs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (3)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (4)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R- or X5R-grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum

VBIAS of 2.7 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin (see the internal block diagram).

VOLTAGE REFERENCE

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature-stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high-precision regulation of the TPS54974, because it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ [\text{kHz}] \quad (5)$$

ERROR AMPLIFIER

The high-performance, wide bandwidth, voltage error amplifier sets the TPS54974 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54974 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip-point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down on reaching the thermal shutdown trip-point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRGD)

The power-good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of V_{ref}, the open-drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling edge deglitch circuit prevent tripping of the power-good comparator due to high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54974PWP	NRND	HTSSOP	PWP	28		TBD	Call TI	Call TI	-40 to 85	TPS54974	
TPS54974PWPR	OBSOLETE	HTSSOP	PWP	28		TBD	Call TI	Call TI	-40 to 85		
TPS54974PWPRG4	OBSOLETE	HTSSOP	PWP	28		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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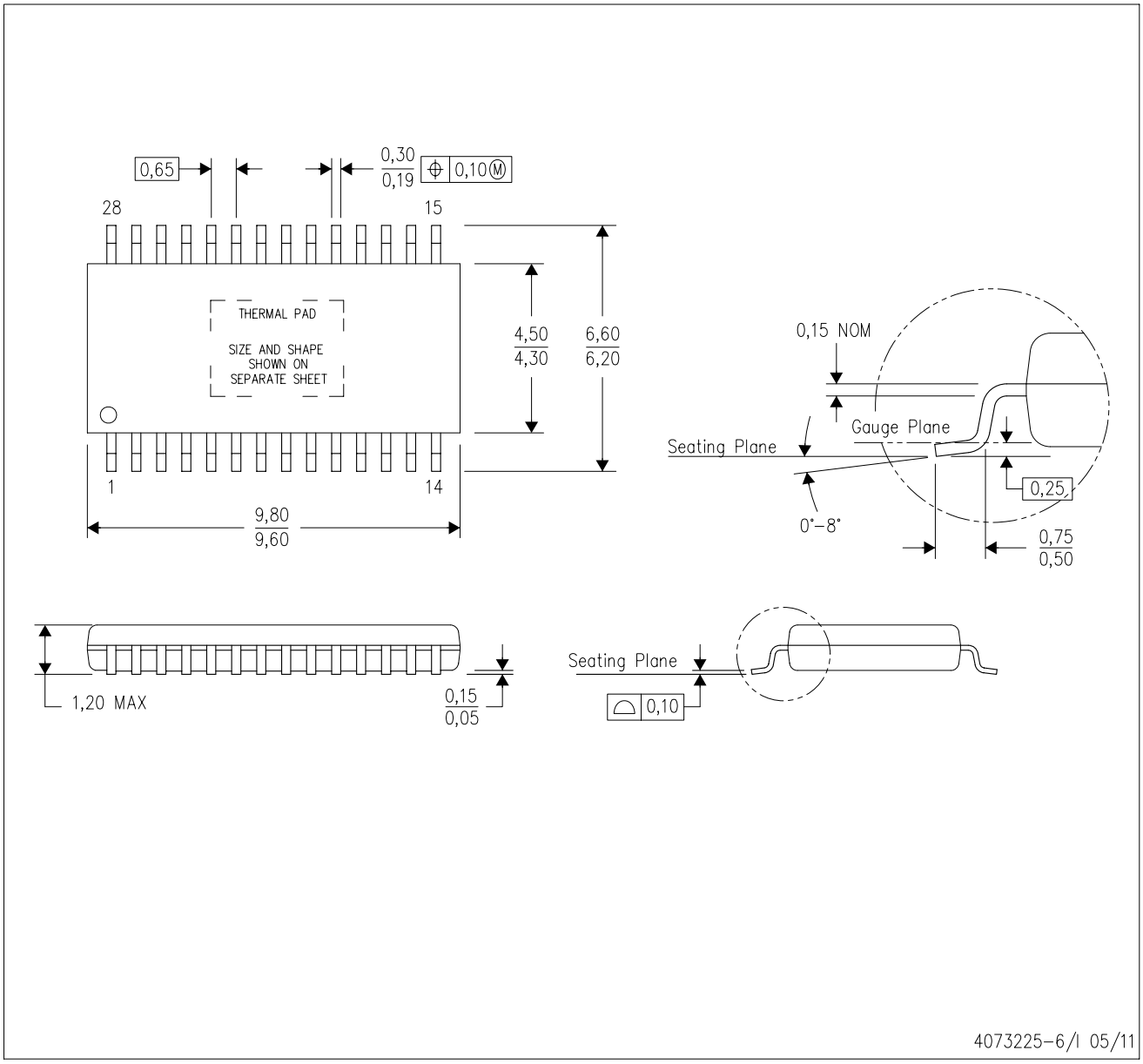
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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