

### PROTECTION PRODUCTS

#### Description

RClamp®2594N is specifically designed to provide secondary surge and ESD protection on high-speed ports. RClamp2594N integrates low capacitance, surge-rated steering diodes with a high power transient voltage suppressor (TVS). The TVS utilizes snap-back or “crow-bar” technology to minimize device clamping voltage and features high surge current capability of 35A ( $t_p=8/20\mu s$ ). ESD characteristics are highlighted by high ESD withstand voltage ( $\pm 30kV$  per IEC 61000-4-2) and extremely low dynamic resistance (0.05 Ohms typical). Each device will protect four lines operating at 5 volts.

RClamp2594N is in a DFN 3.0 x 2.0 x 0.4mm 10 Lead package. The leads are finished with NiPdAu.

#### Features

- Transient Protection to
  - ♦ IEC 61000-4-2 (ESD) 30kV (Air), 30kV (Contact)
  - ♦ IEC 61000-4-4 (EFT) 4kV (5/50ns)
  - ♦ IEC 61000-4-5 (Lightning) 35A (8/20 $\mu s$ )
- Very Small PCB Area
- Protects four High-Speed Data Lines
- Working Voltage: 5V
- Low Capacitance: 3pF Maximum
- Dynamic Resistance: 0.05 Ohms (Typ)
- Solid-State Silicon-Avalanche Technology

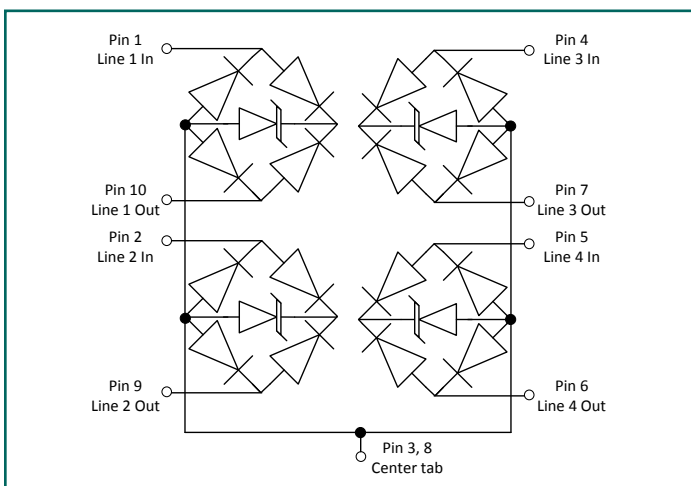
#### Mechanical Characteristics

- Package: DFN 3.0 x 2.0 x 0.4mm 10 Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 3.0 x 2.0 x 0.40 mm
- Lead Finish: NiPdAu
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

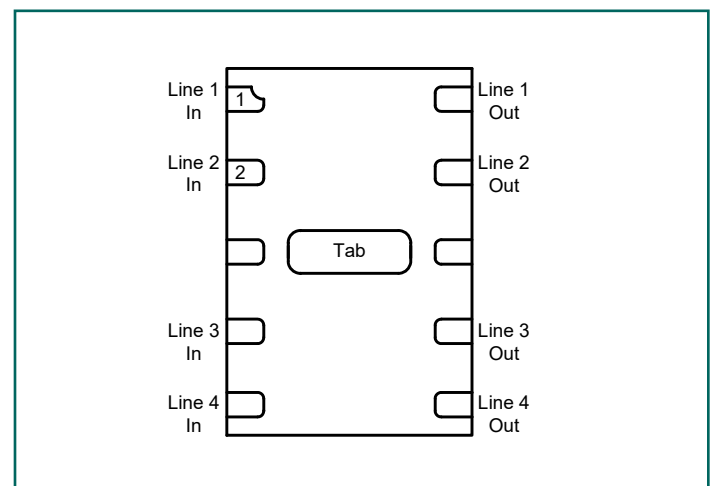
#### Applications

- Gigabit Ethernet
- 2.5GbE
- Integrated Magnetics / RJ-45 Connectors
- Central office Equipment
- Industrial Equipment
- LVDS Interfaces

#### Functional Schematic



#### Pin Configuration



## Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P <sub>PK</sub>	300	W
Peak Pulse Current (tp = 8/20μs)	I <sub>PP</sub>	35	A
ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup> ESD per IEC 61000-4-2 (Air) <sup>(1)</sup>	V <sub>ESD</sub>	±30 ±30	kV
Operating Temperature	T <sub>OP</sub>	-40 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

## Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	
Reverse Stand-Off Voltage	V <sub>RWM</sub>	-40°C to 125°C, any I/O Pin to GND			5	V	
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 10mA, Any I/O Pin to GND	-40°C to 125°C	6.5	9.5	11.5	V
Holding Current	I <sub>H</sub>	T = 25°C	75	150	250	mA	
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V	T = 25°C		0.01	0.100	μA
			T = 125°C		0.03	0.325	μA
Clamping Voltage <sup>(2)</sup>	V <sub>C</sub>	I <sub>PP</sub> = 35A, tp = 8/20μs, Line 1 to Line 2 or Line 3 to Line 4		7.5	8.5	V	
ESD Clamping Voltage <sup>(3)</sup>	V <sub>C</sub>	I <sub>PP</sub> = 4A, tp = 0.2/100ns (TLP) Any I/O Pin to GND		4.2		V	
ESD Clamping Voltage <sup>(3)</sup>	V <sub>C</sub>	I <sub>PP</sub> = 16A, tp = 0.2/100ns (TLP) Any I/O Pin to GND		4.7		V	
Dynamic Resistance <sup>(3), (4)</sup>	R <sub>DYN</sub>	tp = 0.2/100ns (TLP)		0.05		Ohms	
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0V, f = 1MHz, any I/O Pin to GND		2.1	3	pF	

### Notes:

(1): ESD Gun return path to Ground Reference Plane (GRP)

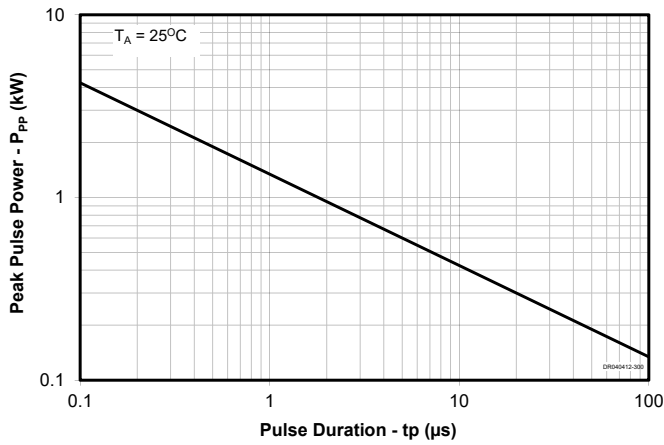
(2): Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, R<sub>s</sub> = 2 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I<sub>TLP</sub> and V<sub>TLP</sub> averaging window: t<sub>1</sub> = 70ns to t<sub>2</sub> = 90ns.

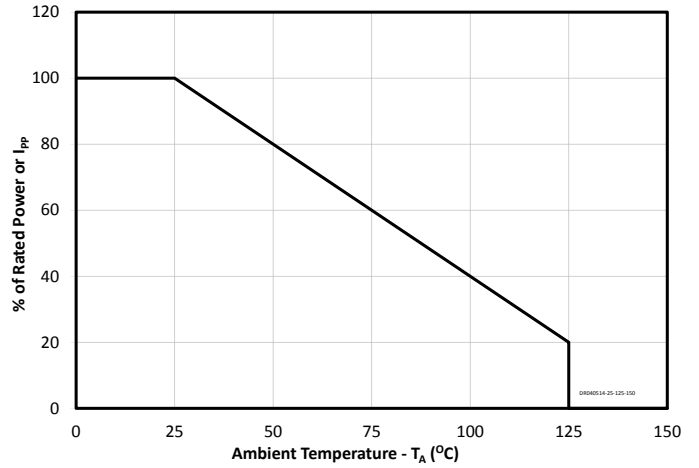
(4): Dynamic resistance calculated from I<sub>TLP</sub> = 4A to I<sub>TLP</sub> = 16A

# Typical Characteristics

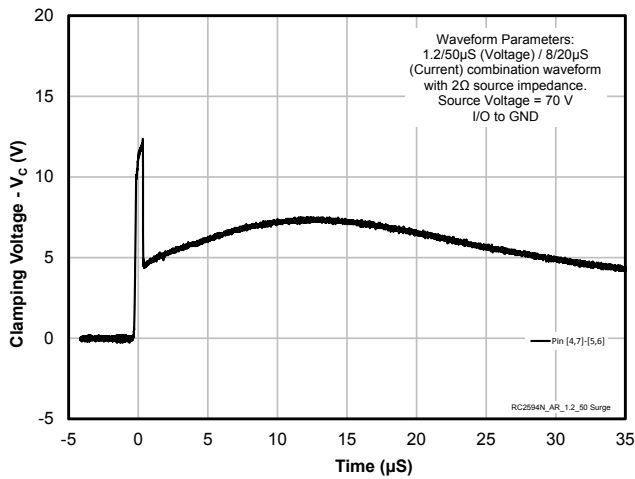
**Non-Repetitive Peak Pulse Power vs. Pulse Time**



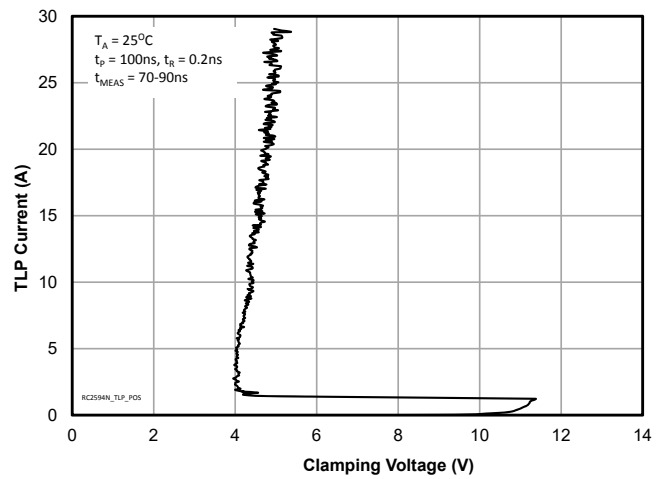
**Power Derating Curve**



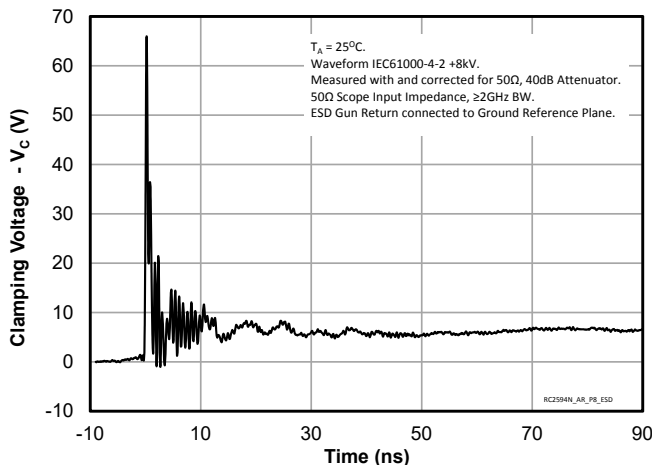
**Clamping Characteristic (70V/2 Ohms, 1.2/50us Pulse)**



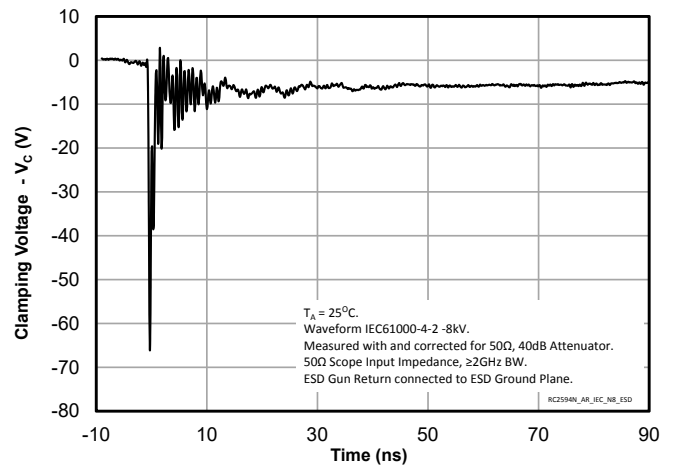
**TLP IV Curve (Positive Pulse)**



**ESD Clamping (+8kV Contact per IEC 61000-4-2)**

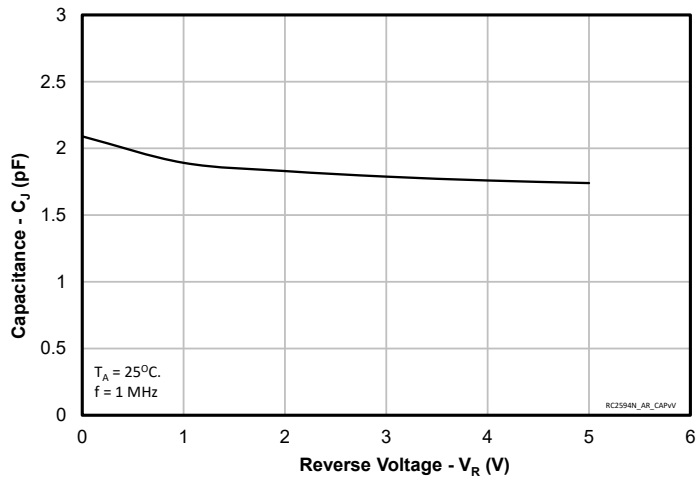


**ESD Clamping (-8kV Contact per IEC 61000-4-2)**

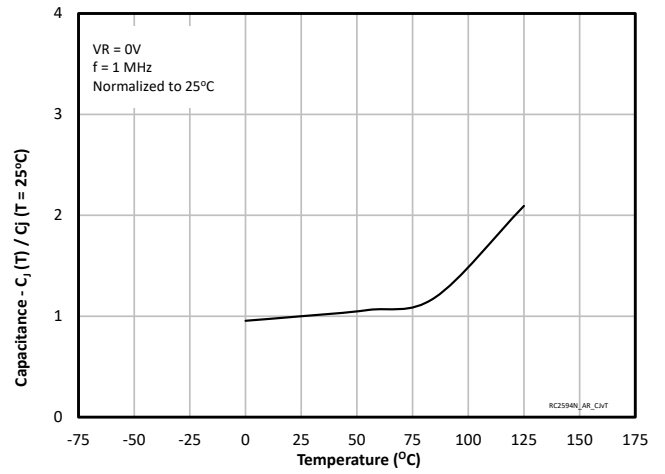


## Typical Characteristics (Continued)

### Capacitance vs. Reverse Voltage (Line to GND)



### Capacitance vs. Temperature (Line to GND)



# Application Information

## Ethernet Protection

Ethernet ports are exposed to external transient events in the form of ESD, EFT, lightning, and cable discharge events (CDE). Test standards that model these events include IEC 61000-4-2 for ESD, IEC 61000-4-4 for EFT, and IEC 61000-4-5 and GR-1089 for lightning. Any of these events can cause catastrophic damage to the PHY IC.

When designing Ethernet protection, the entire system must be considered. Over-voltage events can be common mode (with respect to ground) or differential (line-to-line). An Ethernet port includes interface magnetics consisting of transformers integrated with common mode chokes. The transformer center taps are connected to ground via an RC network or “Bob Smith” termination. The purpose of this termination is to reduce common mode emissions. The transformer provides common mode isolation to transient events, but no protection for differential surges. During a differential transient event, current will flow through the transformer, charging the windings on the line side. Energy is transferred to the secondary until the surge subsides or the transformer saturates.

A typical protection scheme which utilizes RClamp2594N is shown in Figure 1. The devices are located on the PHY side of the transformer with one device placed across two line pairs. Parasitic inductance in the protection

path should be minimized by locating RClamp2594N as physically close to the magnetics as possible, and preferably on the same side of the PCB. Reducing parasitic inductance is especially important for suppressing fast rise time transients such as ESD and EFT. Inductance in the path of the protection device increases the peak clamping voltage seen by the protected device ( $V = L di/dt$ ). Differential pairs are routed through each RClamp2594N. Traces are routed unbroken to connect pins 1 and 10 (Line 1), 2 and 9 (Line 2), 4 and 7 (Line 3) and 5 and 6 (Line 4). Pins 3 and 8 as well as the tab are not connected.

Placing the protection on the PHY side of the magnetics is advantageous in that the magnitude and duration of the surge is attenuated by the transformer windings. The amount of attenuation will vary by vendor and configuration of the magnetics. The Ethernet transformer has to be able to support the impulse tests without failure. A typical Ethernet transformer can withstand a few hundred amperes ( $t_p=8/20\mu s$ ) before failure occurs, but this needs to be verified by testing. Alternatively, the protection can be placed on the line side of the transformer. However, the additional protection afforded by the transformer is lost, and the ability of the system to withstand high energy surges is limited to the capability of the protection device.

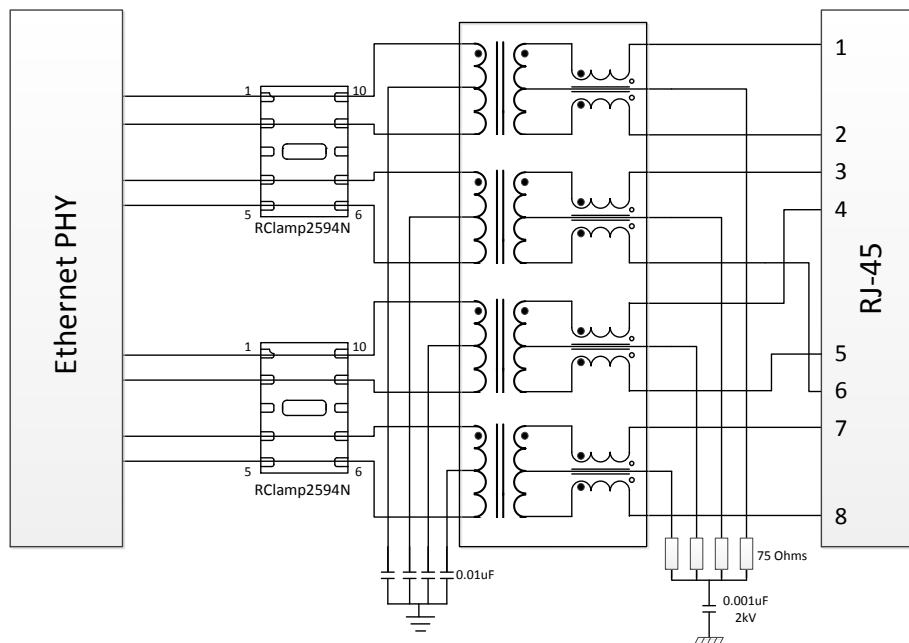
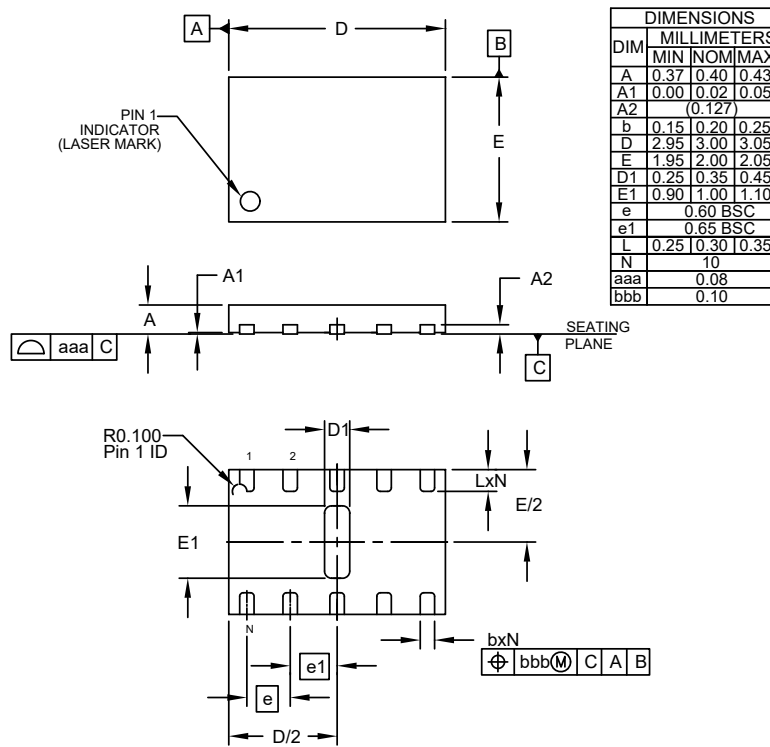


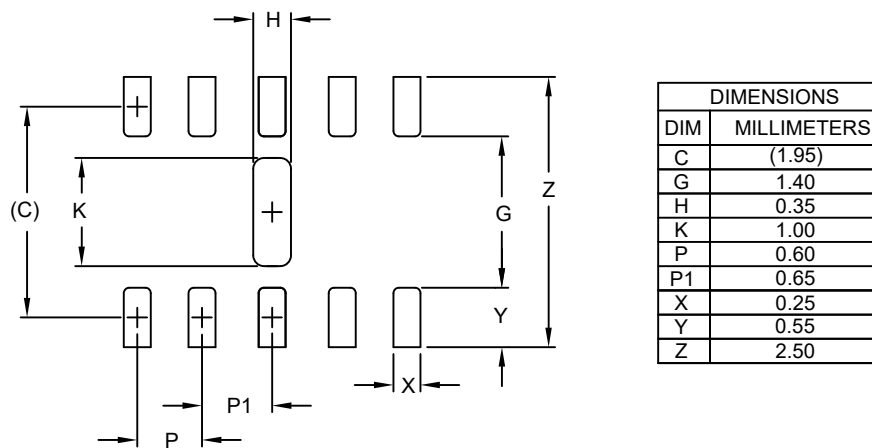
Figure 1 - Typical Ethernet Protection Circuit

## Outline Drawing - DFN 3.0 x 2.0 x 0.4mm 10 Lead



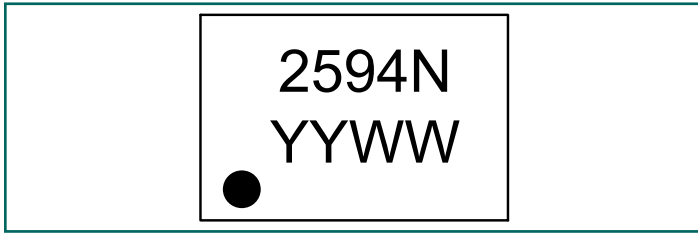
NOTES:  
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

## Land Pattern - DFN 3.0 x 2.0 x 0.4mm 10 Lead



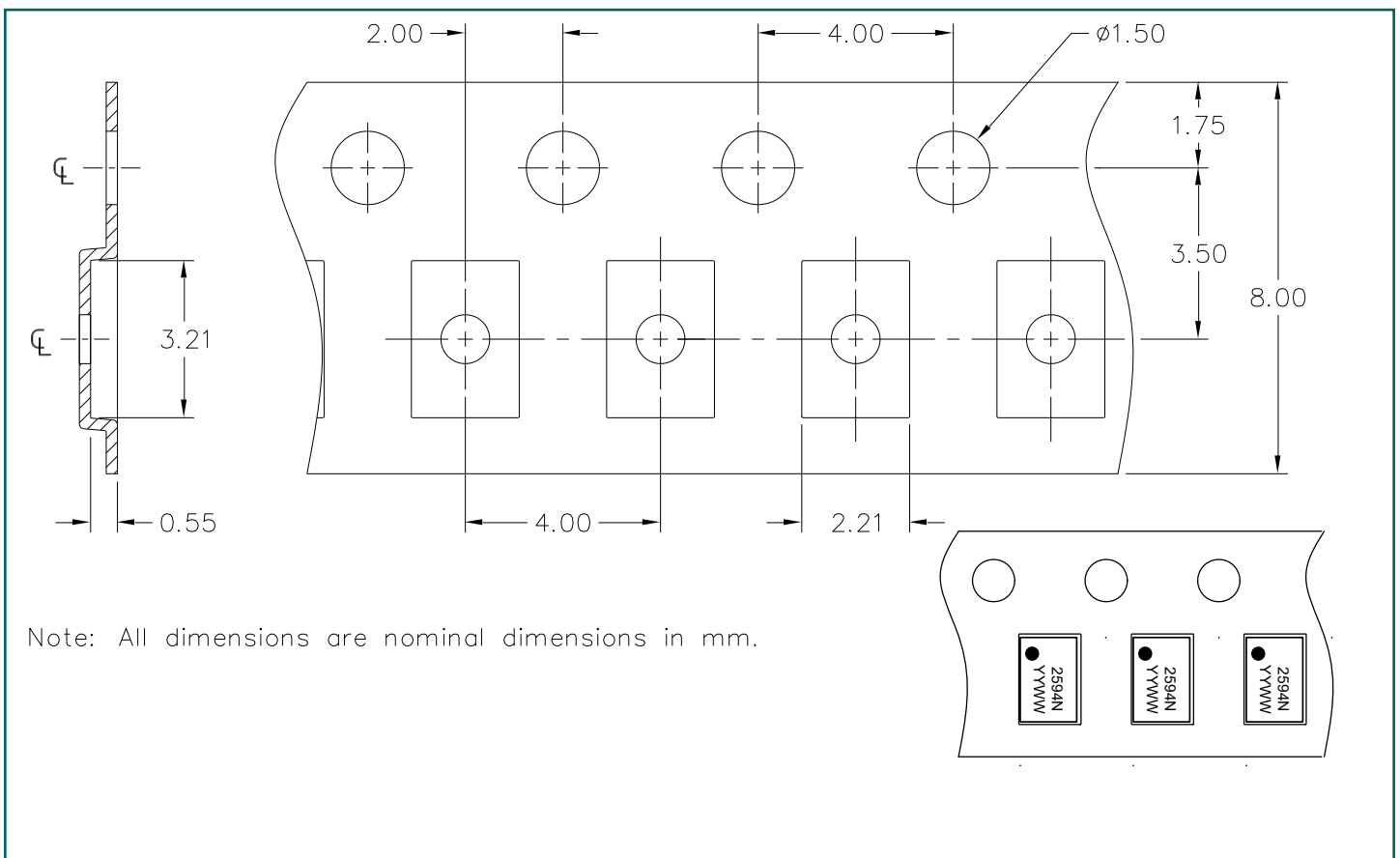
NOTES:  
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).  
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

## Marking Code



Notes: Dot indicates Pin 1 Location

## Tape and Reel Specification



## Ordering Information

Part Number	Qty per Reel	Reel Size	Carrier Tape	Pitch
RClamp2594N.TCT	3000	7 Inch	Plastic	4mm

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