14-/12-Bit, 250MSPS, Ultralow-Power ADC with Analog Buffers

Check for Samples: ADS41B29, ADS41B49

FEATURES

- **ADS41B49: 14-Bit, 250MSPS**
  ADS41B29: 12-Bit, 250MSPS
- **Integrated High-Impedance Analog Input Buffer:**
  - **Input Capacitance: 2pF**
  - **200MHz Input Resistance: 3kΩ**
- **Maximum Sample Rate: 250MSPS**
- **Ultralow Power:**
  - **1.8V Analog Power: 180mW**
  - **3.3V Buffer Power: 96mW**
  - **I/O Power: 135mW (DDR LVDS)**
- **High Dynamic Performance:**
  - **SNR: 69dBFS at 170MHz**
  - **SFDR: 82.5dBc at 170MHz**
- **Output Interface:**
  - **Double Data Rate (DDR) LVDS with Programmable Swing and Strength:**
    - **Standard Swing: 350mV**
    - **Low Swing: 200mV**
    - **Default Strength: 100Ω Termination**
    - **2x Strength: 50Ω Termination**
  - **1.8V Parallel CMOS Interface Also Supported**
- **Programmable Gain for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude**
- **Package: QFN-48 (7mm × 7mm)**

DESCRIPTION

The ADS41B29/B49 are members of the ultralow-power ADS4xxx analog-to-digital converter (ADC) family, featuring integrated analog input buffers. These devices use innovative design techniques to achieve high dynamic performance, while consuming extremely low power. The analog input pins have buffers, with benefits of constant performance and input impedance across a wide frequency range. The devices are well-suited for multi-carrier, wide bandwidth communications applications such as PA linearization.

The ADS41B49/29 have features such as digital gain and offset correction. The gain option can be used to improve SFDR performance at lower full-scale input ranges, especially at high input frequencies. The integrated dc offset correction loop can be used to estimate and cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance.

The devices support both double data rate (DDR) low-voltage differential signaling (LVDS) and parallel CMOS digital output interfaces. The low data rate of the DDR LVDS interface (maximum 500MBPS) makes it possible to use low-cost field-programmable gate array (FPGA)-based receivers. The devices have a low-swing LVDS mode that can be used to further reduce the power consumption. The strength of the LVDS output buffers can also be increased to support 50Ω differential termination.

The devices are available in a compact QFN-48 package and are specified over the industrial temperature range (–40°C to +85°C).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS41B29	QFN-48	RGZ	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ41B29	ADS41B29IRGZR	Tape and reel
							ADS41B29IRGZT	Tape and reel
ADS41B49	QFN-48	RGZ	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ41B49	ADS41B49IRGZR	Tape and reel
							ADS41B49IRGZT	Tape and reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

ABSOLUTE MAXIMUM RATINGS(1)

		ADS41B29, ADS41B49		UNIT
		MIN	MAX	
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, AVDD_BUF		–0.3	3.9	V
Supply voltage range, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4	2.4	V
Voltage between AVDD_BUF to DRVDD/AVDD		–4.2	4.2	V
Voltage applied to input pins	INP, INM	–0.3	Minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, DFS	–0.3	AVDD + 0.3	V
Operating free-air temperature range, T_A		–40	+85	°C
Operating junction temperature range, T_J			+125	°C
Storage temperature range, T_{stg}		–65	+150	°C
ESD, human body model (HBM)			2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|. Doing so prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC[1]		ADS41B29, ADS41B49 RGZ 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	29	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	n/a	
θ_{JB}	Junction-to-board thermal resistance	10	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.13	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		ADS41B29, ADS41B49			UNIT
		MIN	TYP	MAX	
SUPPLIES					
AVDD	Analog supply voltage	1.7	1.8	1.9	V
AVDD_BUF	Analog buffer supply voltage	3	3.3	3.6	V
DRVDD	Digital supply voltage	1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input voltage range[1]			1.5		V_{PP}
Input common-mode voltage			1.7 ± 0.05		V
Maximum analog input frequency with 1.5V_{PP} input amplitude[2]			400		MHz
Maximum analog input frequency with 1V_{PP} input amplitude[2]			600		MHz
CLOCK INPUT					
ADS41B29/ ADS41B49	Low-speed mode enabled[3]	20		80	MSPS
	Low-speed mode disabled[3]	> 80		250	MSPS
Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)					
	Sine wave, ac-coupled	0.2	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled		1.8		V
Input clock duty cycle	Low-speed mode enabled	40	50	60	%
	Low-speed mode disabled	35	50	65	%
DIGITAL OUTPUTS					
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND		5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
T_A	Operating free-air temperature	–40		+85	°C
HIGH-PERFORMANCE MODES[4][5][6]					
MODE 1	Set the MODE 1 register bits to get the best performance across sample clock and input signal frequencies. Register address = 03h, register data = 03h.				
MODE 2	Set the MODE 2 register bit to get the best performance at high input signal frequencies greater than 230MHz. Register address = 4Ah, register data = 01h.				

(1) With 0dB gain. See the *Gain for SFDR/SNR Trade-Off* section in *Application Information* for the relationship between input voltage range and gain.
(2) See the *Theory of Operation* section in the *Application Information*.
(3) See the *Serial Interface* section for details on the low-speed mode.
(4) It is recommended to use these modes to get best performance. These modes can only be set with the serial interface.
(5) See the *Serial Interface* section for details on register programming.
(6) Note that these modes cannot be set when the serial interface is not used (when the RESET pin is tied high); see the *Device Configuration* section.

ELECTRICAL CHARACTERISTICS: ADS41B29, ADS41B49

Typical values are at +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, 1.5V_{PP} clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, AVDD_BUF = 3.3V, and DRVDD = 1.8V.

PARAMETER		TEST CONDITIONS	ADS41B29			ADS41B49			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution					12			14	Bits
SNR (signal-to-noise ratio), LVDS		f_{IN} = 20MHz		68.4			69.7		dBFS
		f_{IN} = 70MHz		68.3			69.5		dBFS
		f_{IN} = 100MHz		68.3			69.5		dBFS
		f_{IN} = 170MHz	65.5	68		66.5	69.1		dBFS
		f_{IN} = 300MHz		67.5			68.4		dBFS
SINAD (signal-to-noise and distortion ratio), LVDS		f_{IN} = 20MHz		68.3			69.5		dBFS
		f_{IN} = 70MHz		68.1			69.3		dBFS
		f_{IN} = 100MHz		68.2			69.3		dBFS
		f_{IN} = 170MHz	65	67.8		66	68.8		dBFS
		f_{IN} = 300MHz		66.5			67.4		dBFS
Spurious-free dynamic range	SFDR	f_{IN} = 20MHz		89			89		dBc
		f_{IN} = 70MHz		85			85		dBc
		f_{IN} = 100MHz		87			87		dBc
		f_{IN} = 170MHz	71	82		72	82		dBc
		f_{IN} = 300MHz		75			75		dBc
Total harmonic distortion	THD	f_{IN} = 20MHz		85			85		dBc
		f_{IN} = 70MHz		82			82		dBc
		f_{IN} = 100MHz		83			83		dBc
		f_{IN} = 170MHz	68	79.5		69	79.5		dBc
		f_{IN} = 300MHz		72			72		dBc
Second-harmonic distortion	HD2	f_{IN} = 20MHz		93			93		dBc
		f_{IN} = 70MHz		85			85		dBc
		f_{IN} = 100MHz		87			87		dBc
		f_{IN} = 170MHz	71	87		72	87		dBc
		f_{IN} = 300MHz		80			80		dBc
Third-harmonic distortion	HD3	f_{IN} = 20MHz		93			93		dBc
		f_{IN} = 70MHz		88			88		dBc
		f_{IN} = 100MHz		88			88		dBc
		f_{IN} = 170MHz	71	82		72	82		dBc
		f_{IN} = 300MHz		75			75		dBc
Worst spur (other than second and third harmonics)		f_{IN} = 20MHz		89			89		dBc
		f_{IN} = 70MHz		90			90		dBc
		f_{IN} = 100MHz		90			90		dBc
		f_{IN} = 170MHz	76	88		77.5	88		dBc
		f_{IN} = 300MHz		88			88		dBc
Two-tone intermodulation distortion	IMD	f_1 = 185MHz, f_2 = 190MHz, each tone at –7dBFS		–86			–86		dBFS
Input overload recovery		Recovery to within 1% (of final value) for 6dB overload with sine-wave input		1			1		Clock cycles
AC power-supply rejection ratio	PSRR	For 100mV_{PP} signal on AVDD supply, up to 10MHz		> 30			> 30		dB
Effective number of bits	ENOB	f_{IN} = 170MHz		11			11.2		LSBs
Integrated nonlinearity	INL	f_{IN} = 170MHz		±1.5	±3.5		±2.5	±5	LSBs

ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, and 50% clock duty cycle, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, AVDD_BUF = 3.3V, and DRVDD = 1.8V.

PARAMETER		ADS41B29, ADS41B49			UNIT
		MIN	TYP	MAX	
ANALOG INPUTS					
Differential input voltage range			1.5		V_{PP}
Differential input resistance, at dc (see Figure 60)			10		kΩ
Differential input capacitance (see Figure 61)			2		pF
Analog input bandwidth			800		MHz
Analog input common-mode current (per input pin)			2		µA
Common-mode output voltage	VCM		1.7		V
VCM output current capability			4		mA
DC ACCURACY					
Offset error		–15	2.5	15	mV
Temperature coefficient of offset error			0.003		mV/°C
Gain error as a result of internal reference inaccuracy alone	E_{GREF}	–2		2	%FS
Gain error of channel alone	E_{GCHAN}		2.5		%FS
POWER SUPPLY					
IAVDD Analog supply current			99.5	115	mA
IAVDD_BUF Analog input buffer supply current			29	42	mA
IDRVDD(1) Output buffer supply current LVDS interface with 100Ω external termination Low LVDS swing (200mV)			63		mA
IDRVDD Output buffer supply current LVDS interface with 100Ω external termination Standard LVDS swing (350mV)			75	90	mA
IDRVDD output buffer supply current(1)(2) CMOS interface(2) 8pF external load capacitance f_{IN} = 2.5MHz			35		mA
Global power-down			10	25	mW
Standby			200		mW

(1) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10pF.

(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

DIGITAL CHARACTERISTICS

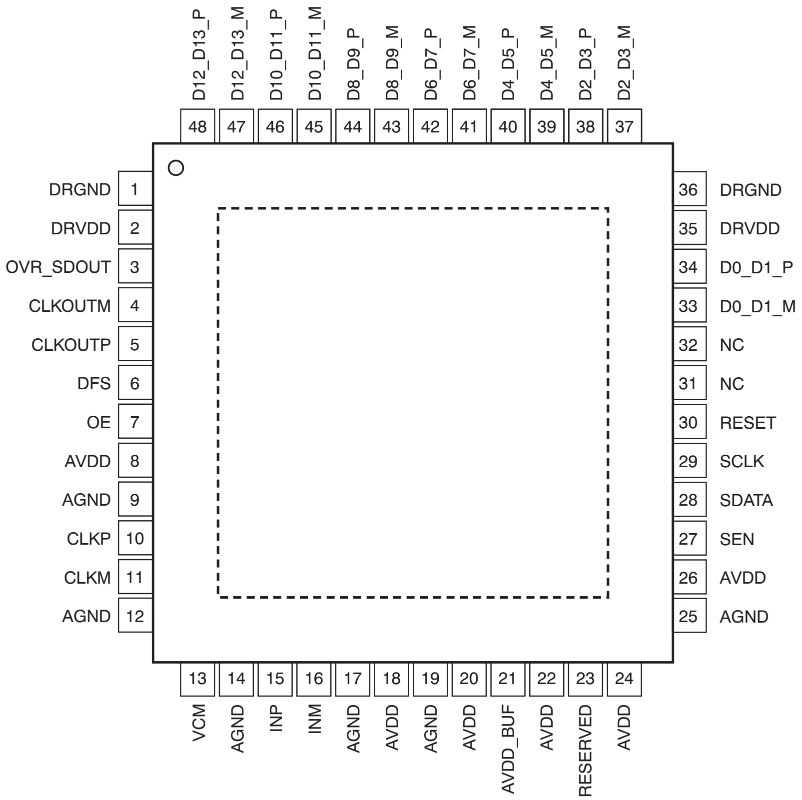
Typical values are at +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, and DRVDD = 1.8V, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, AVDD_BUF = 3.3V, and DRVDD = 1.8V.

PARAMETER		TEST CONDITIONS	ADS41B29, ADS41B49			UNIT
			MIN	TYP	MAX	
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, OE)						
High-level input voltage		RESET, SCLK, SDATA, and SEN support 1.8V and 3.3V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input voltage		OE only supports 1.8V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input current: SDATA, SCLK[1]		V_{HIGH} = 1.8V		10		µA
High-level input current: SEN[2]		V_{HIGH} = 1.8V		0		µA
Low-level input current: SDATA, SCLK		V_{LOW} = 0V		0		µA
Low-level input current: SEN		V_{LOW} = 0V		–10		µA
DIGITAL OUTPUTS (CMOS INTERFACE: D0 TO D13, OVR_SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: D0_D1_P/M to D12_D13_P/M, CLKOUTP/M)						
High-level output voltage[3]	V_{ODH}	Standard swing LVDS	270	+350	430	mV
Low-level output voltage[3]	V_{ODL}	Standard swing LVDS	–430	–350	–270	mV
High-level output voltage[3]	V_{ODH}	Low swing LVDS		+200		mV
Low-level output voltage[3]	V_{ODL}	Low swing LVDS		–200		mV
Output common-mode voltage	V_{OCM}		0.85	1.05	1.25	V

(1) SDATA and SCLK have an internal 180kΩ pull-down resistor.
(2) SEN has an internal 180kΩ pull-up resistor to AVDD.
(3) With an external 100Ω termination.

PIN CONFIGURATION (LVDS MODE)

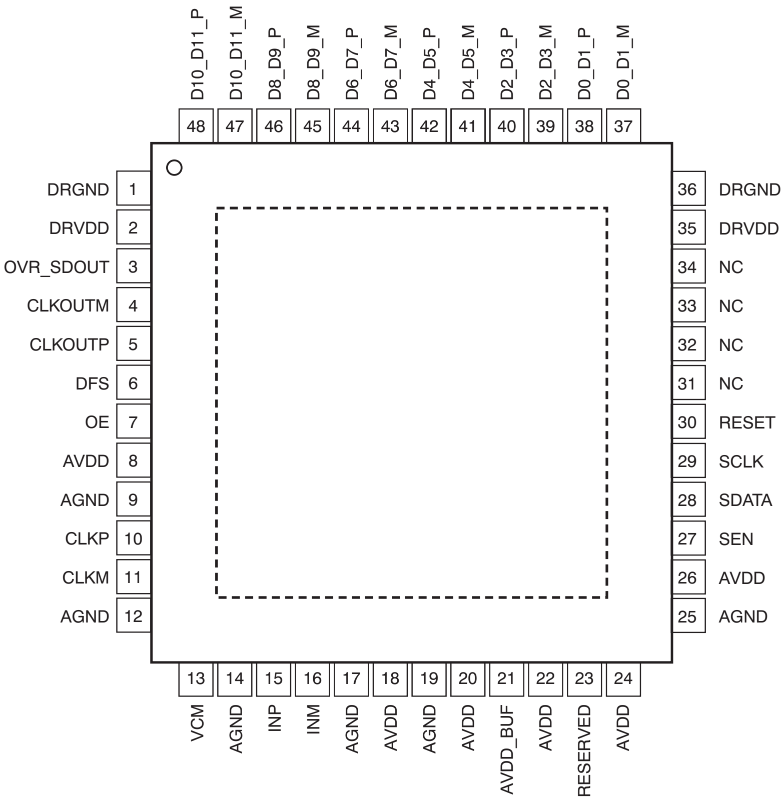
RGZ PACKAGE[1]
QFN-48
(TOP VIEW)



(1) The PowerPAD is connected to DRGND.

Figure 1. ADS41B49 LVDS Pinout

RGZ PACKAGE[2]
QFN-48
(TOP VIEW)



(2) The PowerPAD™ is connected to DRGND.

Figure 2. ADS41B29 LVDS Pinout

ADS41B49, ADS41B29 Pin Descriptions (LVDS Mode)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	8, 18, 20, 22, 24, 26	6	I	1.8V analog power supply
AVDD_BUF	21	1	I	3.3V input buffer supply
AGND	9, 12, 14, 17, 19, 25	6	I	Analog ground
CLKP	10	1	I	Differential clock input, positive
CLKM	11	1	I	Differential clock input, negative
INP	15	1	I	Differential analog input, positive
INM	16	1	I	Differential analog input, negative
VCM	13	1	O	Outputs the common-mode voltage that can be used externally to bias the analog input pins.
RESET	30	1	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SDATA can be used as a control pin. RESET has an internal 100kΩ pull-down resistor.
SCLK	29	1	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180kΩ pull-down resistor
SDATA	28	1	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 7). This pin has an internal 180kΩ pull-down resistor.

ADS41B49, ADS41B29 Pin Descriptions (LVDS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
SEN	27	1	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180kΩ pull-up resistor to AVDD.
OE	7	1	I	Output buffer enable input, active high; this pin has an internal 100kΩ pull-up resistor to DRVDD.
DFS	6	1	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS/CMOS output interface type.
RESERVED	23	1	I	Digital control pin, reserved for future use
CLKOUTP	5	1	O	Differential output clock, true
CLKOUTM	4	1	O	Differential output clock, complement
D0_D1_P	Refer to Figure 1	1	O	Differential output data D0 and D1 multiplexed, true
D0_D1_M	Refer to Figure 1	1	O	Differential output data D0 and D1 multiplexed, complement
D2_D3_P	Refer to Figure 1	1	O	Differential output data D2 and D3 multiplexed, true
D2_D3_M	Refer to Figure 1	1	O	Differential output data D2 and D3 multiplexed, complement
D4_D5_P	Refer to Figure 1	1	O	Differential output data D4 and D5 multiplexed, true
D4_D5_M	Refer to Figure 1	1	O	Differential output data D4 and D5 multiplexed, complement
D6_D7_P	Refer to Figure 1	1	O	Differential output data D6 and D7 multiplexed, true
D6_D7_M	Refer to Figure 1	1	O	Differential output data D6 and D7 multiplexed, complement
D8_D9_P	Refer to Figure 1	1	O	Differential output data D8 and D9 multiplexed, true
D8_D9_M	Refer to Figure 1	1	O	Differential output data D8 and D9 multiplexed, complement
D10_D11_P	Refer to Figure 1	1	O	Differential output data D10 and D11 multiplexed, true
D10_D11_M	Refer to Figure 1	1	O	Differential output data D10 and D11 multiplexed, complement
D12_D13_P	Refer to Figure 1	1	O	Differential output data D12 and D13 multiplexed, true
D12_D13_M	Refer to Figure 1	1	O	Differential output data D12 and D13 multiplexed, complement
OVR_SDOUT	3	1	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1. This pin is a 1.8V CMOS output pin (running off of DRVDD).
DRVDD	2, 35	2	I	1.8V digital and output buffer supply
DRGND	1, 36, PAD	2	I	Digital and output buffer ground
NC	Refer to Figure 1	—	—	Do not connect

FUNCTIONAL BLOCK DIAGRAM

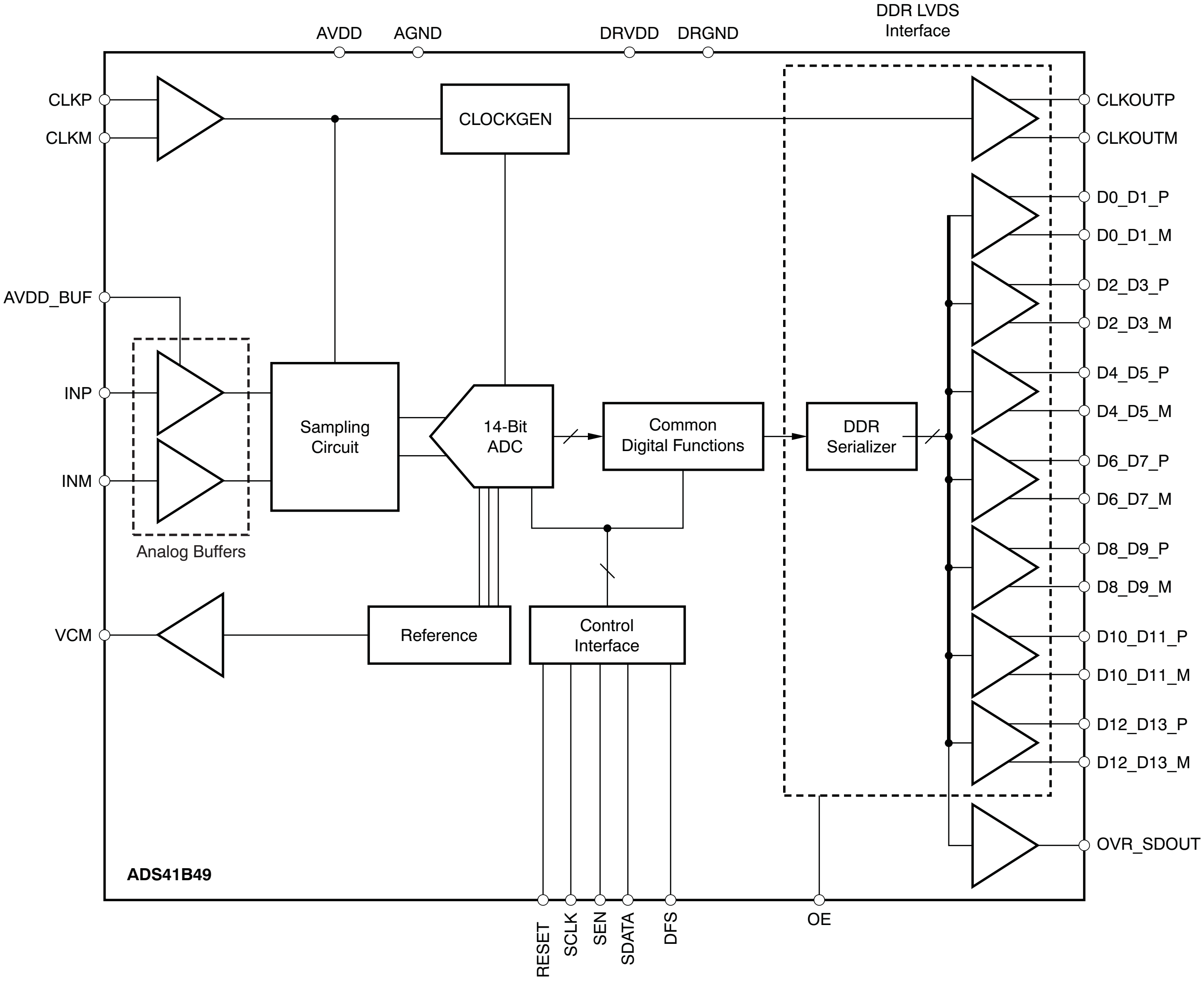
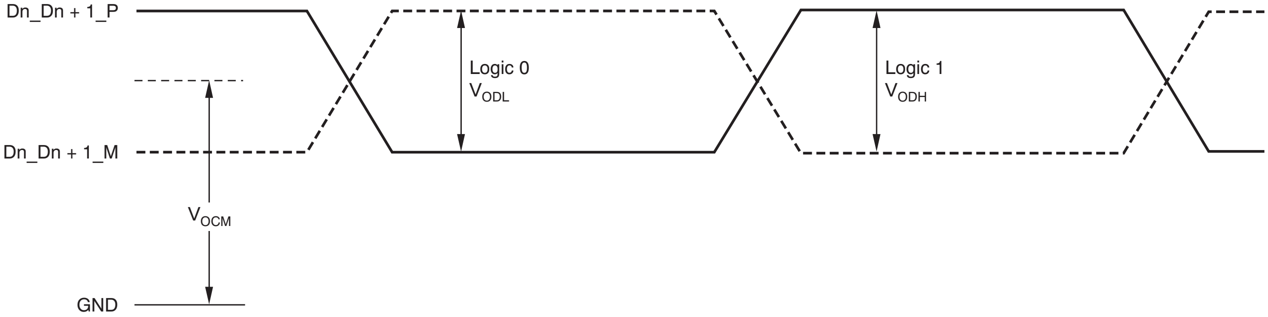


Figure 3. ADS41B49 Block Diagram

TIMING CHARACTERISTICS



(1) With external 100Ω termination.

Figure 4. LVDS Output Voltage Levels

TIMING REQUIREMENTS: LVDS and CMOS Modes(1)

Typical values are at +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5pF(2), and R_{LOAD} = 100Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, AVDD_BUF = 3.3V, and DRVDD = 1.7V to 1.9V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.6	0.8	1.2	ns
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±100		ps
t_J	Aperture jitter			100		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of PDN GLOBAL mode		100	500	µs
	ADC latency(4)	Gain enabled (default after reset)		21		Clock cycles
		Gain and offset correction enabled		22		Clock cycles
DDR LVDS MODE						
t_{SU}	Data setup time(5)	Data valid(6) to zero-crossing of CLKOUTP	0.75	1.1		ns
t_H	Data hold time(5)	Zero-crossing of CLKOUTP to data becoming invalid(6)	0.35	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ sampling frequency ≤ 250MSPS*	3	4.2	5.4	ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		±0.6		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP – CLKOUTM) *1MSPS ≤ sampling frequency ≤ 250MSPS*	42	48	54	%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ sampling frequency ≤ 250MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ sampling frequency ≤ 250MSPS*		0.14		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		50	100	ns
PARALLEL CMOS MODE(7)						
t_{START}	Input clock to data delay	Input clock rising edge cross-over to start of data valid(6)			1.6	ns
t_{DV}	Data valid time	Time interval of valid data(6)	2.5	3.2		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ sampling frequency ≤ 200MSPS*	4	5.5	7	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1MSPS ≤ sampling frequency ≤ 200MSPS*		47		%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 250MSPS*		0.35		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 200MSPS*		0.35		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20	40	ns

(1) Timing parameters are ensured by design and characterization but are not production tested.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) R_{LOAD} is the differential load resistance between the LVDS output pair.
(6) Data valid refers to a logic high of 1.26V and a logic low of 0.54V.
(7) For f_S > 200MSPS, it is recommended to use an external clock for data capture instead of the device output clock signal (CLKOUT).

Table 1. LVDS Timing Across Sampling Frequencies

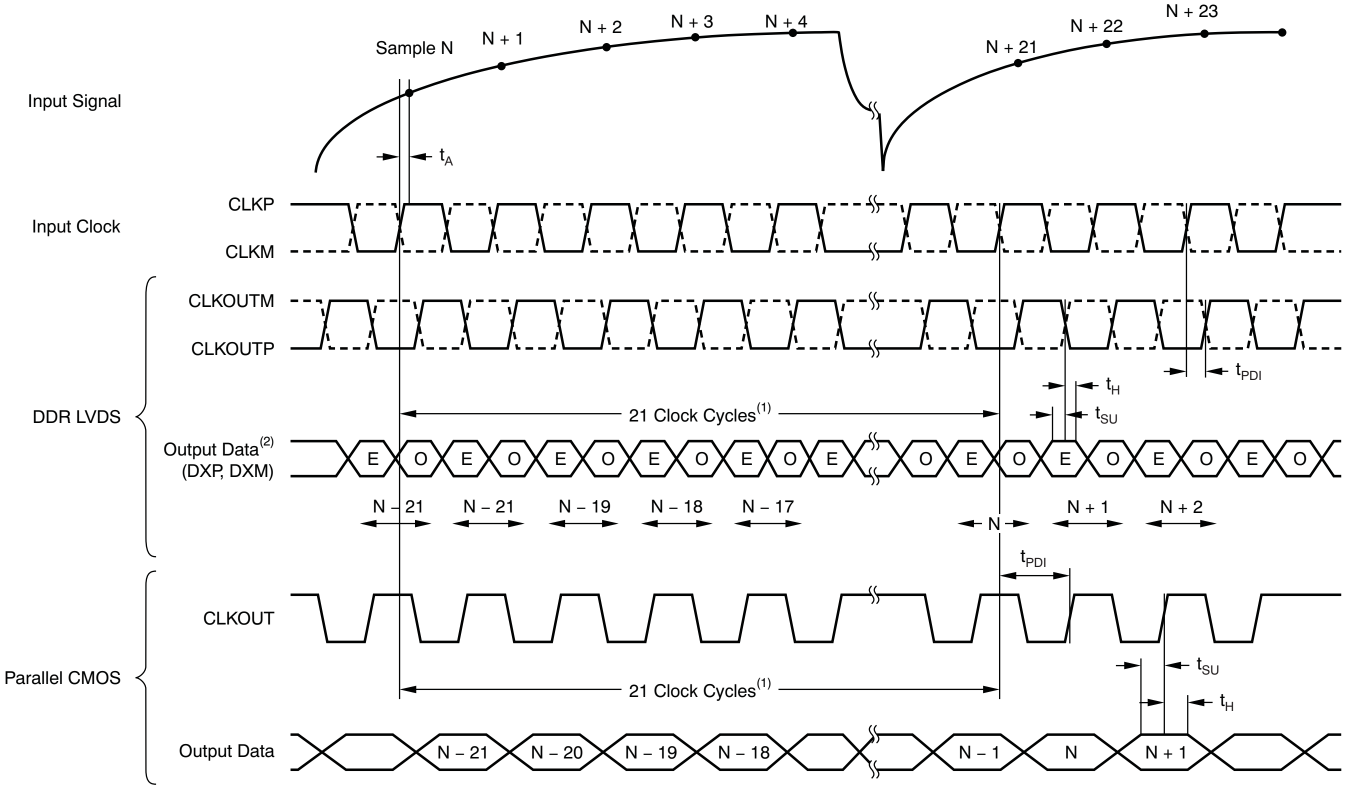
SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
230	0.85	1.25		0.35	0.6	
200	1.05	1.55		0.35	0.6	
185	1.1	1.7		0.35	0.6	
160	1.6	2.1		0.35	0.6	
125	2.3	3		0.35	0.6	
80	4.5	5.2		0.35	0.6	

Table 2. CMOS Timing Across Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO OUTPUT CLOCK								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1	1.6		2	2.8		4	5.5	7
185	1.3	2		2.2	3		4	5.5	7
160	1.8	2.5		2.5	3.3		4	5.5	7
125	2.5	3.2		3.5	4.3		4	5.5	7
80	4.8	5.5		5.7	6.5		4	5.5	7

Table 3. CMOS Timing Across Sampling Frequencies

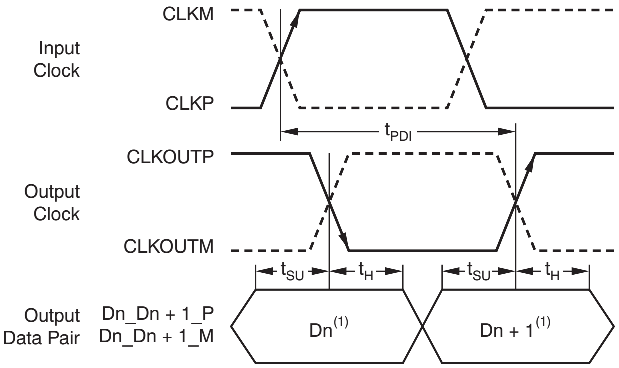
SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
250			1.6	2.5	3.2	
230			1.1	2.9	3.5	
200			0.3	3.5	4.2	
185			0	3.9	4.5	
170			–1.3	4.3	5	



(1) At higher sampling frequencies, t_{DPI} is greater than one clock cycle which then makes the overall latency = ADC latency + 1.

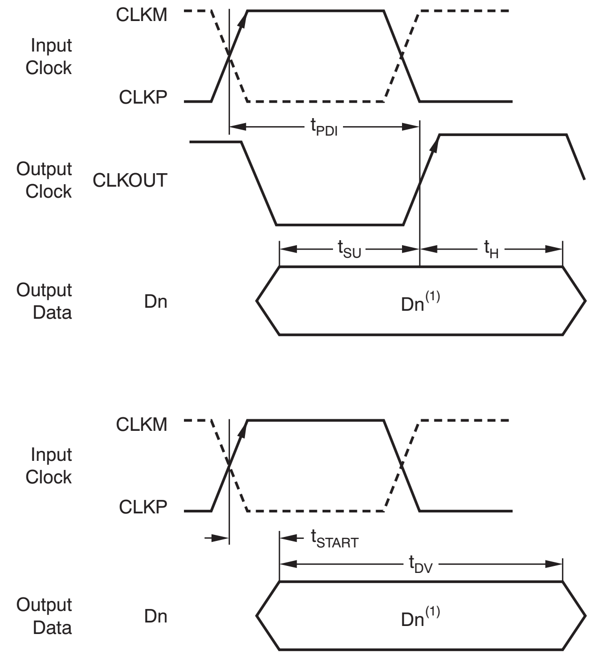
(2) E = Even bits (D0, D2, D4, etc). O = Odd bits (D1, D3, D5, etc).

Figure 5. Latency Diagram



(1) Dn = bits D0, D2, D4, etc. Dn + 1 = Bits D1, D3, D5, etc.

Figure 6. LVDS Mode Timing



Dn = bits D0, D1, D2, etc.

Figure 7. CMOS Mode Timing

DEVICE CONFIGURATION

The ADS41B29/49 have several modes that can be configured using a serial programming interface, as described in Table 4, Table 5, and Table 6. In addition, the devices have two dedicated parallel pins for quickly configuring commonly used functions. The parallel pins are DFS (analog 4-level control pin) and OE (digital control pin). The analog control pins can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 4. DFS: Analog Control Pin

VOLTAGE APPLIED ON DFS	DESCRIPTION (Data Format/Output Interface)
0, +100mV/0mV	Twos complement/DDR LVDS
(3/8) AVDD ± 100mV	Twos complement/parallel CMOS
(5/8) AVDD ± 100mV	Offset binary/parallel CMOS
AVDD, 0mV/–100mV	Offset binary/DDR LVDS

Table 5. OE: Digital Control Pin

VOLTAGE APPLIED ON OE	DESCRIPTION
0	Output data buffers disabled
AVDD	Output data buffers enabled

When the serial interface is not used, the SDATA pin can also be used as a digital control pin to place the device in standby mode. To enable this, the RESET pin must be tied high. In this mode, SEN and SCLK do not have any alternative functions. Keep SEN tied high and SCLK tied low on the board.

Table 6. SDATA: Digital Control Pin

VOLTAGE APPLIED ON SDATA	DESCRIPTION
0	Normal operation
Logic high	Device enters standby

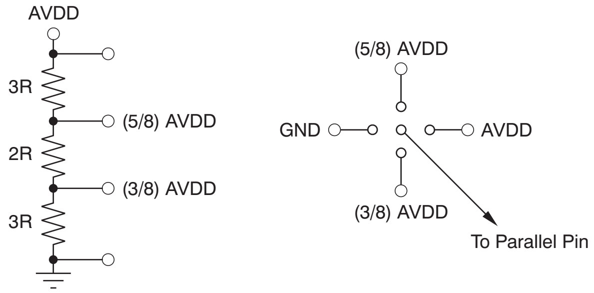


Figure 8. Simplified Diagram to Configure DFS Pin

SERIAL INTERFACE

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every falling edge of SCLK when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequency from 20MHz down to very low speeds (a few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on RESET pin (of width greater than 10ns), as shown in Figure 9; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 0x00) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

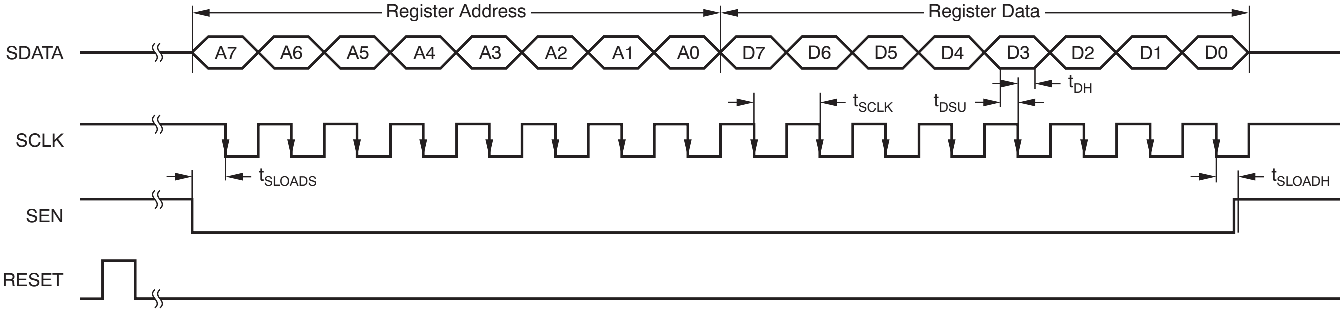


Figure 9. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at +25°C, minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V, unless otherwise noted.

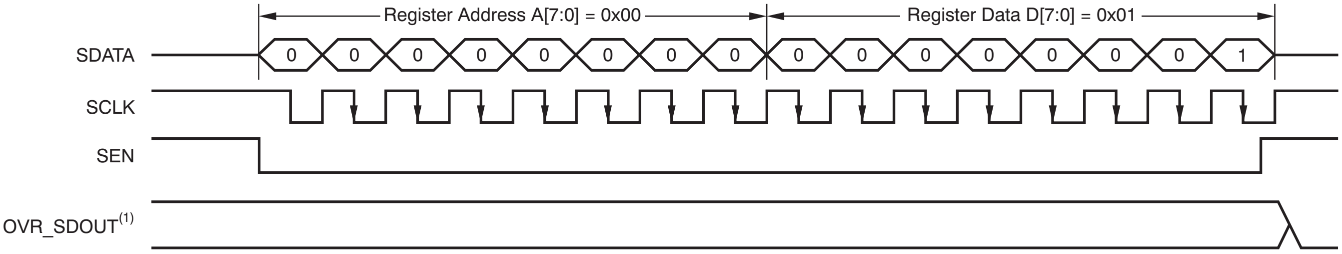
PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/t_{SCLK})	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

Serial Register Readout

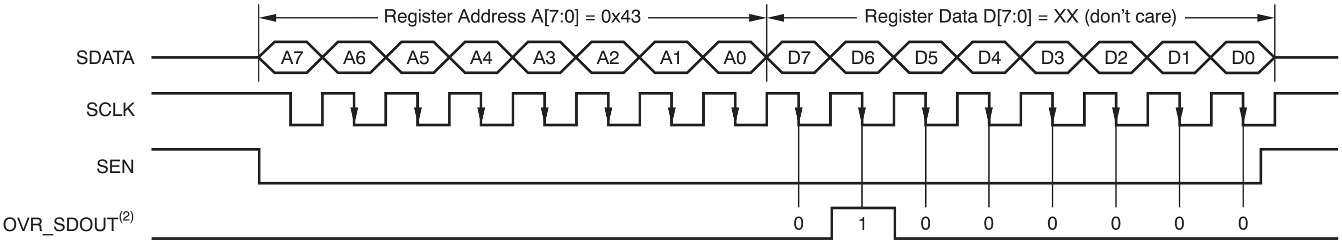
The serial register readout function allows the contents of the internal registers to be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially:

1. Set the READOUT register bit to '1'. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT = 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.



a) Enable Serial Readout (READOUT = 1)



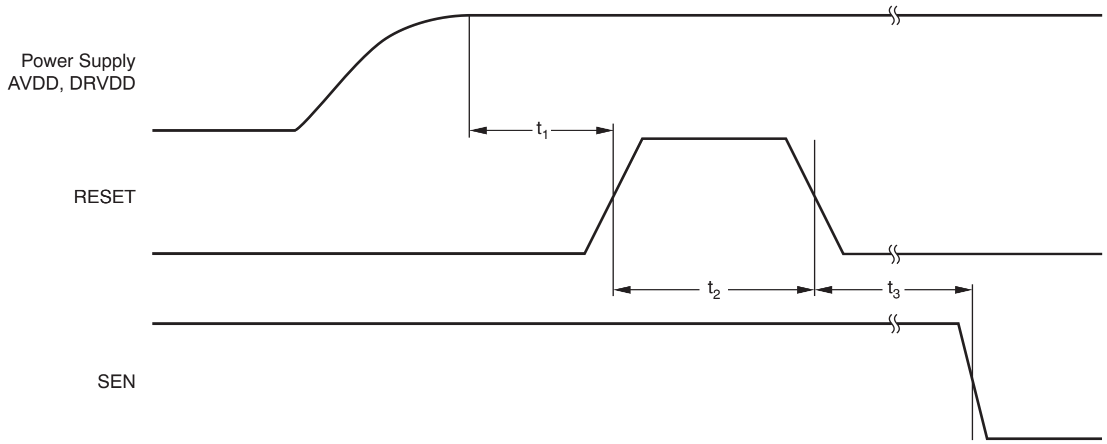
b) Read Contents of Register 0x43. This Register Has Been Initialized with 0x40 (device is put in global power-down mode).

(1) The OVR_SDOUT pin functions as OVR (READOUT = 0).

(2) The OVR_SDOUT pin functions as a serial readout (READOUT = 1).

Figure 10. Serial Readout Timing Diagram

RESET TIMING CHARACTERISTICS



NOTE: A high pulse on the RESET pin is required in the serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 11. Reset Timing Diagram

RESET TIMING REQUIREMENTS

Typical values at +25°C and minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse width	Pulse width of active RESET signal that resets the serial registers	10			ns
					1 (1)	µs
t_3		Delay from RESET disable to SEN active	100			ns

(1) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1µs, the device could enter the parallel configuration mode briefly and then return back to serial interface mode.

SERIAL REGISTER MAP

Table 7 summarizes the functions supported by the serial interface.

Table 7. Serial Interface Register Map(1)

<table>
<tr><th>REGISTER ADDRESS</th><th>DEFAULT VALUE AFTER RESET</th><th colspan="8">REGISTER DATA</th></tr>
<tr><th>A[7:0] (Hex)</th><th>D[7:0] (Hex)</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>00</td><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>RESET</td><td>READOUT</td></tr>
<tr><td>01</td><td>00</td><td colspan="6">LVDS SWING</td><td>0</td><td>0</td></tr>
<tr><td>03</td><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">HIGH PERF MODE 1</td></tr>
<tr><td>25</td><td>00</td><td colspan="4">GAIN</td><td>0</td><td colspan="3">TEST PATTERNS</td></tr>
<tr><td>26</td><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>LVDS CLKOUT STRENGTH</td><td>LVDS DATA STRENGTH</td></tr>
<tr><td>3D</td><td>00</td><td colspan="2">DATA FORMAT</td><td>EN OFFSET CORR</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3F</td><td>00</td><td>0</td><td>0</td><td colspan="6">CUSTOM PATTERN D[13:8]</td></tr>
<tr><td>40</td><td>00</td><td colspan="8">CUSTOM PATTERN D[7:0]</td></tr>
<tr><td>41</td><td>00</td><td colspan="2">LVDS CMOS</td><td colspan="2">CMOS CLKOUT STRENGTH</td><td>EN CLKOUT RISE</td><td colspan="2">CLKOUT RISE POSN</td><td>EN CLKOUT FALL</td></tr>
<tr><td>42</td><td>00</td><td colspan="2">CLKOUT FALL POSN</td><td>0</td><td>0</td><td>0</td><td>STBY</td><td>0</td><td>0</td></tr>
<tr><td>43</td><td>00</td><td>0</td><td>PDN GLOBAL</td><td>0</td><td>PDN OBUF</td><td>0</td><td>0</td><td colspan="2">EN LVDS SWING</td></tr>
<tr><td>4A</td><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>HIGH PERF MODE 2</td></tr>
<tr><td>BF</td><td>00</td><td colspan="6">OFFSET PEDESTAL</td><td>0</td><td>0</td></tr>
<tr><td>CF</td><td>00</td><td>FREEZE OFFSET CORR</td><td>0</td><td colspan="4">OFFSET CORR TIME CONSTANT</td><td>0</td><td>0</td></tr>
<tr><td>DF</td><td>00</td><td>0</td><td>0</td><td colspan="2">LOW SPEED</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

(1) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

For best performance, two special mode register bits must be enabled: HI PERF MODE 1 and HI PERF MODE 2.

Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] **Always write '0'**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the OVR_SDOUT pin functions as an over-voltage indicator.
1 = Serial readout enabled; the OVR_SDOUT pin functions as a serial data readout.

Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] LVDS SWING: LVDS swing programmability[1]

000000 = Default LVDS swing; ±350mV with external 100Ω termination
011011 = LVDS swing *increases* to ±410mV
110010 = LVDS swing *increases* to ±465mV
010100 = LVDS swing *increases* to ±570mV
111110 = LVDS swing *decreases* to ±200mV
001111 = LVDS swing *decreases* to ±125mV

Bits[1:0] Always write '0'

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HI PERF MODE 1	

Bits[7:2] Always write '0'

Bits[1:0] HI PERF MODE 1: High performance mode 1

00 = Default performance after reset
01 = Do not use
10 = Do not use
11 = For best performance across sampling clock and input signal frequencies, set the HIGH PERF MODE 1 bits

Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
GAIN				0	TEST PATTERNS		

Bits[7:4] **GAIN: Gain programmability**

These bits set the gain programmability in 0.5dB steps.

0000, 0001, 0010, 0011, 0100 = Do not use
0101 = 0dB gain (default after reset)
0110 = 0.5dB gain
0111 = 1dB gain
1000 = 1.5dB gain
1001 = 2dB gain
1010 = 2.5dB gain
1011 = 3dB gain
1100 = 3.5dB gain

Bit 3 **Always write '0'**

Bits[2:0] **TEST PATTERNS: Data capture**

These bits verify data capture.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern

In the ADS41B49, output data D[13:0] is an alternating sequence of *01010101010101* and *10101010101010*.
In the ADS41B29, output data D[11:0] is an alternating sequence of *010101010101* and *101010101010*.

100 = Outputs digital ramp

In ADS41B46, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383
In ADS41B26, output data increments by one LSB (12-bit) every 4th clock cycle from code 0 to code 4095

101 = Output custom pattern (use registers 0x3F and 0x40 for setting the custom pattern)
110 = Unused
111 = Unused

Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits[7:2] **Always write '0'**

Bit 1 **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength**

This bit determines the external termination to be used with the LVDS output clock buffer.
0 = 100Ω external termination (default strength)
1 = 50Ω external termination (2x strength)

Bit 0 **LVDS DATA STRENGTH: LVDS data buffer strength**

This bit determines the external termination to be used with all of the LVDS data buffers.
0 = 100Ω external termination (default strength)
1 = 50Ω external termination (2x strength)

Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
DATA FORMAT		EN OFFSET CORR	0	0	0	0	0

Bits[7:6] **DATA FORMAT: Data format selection**

These bits selects the data format.
00 = The DFS pin controls data format selection
10 = Twos complement
11 = Offset binary

Bit 5 **ENABLE OFFSET CORR: Offset correction setting**

This bit sets the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits[4:0] **Always write '0'**

Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

Bits[7:6] **Always write '0'**

Bits[5:0] **CUSTOM PATTERN**(1)

These bits set the custom pattern.

(1) For the ADS41B4x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS41B2x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0

Bits[7:0] **CUSTOM PATTERN**(1)

These bits set the custom pattern.

(1) For the ADS41B4x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS41B2x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL

Bits[7:6] **LVDS CMOS: Interface selection**

These bits select the interface.
00, 10 = The DFS pin controls the selection of either LVDS or CMOS interface
01 = DDR LVDS interface
11 = Parallel CMOS interface

Bits[5:4] **CMOS CLKOUT STRENGTH**

Controls strength of CMOS output clock only.
00 = Maximum strength (recommended and used for specified timings)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bit 3 **ENABLE CLKOUT RISE**

0 = Disables control of output clock rising edge
1 = Enables control of output clock rising edge

Bits[2:1] **CLKOUT RISE POSN: CLKOUT rise control**

Controls position of output clock rising edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 500ps, hold increases by 500ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200ps, hold increases by 200ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 100ps, hold increases by 100ps
10 = Setup reduces by 200ps, hold increases by 200ps
11 = Setup reduces by 1.5ns, hold increases by 1.5ns

Bit 0 **ENABLE CLKOUT FALL**

0 = Disables control of output clock fall edge
1 = Enables control of output clock fall edge

Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL POSN		0	0	0	STBY	0	0

Bits[7:6] **CLKOUT FALL POSN**

Controls position of output clock falling edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 400ps, hold increases by 400ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200ps, hold increases by 200ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Falling edge is advanced by 100ps
10 = Falling edge is advanced by 200ps
11 = Falling edge is advanced by 1.5ns

Bits[5:3] **Always write '0'**

Bit 2 **STBY: Standby mode**

This bit sets the standby mode.
0 = Normal operation
1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bits[1:0] **Always write '0'**

Register Address 43h (Default = 00h)

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 0 **Always write '0'**

Bit 6 **PDN GLOBAL: Power-down**

This bit sets the state of operation.
0 = Normal operation
1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 **Always write '0'**

Bit 4 **PDN OBUF: Power-down output buffer**

This bit set the output data and clock pins.
0 = Output data and clock pins enabled
1 = Output data and clock pins powered down and put in high- impedance state

Bits[3:2] **Always write '0'**

Bits[1:0] **EN LVDS SWING: LVDS swing control**

00 = LVDS swing control using LVDS SWING register bits is disabled
01, 10 = Do not use
11 = LVDS swing control using LVDS SWING register bits is enabled

Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HI PERF MODE 2

Bits[7:1] **Always write '0'**

Bit[0] **HI PERF MODE 2: High performance mode 2**

This bit is recommended for high input signal frequencies greater than 230MHz.
0 = Default performance after reset
1 = For best performance with high-frequency input signals, set the HIGH PERF MODE 2 bit

Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
OFFSET PEDESTAL						0	0

Bits[7:2] **OFFSET PEDESTAL**

These bits set the offset pedestal.
When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

ADS414x VALUE	PEDESTAL
011111	31LSB
011110	30LSB
011101	29LSB
—	—
000000	0LSB
—	—
111111	–1LSB
111110	–2LSB
—	—
100000	–32LSB

Bits[1:0] **Always write '0'**

Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 **FREEZE OFFSET CORR**

This bit sets the freeze offset correction.
0 = Estimation of offset correction is not frozen (bit EN OFFSET CORR must be set)
1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle; see the *OFFSET CORRECTION* section.

Bit 6 **Always write '0'**

Bits[5:2] **OFFSET CORR TIME CONSTANT**

These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

VALUE	TIME CONSTANT (Number of Clock Cycles)
0000	1M
0001	2M
0010	4M
0011	8M
0100	16M
0101	32M
0110	64M
0111	128M
1000	256M
1001	512M
1010	1G
1011	2G

Bits[1:0] **Always write '0'**

Register Address DFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	LOW SPEED		0	0	0	0

Bits[7:6] **Always write '0'**

Bits[5:4] **LOW SPEED: Low-speed mode**

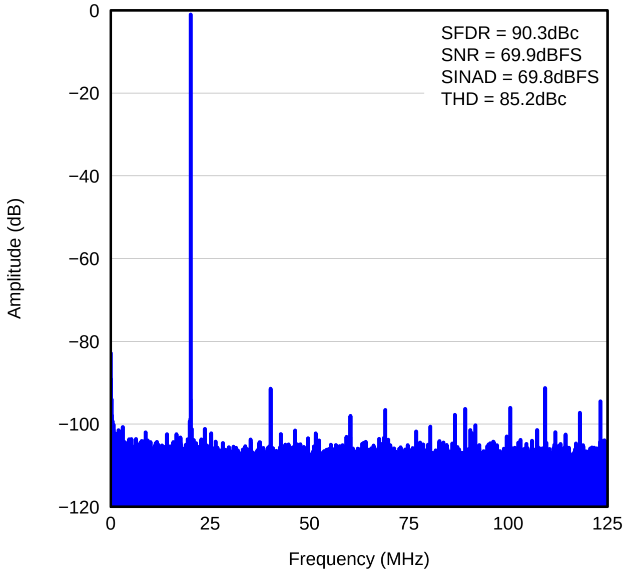
00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80MSPS.
11 = Low-speed mode enabled; this setting is recommended for sampling rates less than or equal to 80MSPS.

Bits[3:0] **Always write '0'**

TYPICAL CHARACTERISTICS: ADS41B49

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

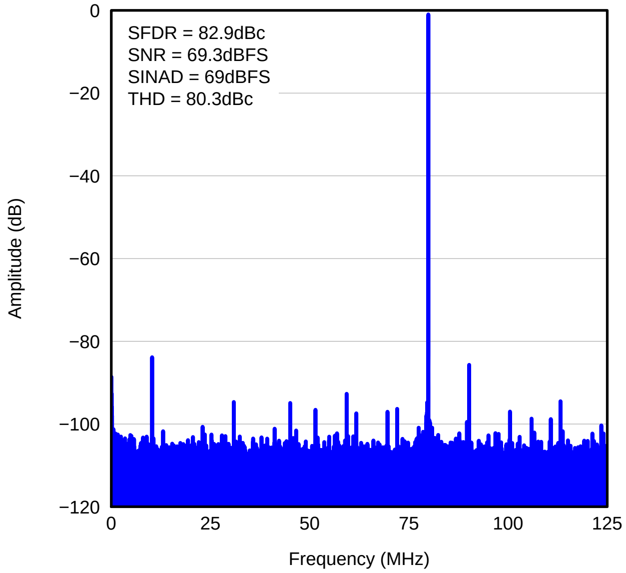
FFT FOR 20MHz INPUT SIGNAL



SFDR = 90.3dBc
SNR = 69.9dBFS
SINAD = 69.8dBFS
THD = 85.2dBc

Figure 12.

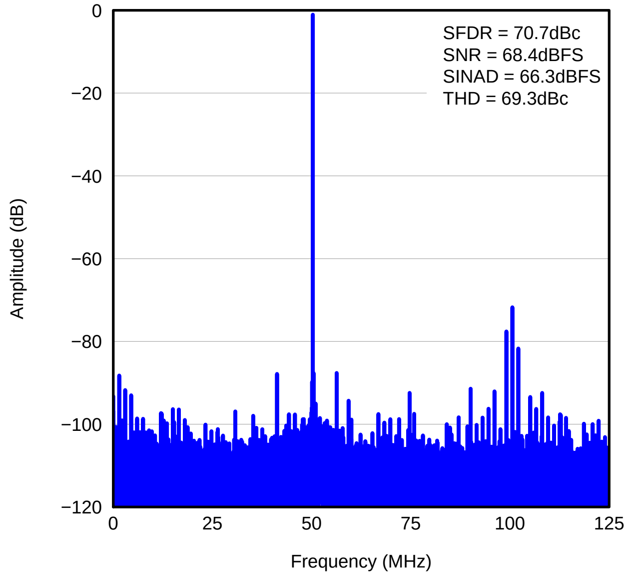
FFT FOR 170MHz INPUT SIGNAL



SFDR = 82.9dBc
SNR = 69.3dBFS
SINAD = 69dBFS
THD = 80.3dBc

Figure 13.

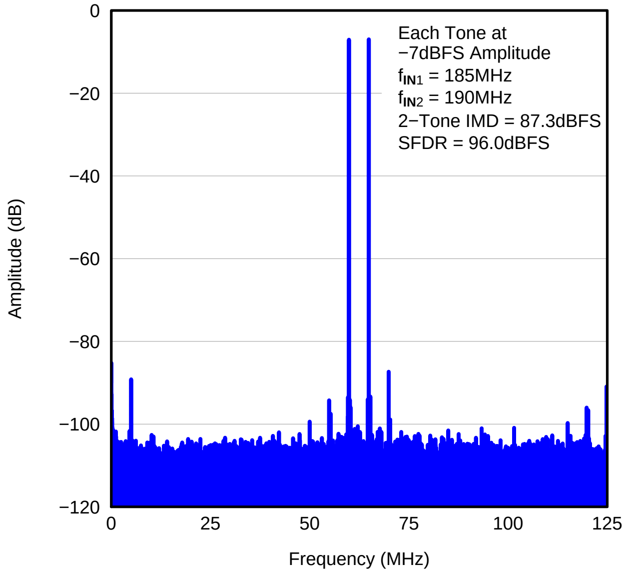
FFT FOR 300MHz INPUT SIGNAL



SFDR = 70.7dBc
SNR = 68.4dBFS
SINAD = 66.3dBFS
THD = 69.3dBc

Figure 14.

FFT FOR TWO-TONE INPUT SIGNAL



Each Tone at
−7dBFS Amplitude
f_{IN1} = 185MHz
f_{IN2} = 190MHz
2−Tone IMD = 87.3dBFS
SFDR = 96.0dBFS

Figure 15.

TYPICAL CHARACTERISTICS: ADS41B49 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR TWO-TONE INPUT SIGNAL

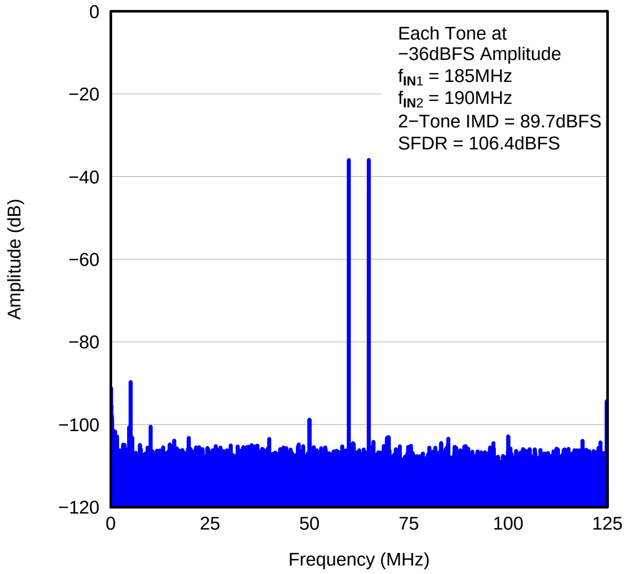


Figure 16.

SFDR vs INPUT FREQUENCY

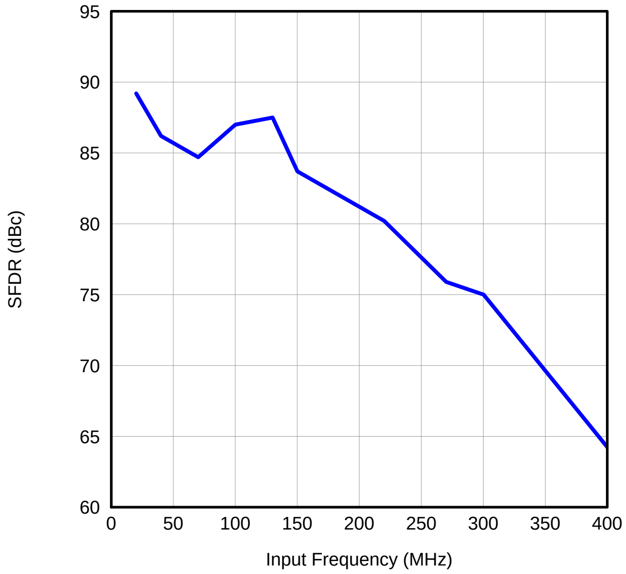


Figure 17.

SNR vs INPUT FREQUENCY

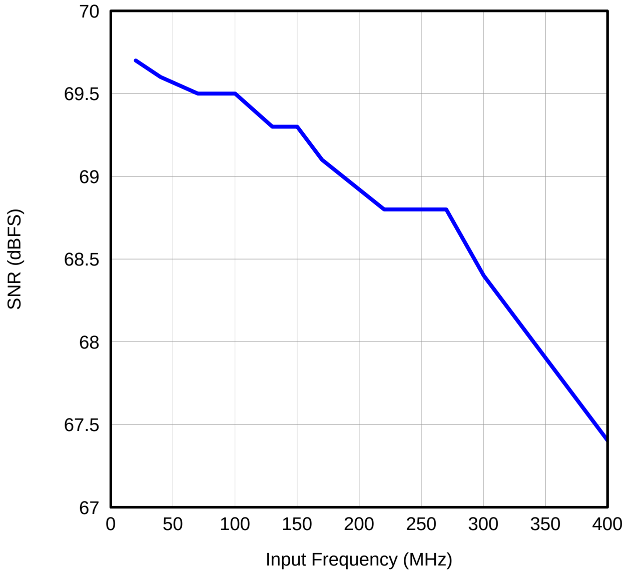


Figure 18.

SFDR ACROSS GAIN AND INPUT FREQUENCY

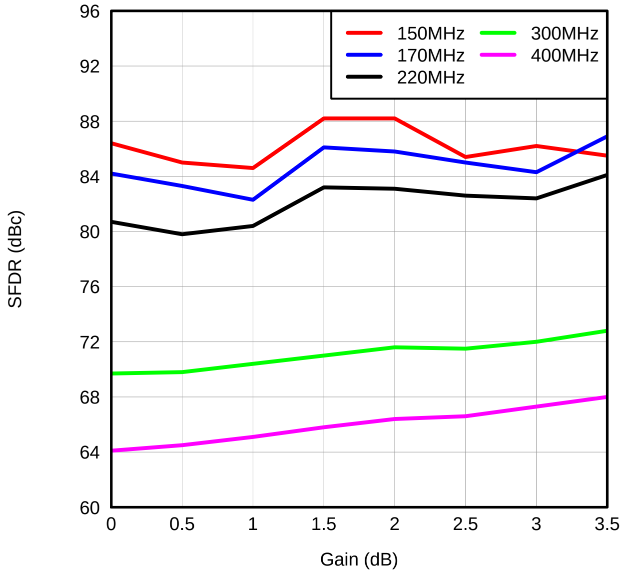


Figure 19.

TYPICAL CHARACTERISTICS: ADS41B49 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SINAD ACROSS GAIN AND INPUT FREQUENCY

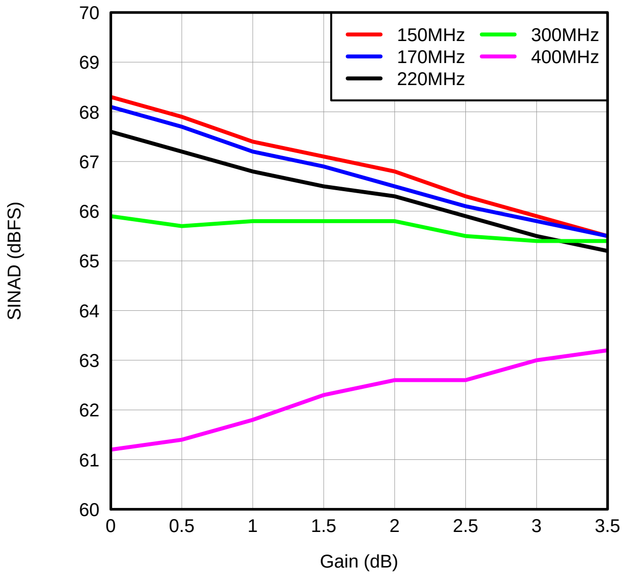


Figure 20.

PERFORMANCE ACROSS INPUT AMPLITUDE (Single Tone)

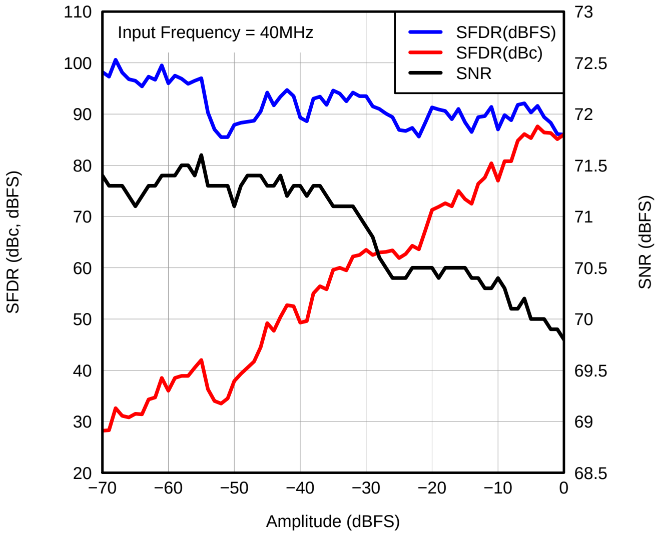


Figure 21.

PERFORMANCE ACROSS INPUT AMPLITUDE (Single Tone)

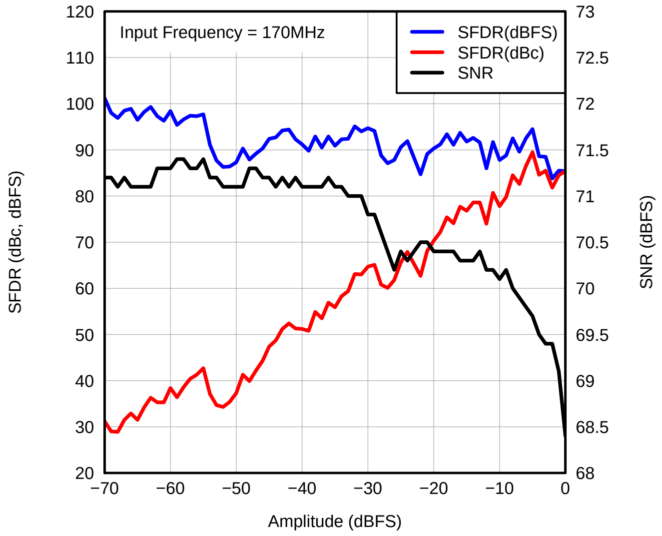


Figure 22.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

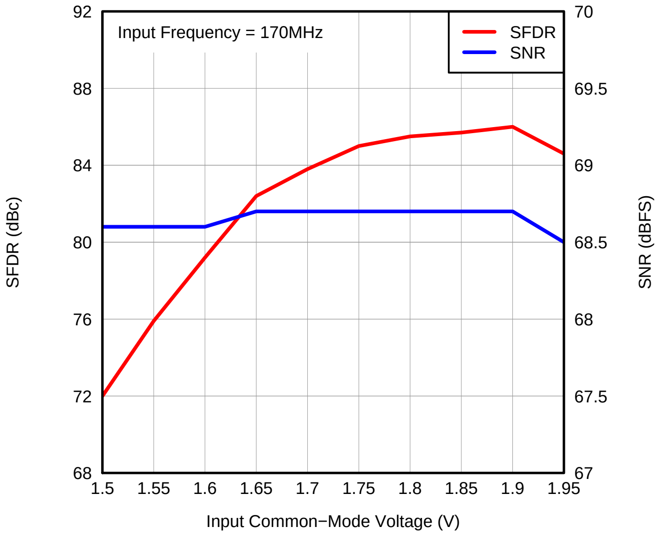


Figure 23.

TYPICAL CHARACTERISTICS: ADS41B49 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR ACROSS TEMPERATURE vs AVDD SUPPLY

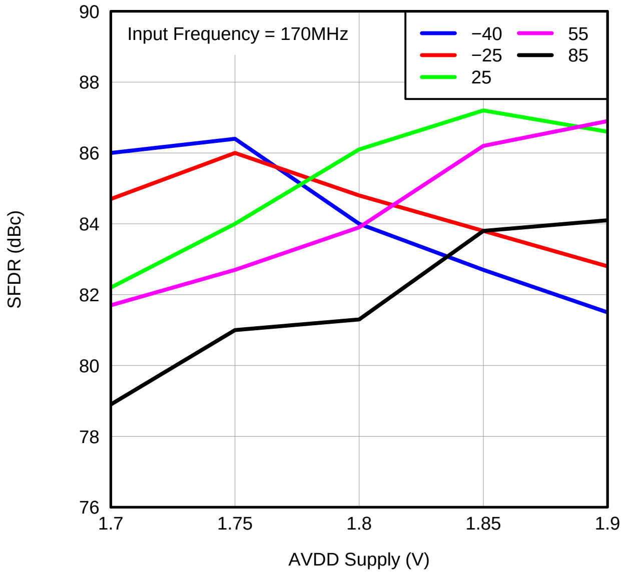


Figure 24.

SNR ACROSS TEMPERATURE vs AVDD SUPPLY

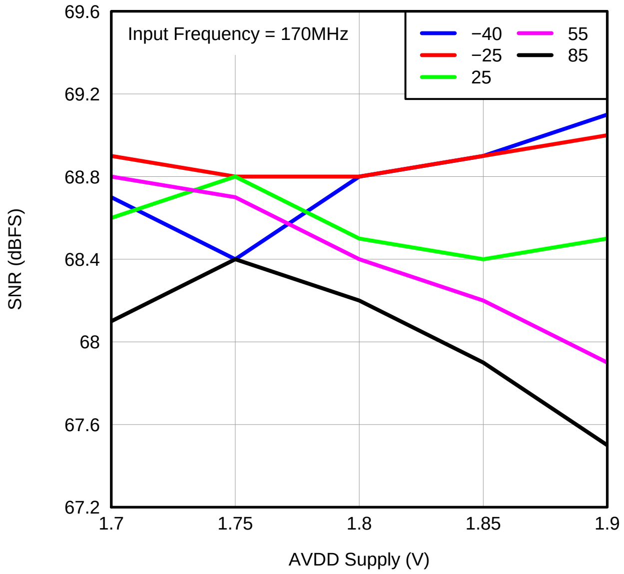


Figure 25.

PERFORMANCE ACROSS DRVDD SUPPLY VOLTAGE

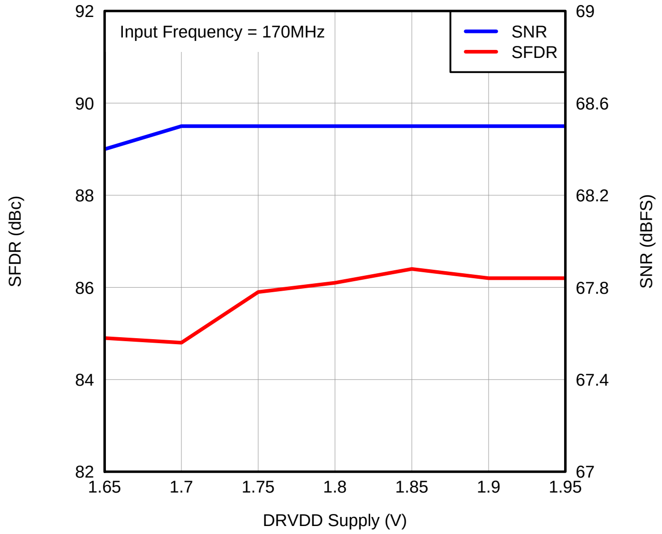


Figure 26.

PERFORMANCE ACROSS INPUT CLOCK AMPLITUDE

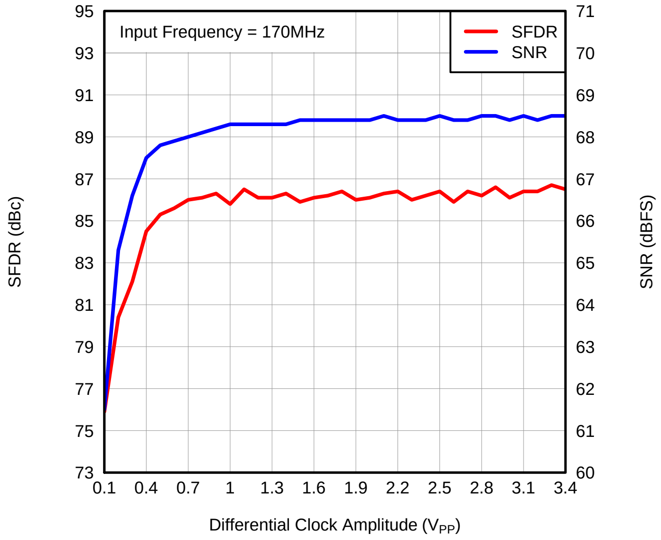


Figure 27.

TYPICAL CHARACTERISTICS: ADS41B49 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

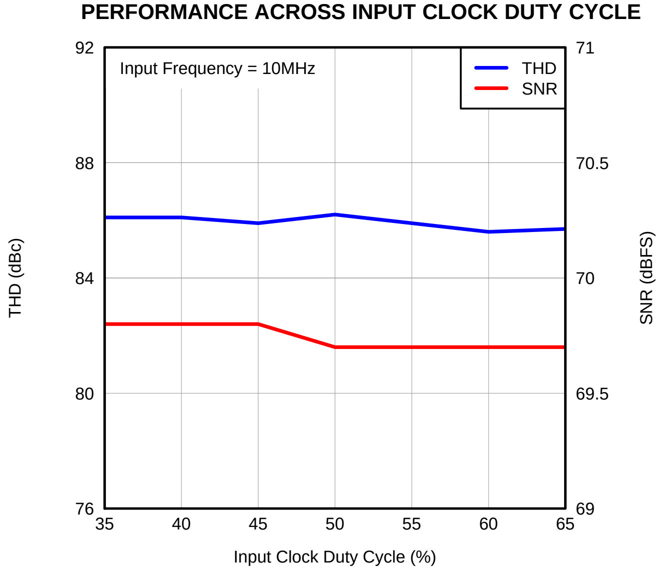


Figure 28.

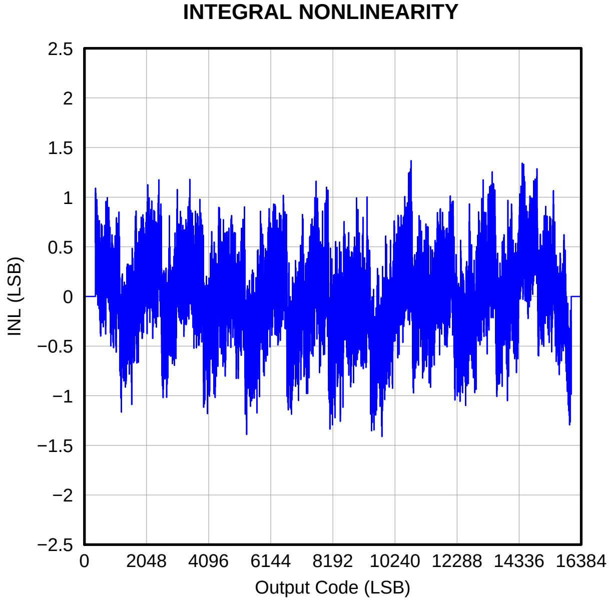


Figure 29.

TYPICAL CHARACTERISTICS: ADS41B29

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR 20MHz INPUT SIGNAL

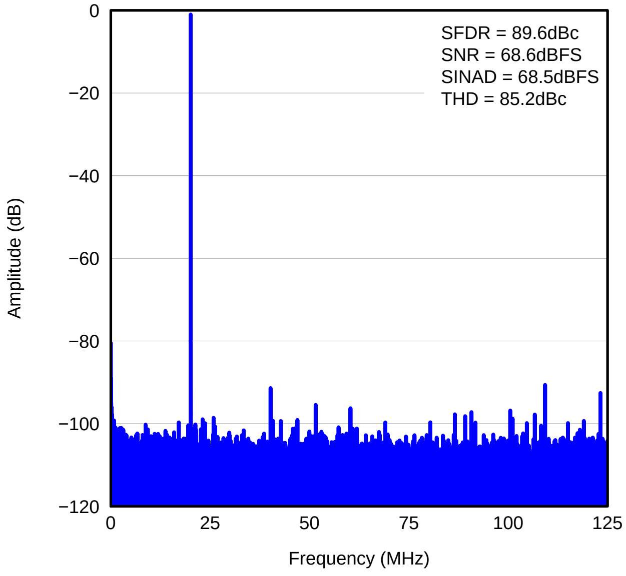


Figure 30.

FFT FOR 170MHz INPUT SIGNAL

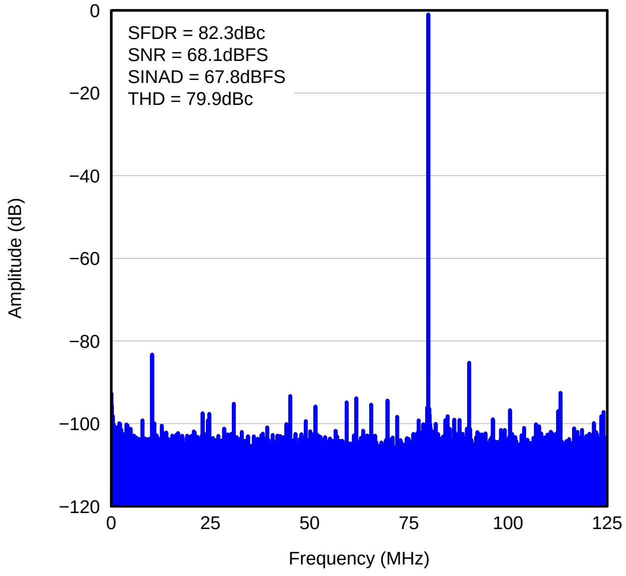


Figure 31.

FFT FOR 300MHz INPUT SIGNAL

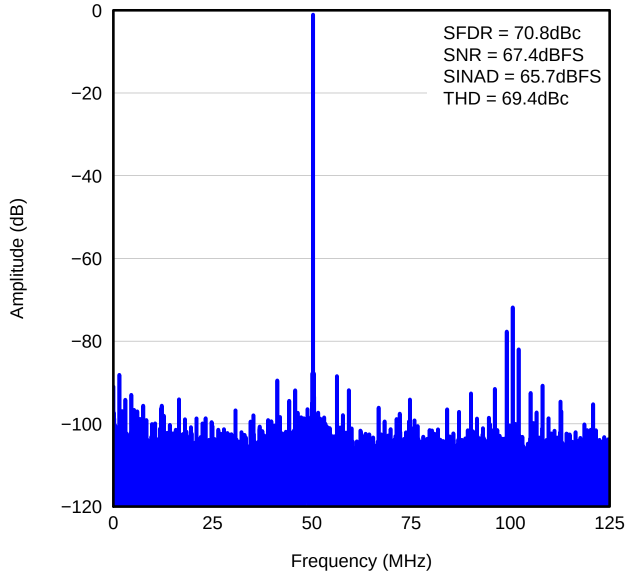


Figure 32.

FFT FOR TWO-TONE INPUT SIGNAL

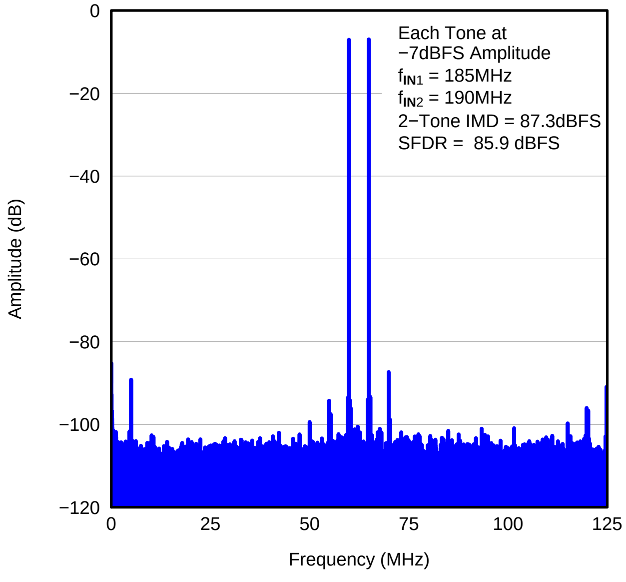


Figure 33.

TYPICAL CHARACTERISTICS: ADS41B29 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR TWO-TONE INPUT SIGNAL

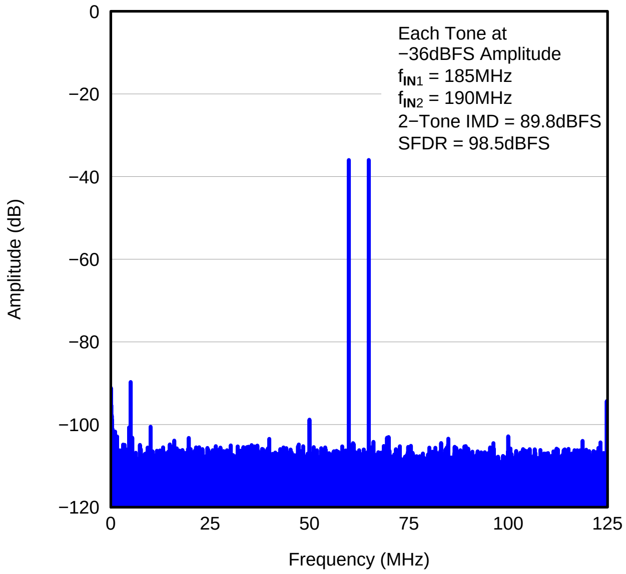


Figure 34.

SFDR vs INPUT FREQUENCY

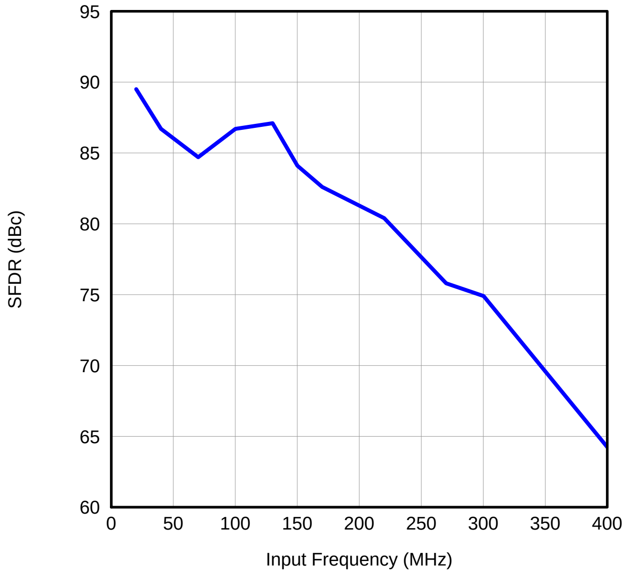


Figure 35.

SNR vs INPUT FREQUENCY

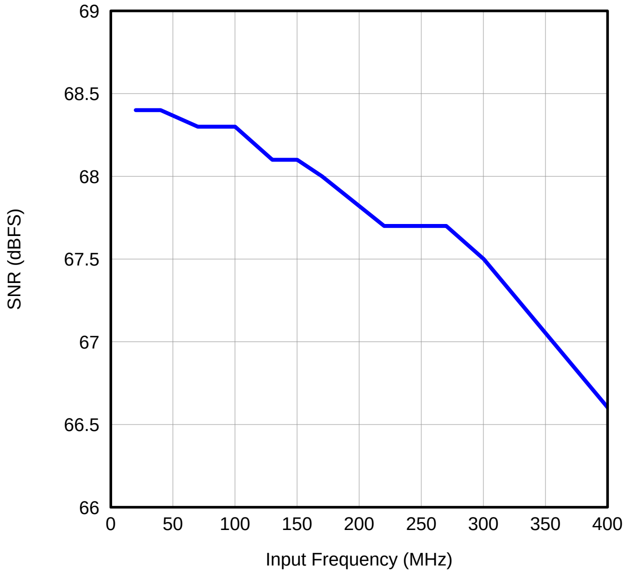


Figure 36.

SFDR ACROSS GAIN AND INPUT FREQUENCY

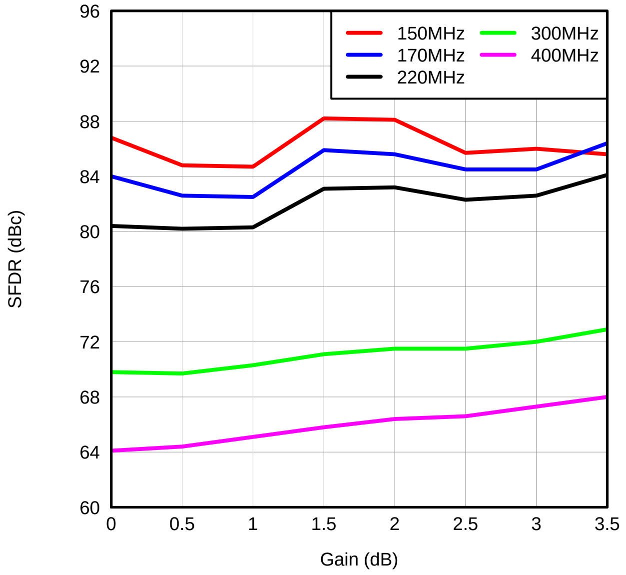


Figure 37.

TYPICAL CHARACTERISTICS: ADS41B29 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SINAD ACROSS GAIN AND INPUT FREQUENCY

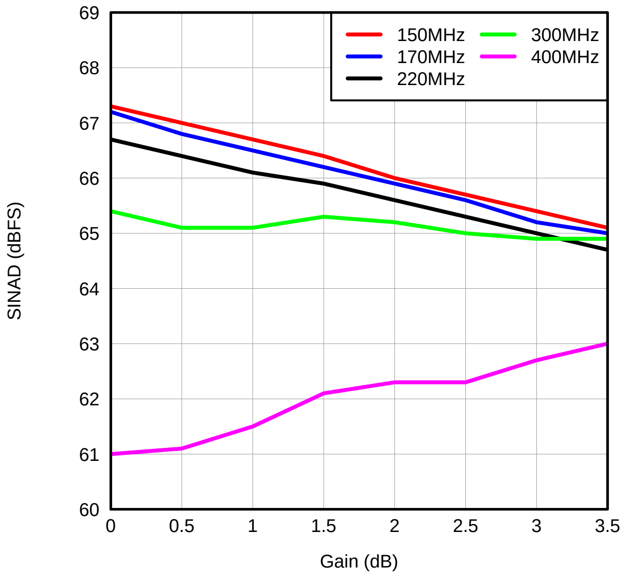


Figure 38.

PERFORMANCE ACROSS INPUT AMPLITUDE (Single Tone)

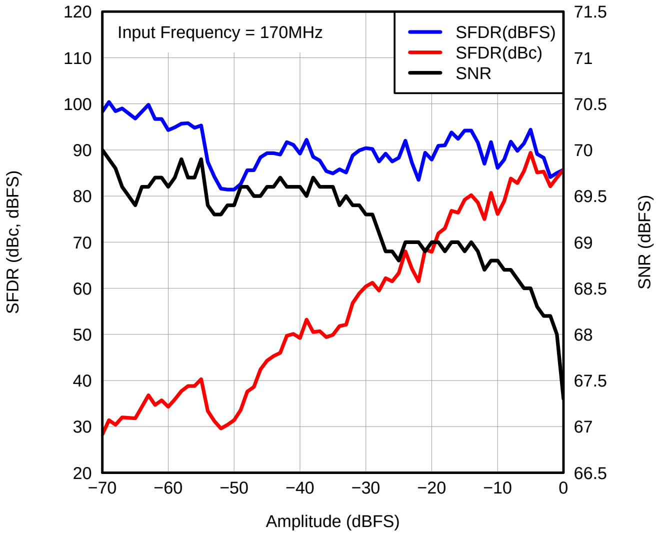


Figure 39.

PERFORMANCE ACROSS INPUT AMPLITUDE (Single Tone)

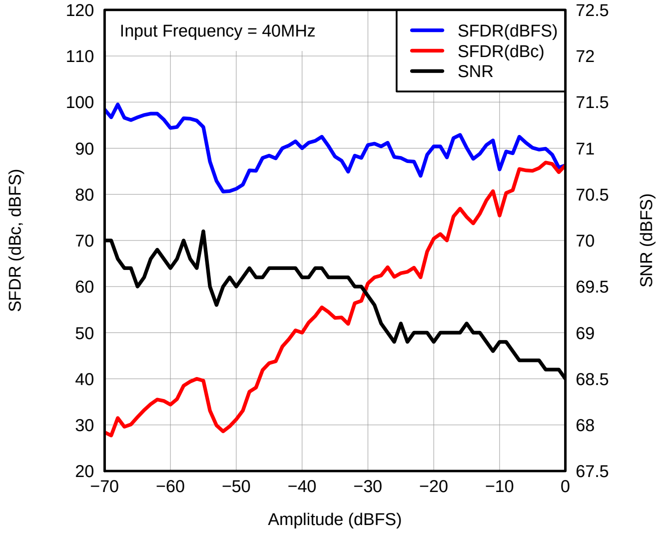


Figure 40.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

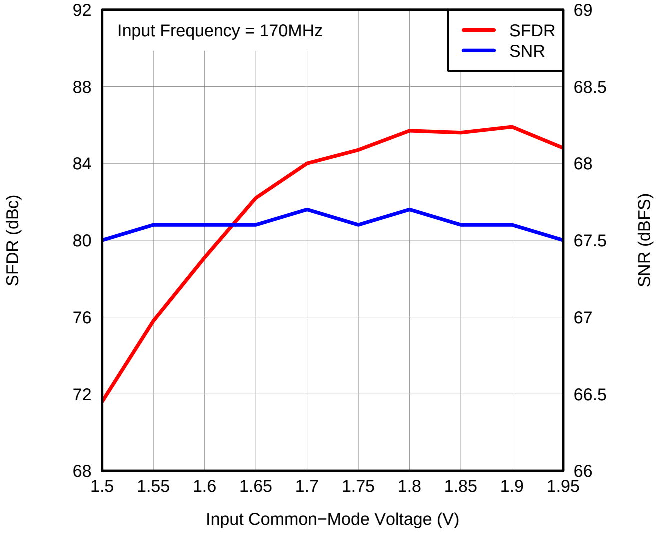


Figure 41.

TYPICAL CHARACTERISTICS: ADS41B29 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR ACROSS TEMPERATURE vs AVDD SUPPLY

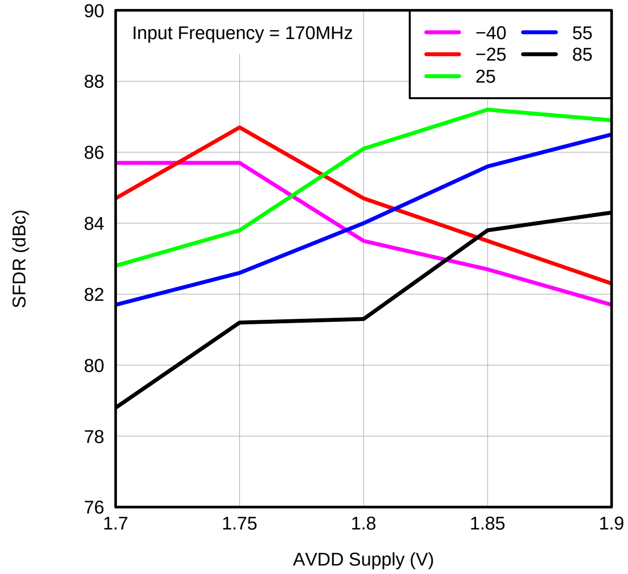


Figure 42.

SNR ACROSS TEMPERATURE vs AVDD SUPPLY

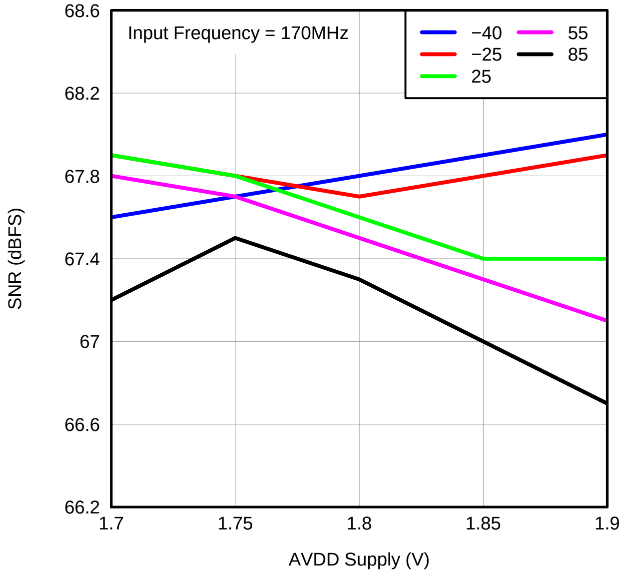


Figure 43.

PERFORMANCE ACROSS DRVDD SUPPLY VOLTAGE

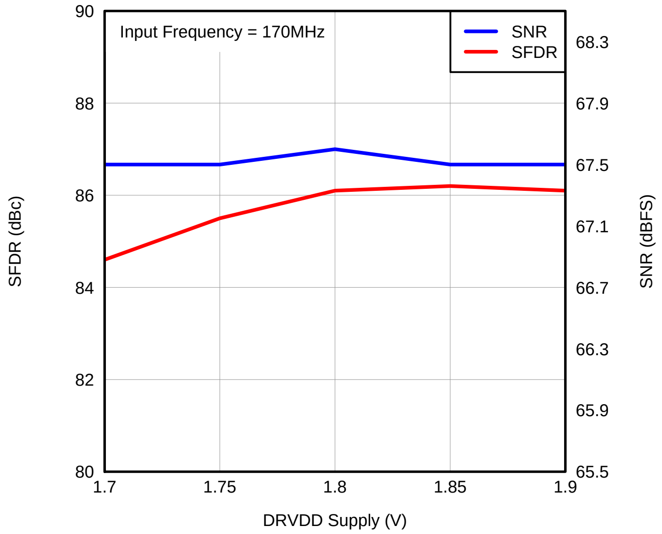


Figure 44.

PERFORMANCE ACROSS INPUT CLOCK AMPLITUDE

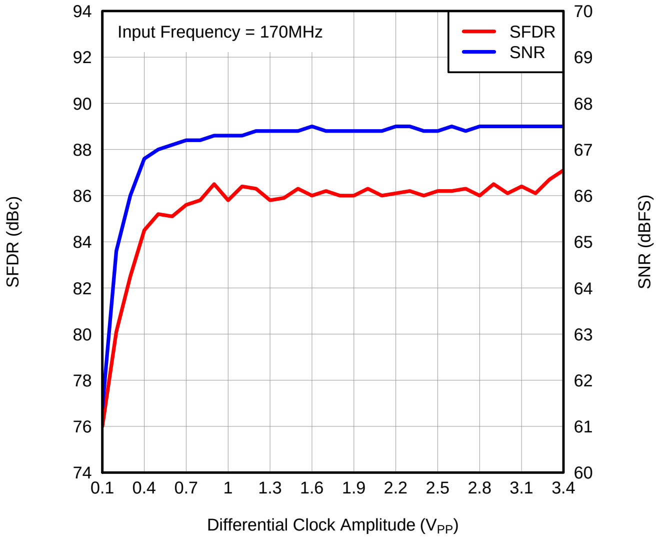


Figure 45.

TYPICAL CHARACTERISTICS: ADS41B29 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE ACROSS INPUT CLOCK DUTY CYCLE

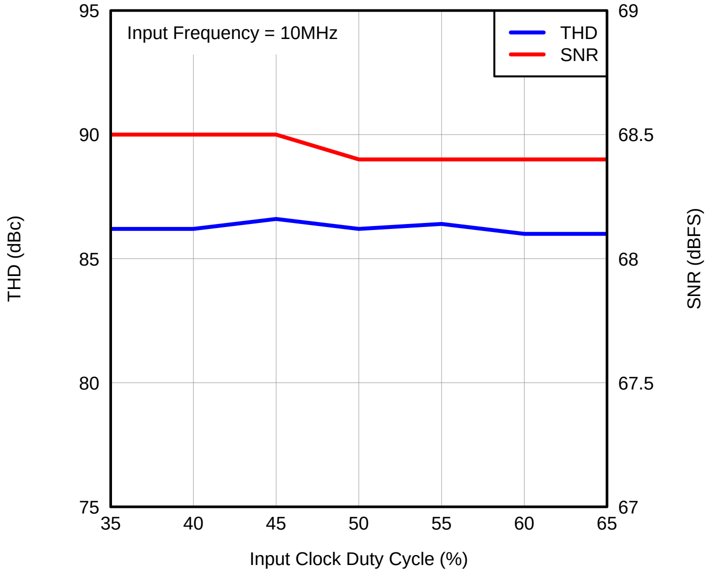


Figure 46.

TYPICAL CHARACTERISTICS: GENERAL

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

CMRR ACROSS FREQUENCY

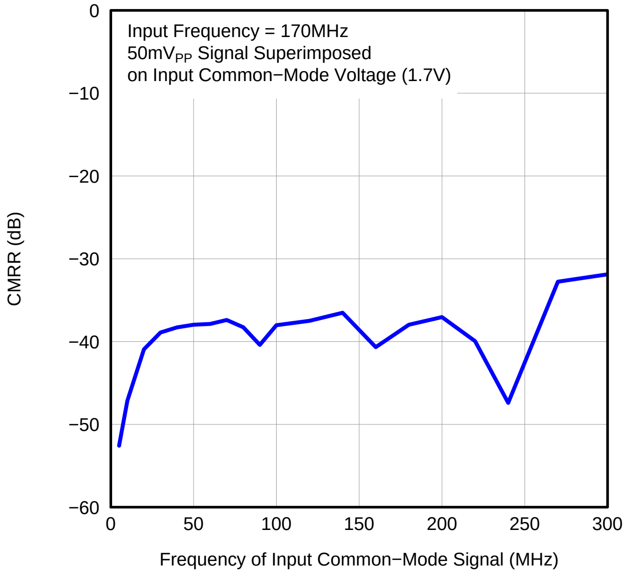


Figure 47.

CMRR FFT

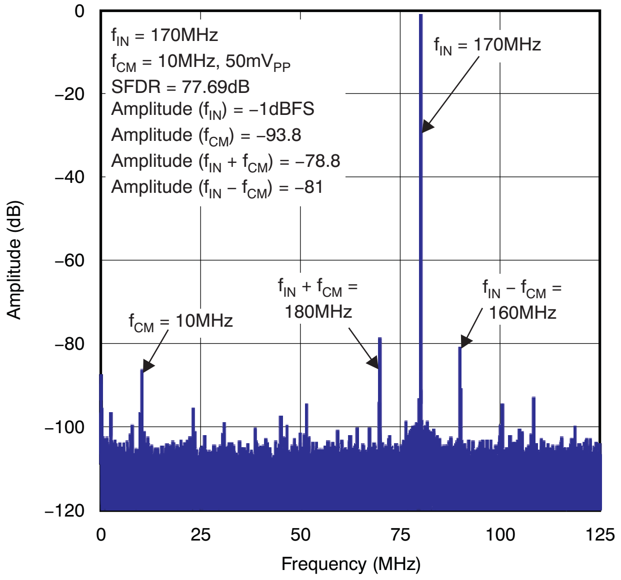


Figure 48.

PSRR ACROSS FREQUENCY

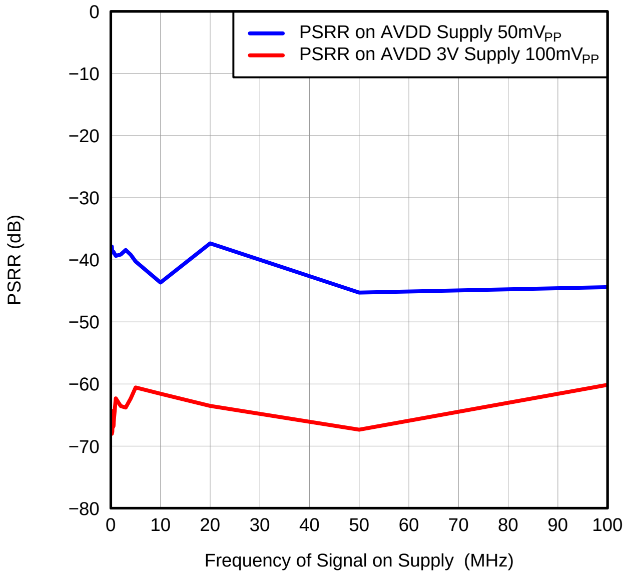


Figure 49.

PSRR FFT

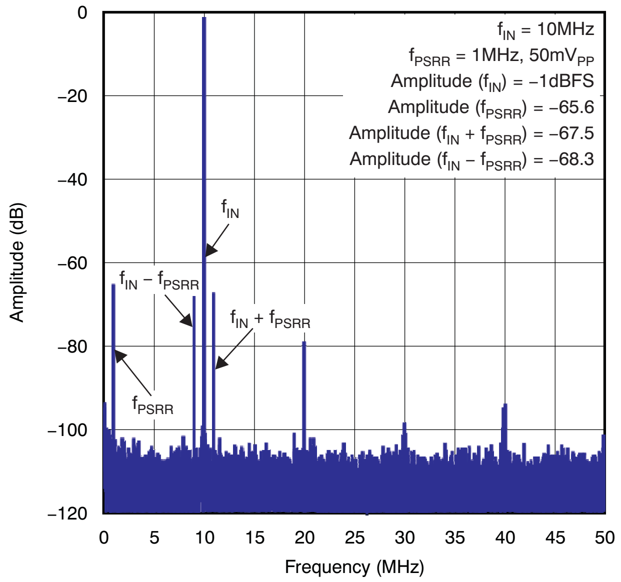


Figure 50.

TYPICAL CHARACTERISTICS: GENERAL (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

POWER ACROSS SAMPLING FREQUENCY

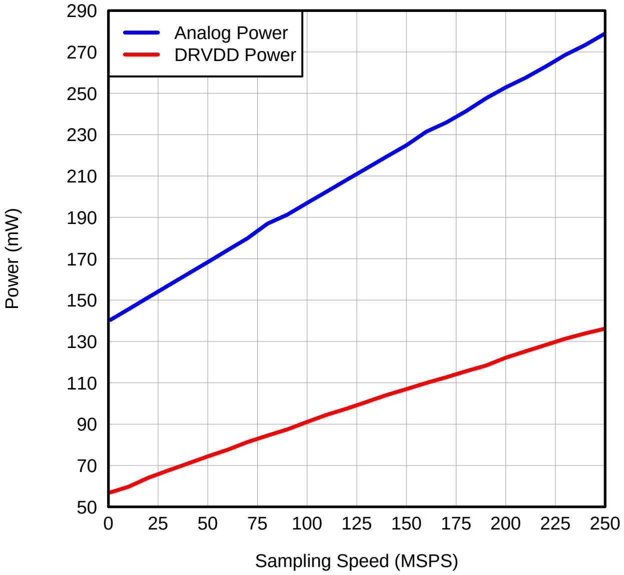


Figure 51.

DRVDD CURRENT ACROSS SAMPLING FREQUENCY

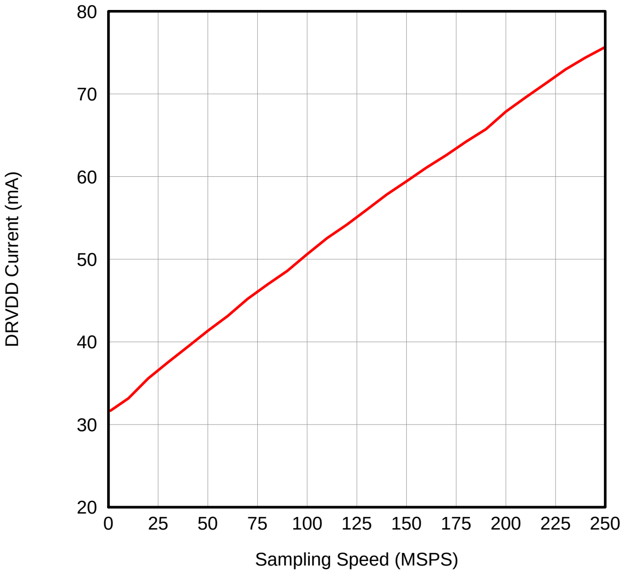


Figure 52.

TYPICAL CHARACTERISTICS: CONTOUR

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR CONTOUR
(0dB Gain, Applies to ADS41B29/B49)

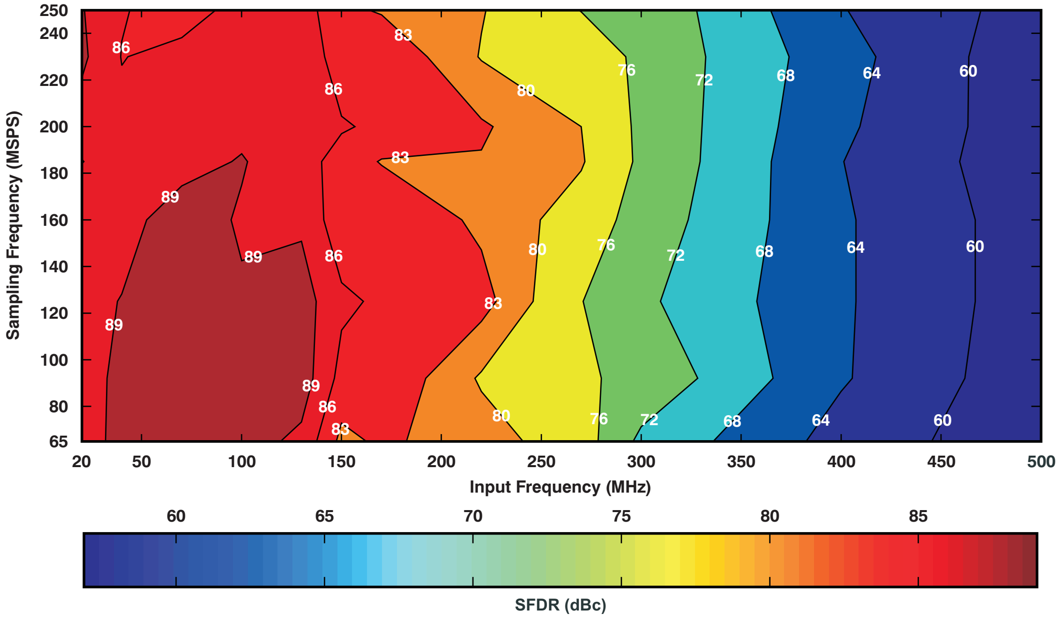


Figure 53.

SFDR CONTOUR
(3.5dB Gain, Applies to ADS41B29/B49)

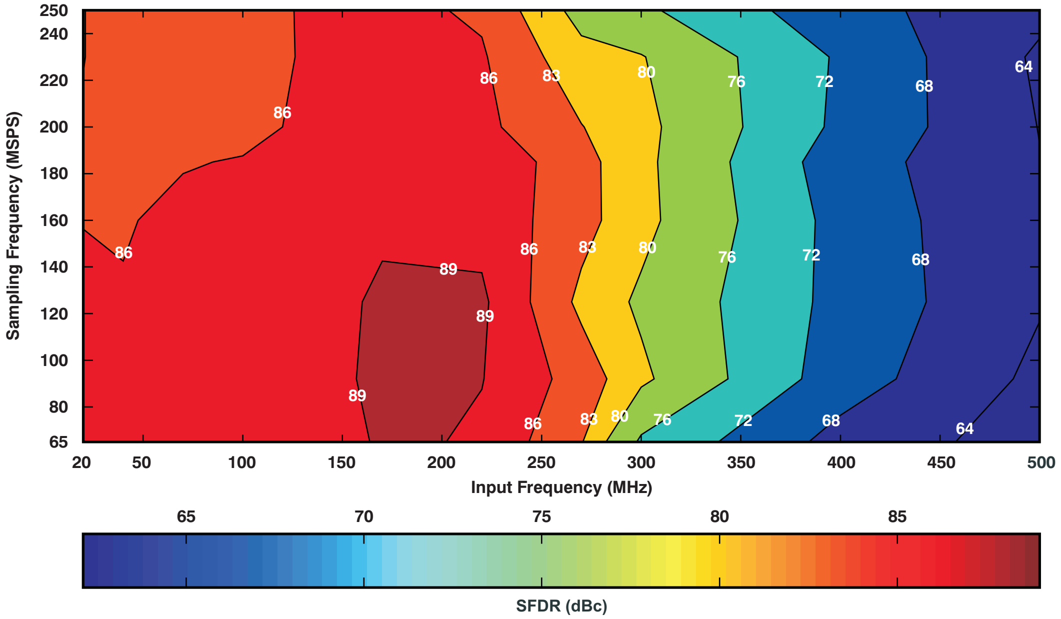


Figure 54.

TYPICAL CHARACTERISTICS: CONTOUR (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

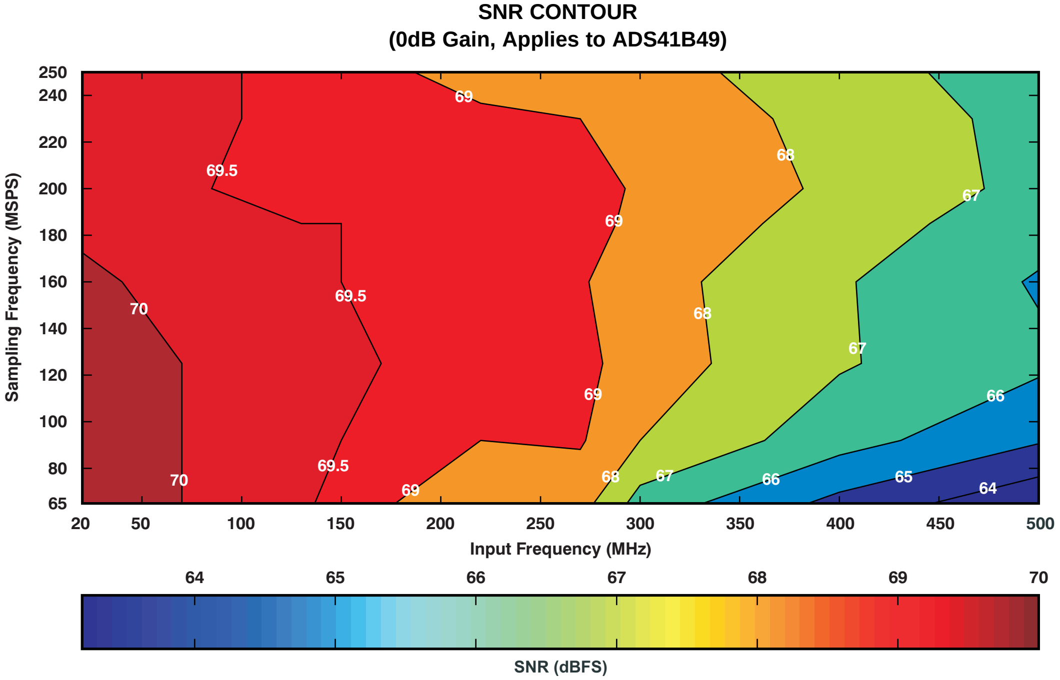


Figure 55.

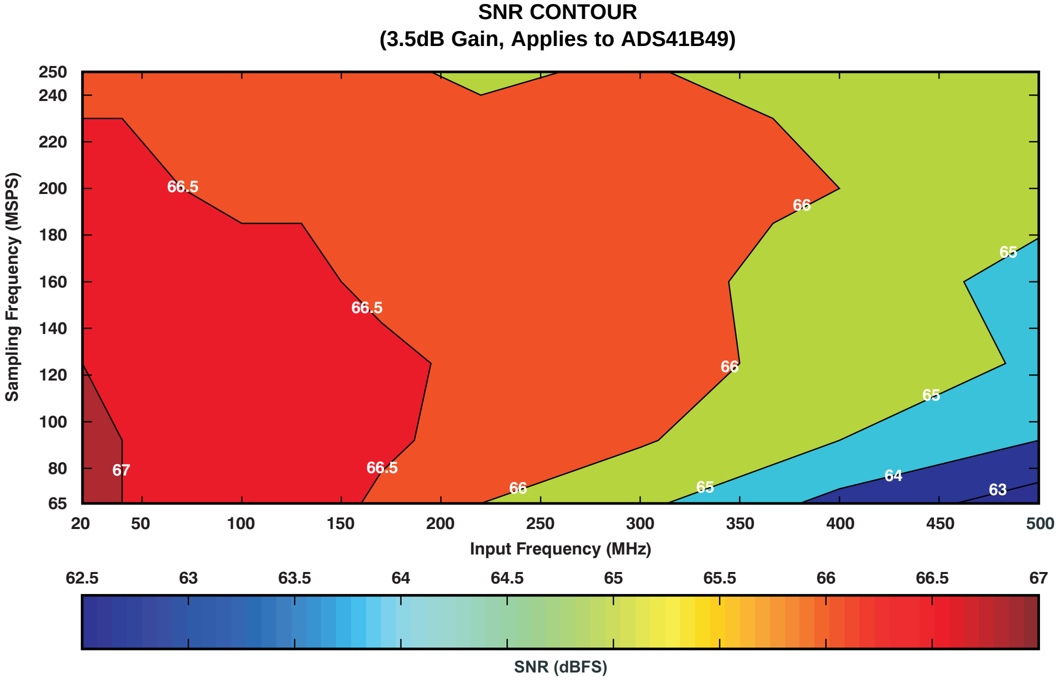


Figure 56.

TYPICAL CHARACTERISTICS: CONTOUR (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

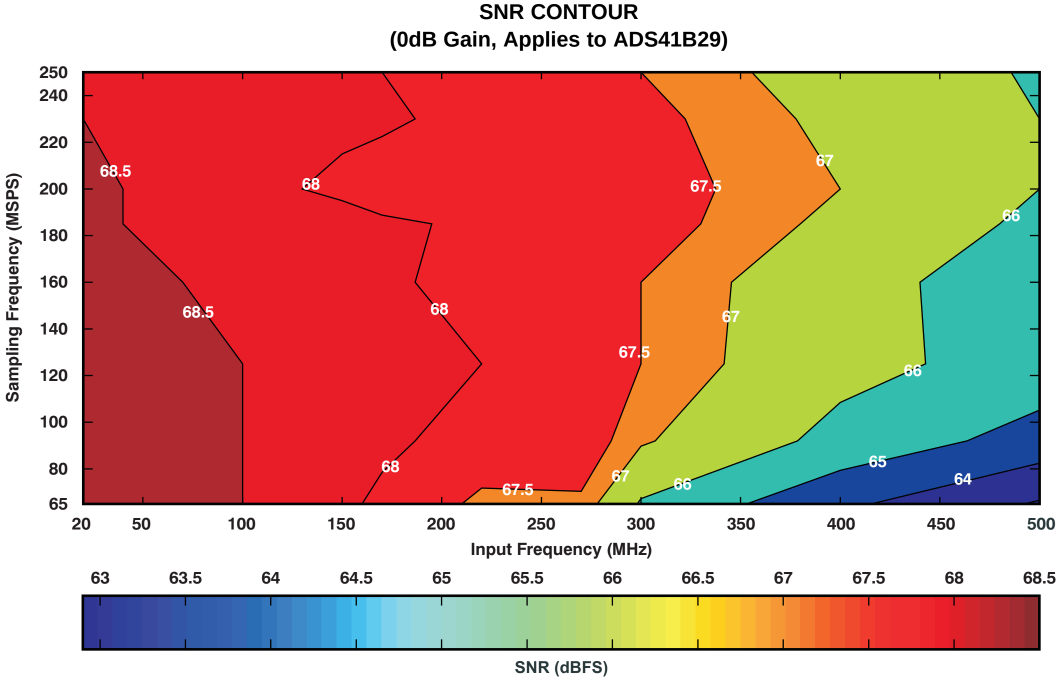


Figure 57.

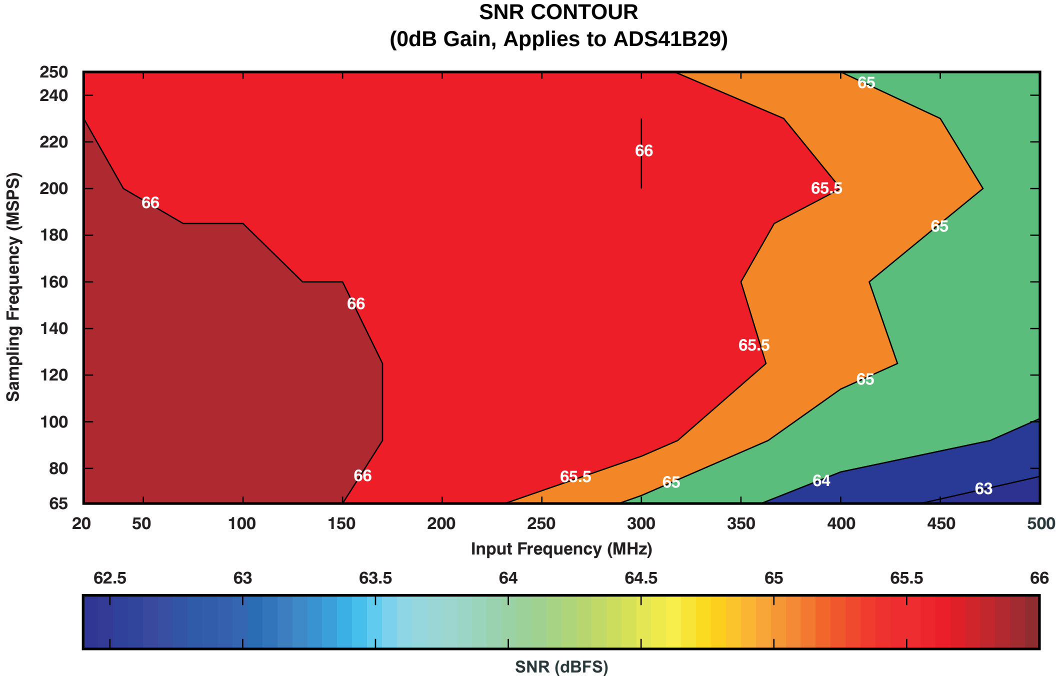


Figure 58.

APPLICATION INFORMATION

THEORY OF OPERATION

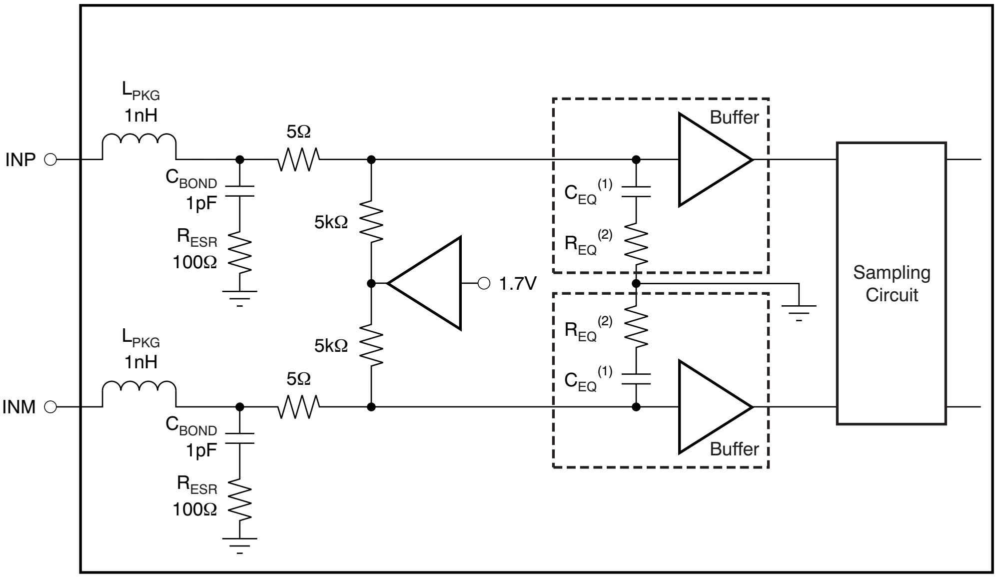
The ADS41B49/29 is a family of buffered analog input and ultralow power ADCs with maximum sampling rates up to 250MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 21 clock cycles. The output is available as 14-bit data or 12-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

ANALOG INPUT

The analog input pins have analog buffers (running off the AVDD_BUF supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10kΩ dc resistance and 2pF input capacitance). The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. This buffering makes it easy to drive the buffered inputs compared to an ADC without the buffer.

The input common-mode is set internally using a 5kΩ resistor from each input pin to 1.7V, so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.375V) and (VCM – 0.375V), resulting in a 1.5V_{PP} differential input swing.

The input sampling circuit has a high 3dB bandwidth that extends up to 800MHz (measured from the input pins to the sampled voltage). Figure 59 shows an equivalent circuit for the analog input.



(1) C_{EQ} refers to the equivalent input capacitance of the buffer = 3pF.

(2) R_{EQ} refers to the R_{EQ} buffer = 10Ω.

Figure 59. Analog Input Equivalent Circuit

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5Ω to 10Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 60 and Figure 61 show the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) seen by looking into the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1GHz.

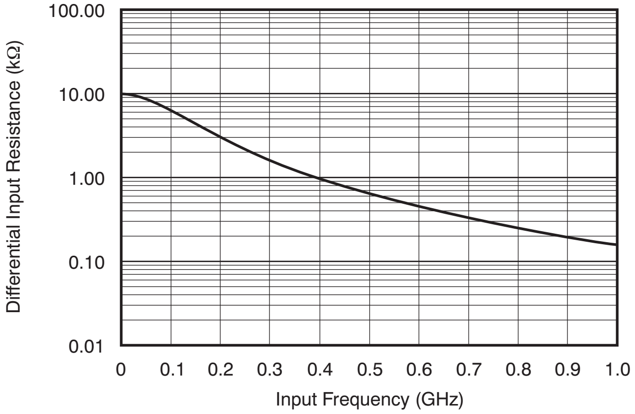


Figure 60. ADC Analog Input Resistance (R_{IN}) Across Frequency

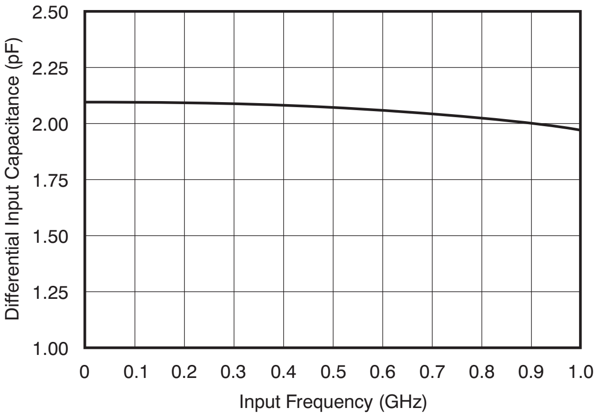


Figure 61. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 62 and Figure 63—one optimized for low input frequencies and the other optimized for high input frequencies. Notice in both cases that the board circuitry is simplified compared to the non-buffered ADS4149.

In Figure 62, a single transformer is used and is suited for low input frequencies. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended (see Figure 63). Note that both drive circuits have been terminated by 50Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

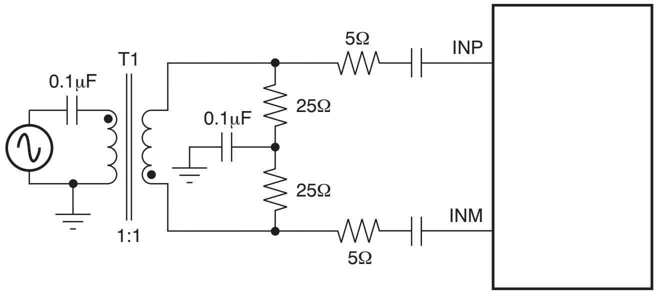


Figure 62. Drive Circuit for Low Input Frequencies

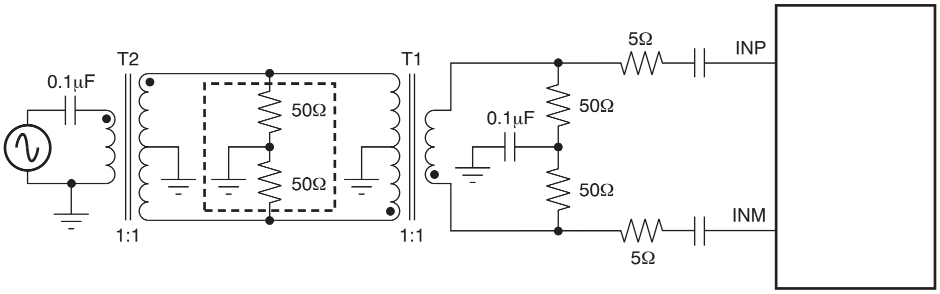
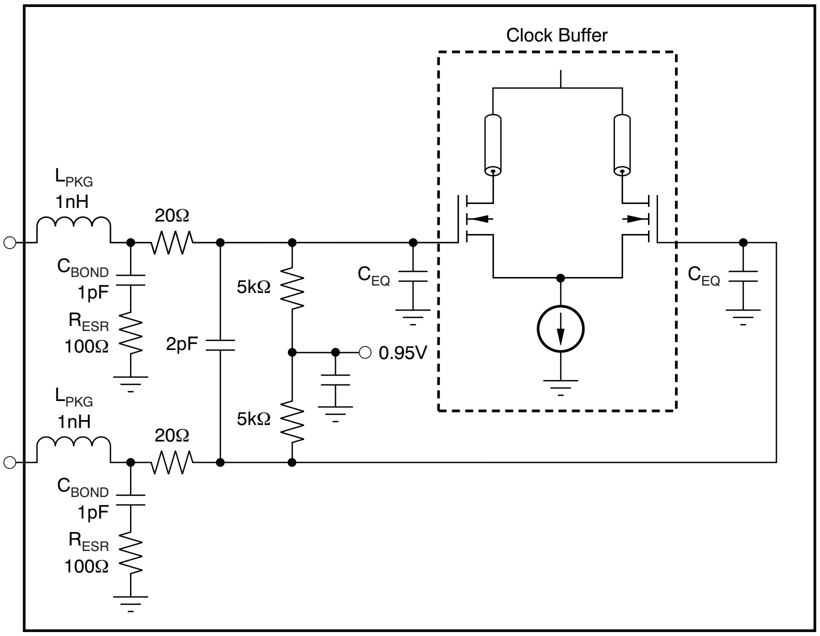


Figure 63. Drive Circuit for High Input Frequencies

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 62 and Figure 63. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50Ω (for a 50Ω source impedance).

CLOCK INPUT

The ADS41B29/49 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 64 shows an equivalent circuit for the input clock.



NOTE: C_{EQ} is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

Figure 64. Input Clock Equivalent Circuit

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1μF capacitor, as shown in Figure 65. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 66 shows a differential circuit.

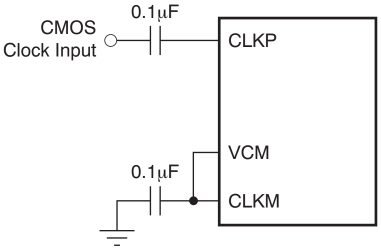


Figure 65. Single-Ended Clock Driving Circuit

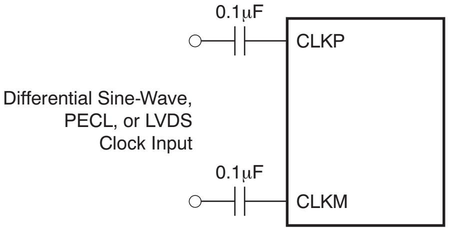


Figure 66. Differential Clock Driving Circuit

GAIN FOR SFDR/SNR TRADE-OFF

The ADS41B29/49 include gain settings that can be used to get improved SFDR performance. The gain is programmable from 0dB to 3.5dB (in 0.5dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 8.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5dB and 1dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used to trade-off between SFDR and SNR.

After a reset, the gain is enabled with 0dB gain setting. For other gain settings, program the GAIN register bits.

Table 8. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	1.5
0.5	Programmable gain	1.41
1	Programmable gain	1.33
1.5	Programmable gain	1.26
2	Programmable gain	1.19
2.5	Programmable gain	1.12
3	Programmable gain	1.06
3.5	Programmable gain	1

OFFSET CORRECTION

The ADS41B29/49 has an internal offset corretion algorithm that estimates and corrects dc offset up to ±10mV. The correction can be enabled using the EN OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 9.

Table 9. Time Constant of Offset Correction Loop

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0000	1M	4ms
0001	2M	8ms
0010	4M	16.7ms
0011	8M	33.5ms
0100	16M	67ms
0101	32M	134ms
0110	64M	268ms
0111	128M	537ms
1000	256M	1.1s
1001	512M	2.15s
1010	1G	4.3s
1011	2G	8.6s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250MSPS.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by a default after reset.

After a reset, the offset correction is disabled.. To use offset correction set EN OFFSET CORR to '1' and program the required time constant. Figure 67 shows the time response of the offset correction algorithm after it is enabled.

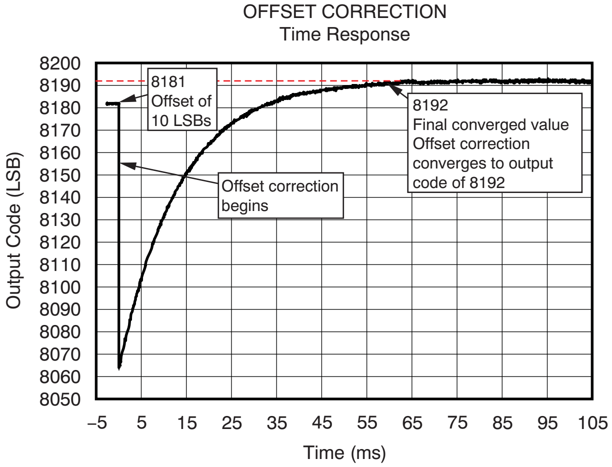


Figure 67. Time Response of Offset Correction

POWER DOWN

The ADS41B29/49 has three power-down modes: power-down global, standby, and output buffer disable.

Power-Down Global

In this mode, the entire chip (including the ADC, internal reference, and the output buffers) is powered down, resulting in reduced total power dissipation of about 7mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100µs. To enter the global power-down mode, set the PDN GLOBAL register bit.

Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5µs. The total power dissipation in standby mode is approximately 200mW. To enter the standby mode, set the STBY register bit.

Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wakeup time from this mode is fast, approximately 100ns. This can be controlled using the PDN OBUF register bit or using the OE pin.

Input Clock Stop

In addition, the converter enters a low-power mode when the input clock frequency falls below 1MSPS. The power dissipation is approximately 92mW.

POWER-SUPPLY SEQUENCE

During power-up, the AVDD, AVDD_BUF, and DRVDD supplies can come up in any sequence. These supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INFORMATION

The ADS41B29/49 provide either 14-bit data or 12-bit data, respectively, and an output clock synchronized with the data.

Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the LVDS CMOS serial interface register bit or using the DFS pin.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 68 and Figure 69.

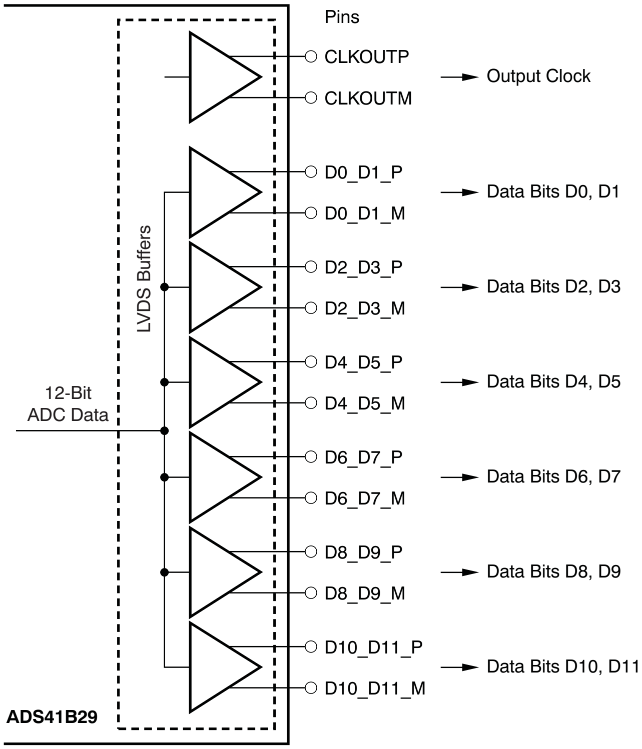


Figure 68. ADS41B29 LVDS Data Outputs

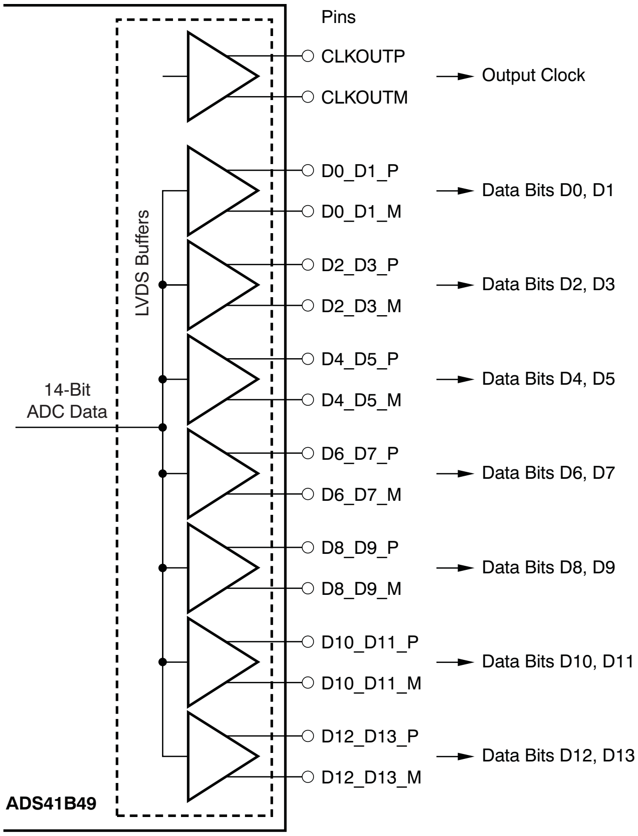


Figure 69. ADS41B49 LVDS Data Outputs

Even data bits (D0, D2, D4, etc.) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3, D5, etc.) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits, as shown in Figure 70.

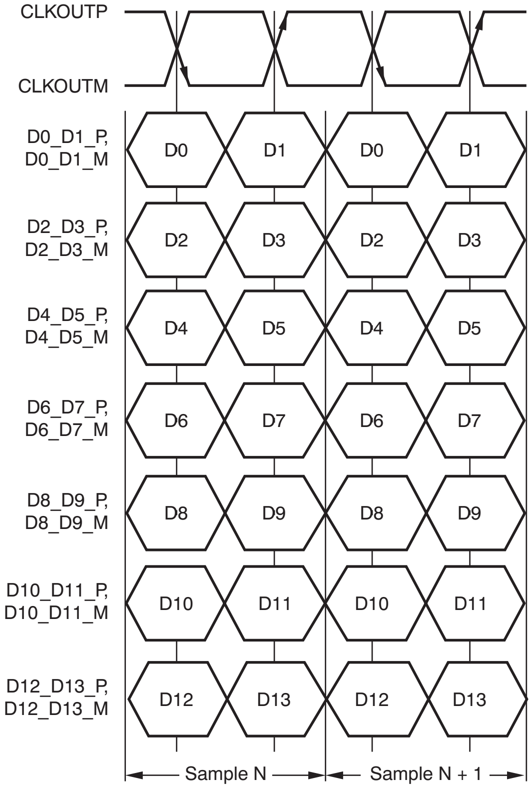


Figure 70. DDR LVDS Interface

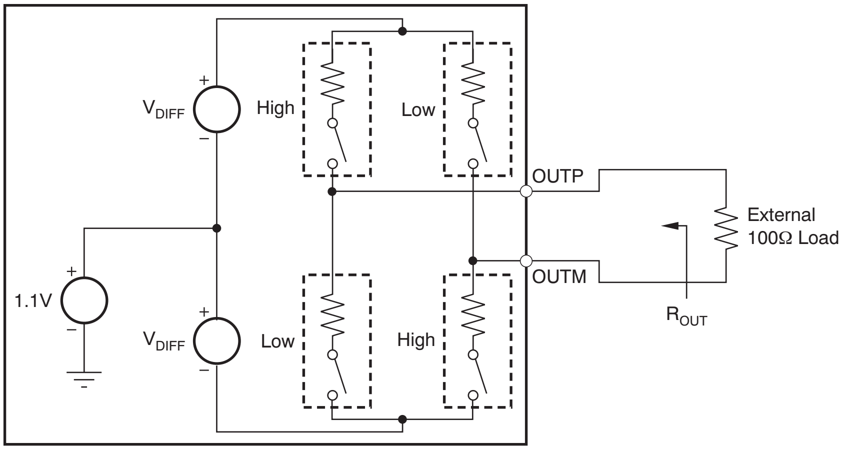
LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 71. After reset, the buffer presents an output impedance of 100Ω to match with the external 100Ω termination.

The V_{DIFF} voltage is nominally 350mV, resulting in an output swing of ±350mV with 100Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125mV to ±570mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.



NOTE: Use the default buffer strength to match 100Ω external termination (R_{OUT} = 100Ω). To match with a 50Ω external termination, set the LVDS STRENGTH bit (R_{OUT} = 50Ω).

Figure 71. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. Figure 72 depicts the CMOS output interface.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures a wide data stable window (even at 250MSPS) is provided so the data outputs have minimal load capacitance. It is recommended to use short traces (one to two inches or 2,54cm to 5,08cm) terminated with less than 5pF load capacitance, as shown in Figure 73.

For sampling frequencies greater than 200MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture data.

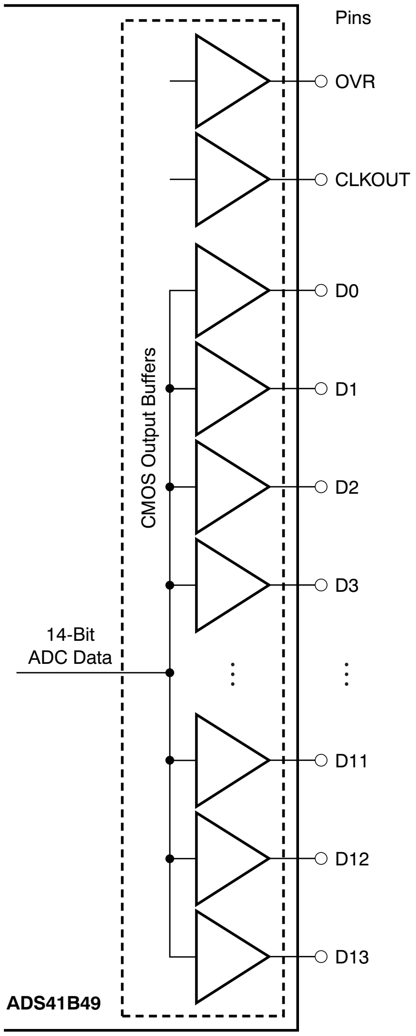


Figure 72. CMOS Output Interface

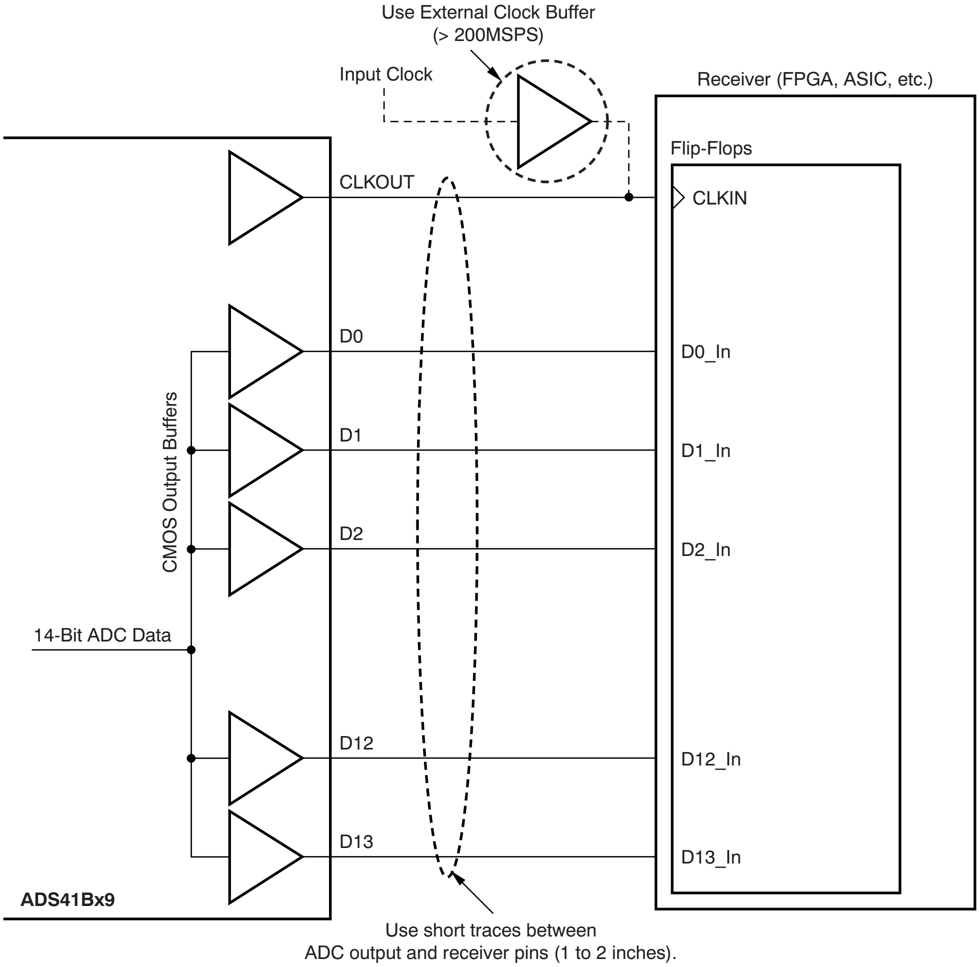


Figure 73. Using the CMOS Data Outputs

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between '0' and '1' every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital Current as a Result of CMOS Output Switching = $C_L \times DRVDD \times (N \times f_{AVG})$

where:

C_L = load capacitance,

$N \times F_{AVG}$ = average number of output bits switching. (1)

Figure 52 illustrates the current across sampling frequencies at 2MHz analog input frequency.

Input Over-Voltage Indication (OVR Pin)

The device has an OVR pin that provides information about analog input overload. At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. The OVR remains high as long as the overload condition persists. The OVR pin is a CMOS output buffer (running off DRVDD supply), independent of the type of output data interface (DDR LVDS or CMOS).

For a positive overload, the D[13:0] output data bits are 0x3FFF in offset binary output format and 0x1FFF in twos complement output format. For a negative input overload, the output code is 0x0000 in offset binary output format and 0x2000 in twos complement output format.

Output Data Format

Two output data formats are supported: twos complement and offset binary. They can be selected using the DATA FORMAT serial interface register bit or controlling the DFS pin in parallel configuration mode. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level.

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS414x, ADS412x EVM User Guide* (SLWU067) for details on layout and grounding.

Supply Decoupling

Because the ADS41B29/49 already include internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271), both available for download at the TI web site (www.ti.com).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 – 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$\text{SNR} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \tag{2}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$\text{SINAD} = 10\text{Log}^{10}\ \frac{P_S}{P_N + P_D} \tag{3}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (4)$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \quad (5)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{SUP}}\ \text{(Expressed in dBc)} \quad (6)$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{CM}}\ \text{(Expressed in dBc)} \quad (7)$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
ADS41B29IRGZ25	ACTIVE	VQFN	RGZ	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS41B29IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS41B29IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS41B49IRGZ25	ACTIVE	VQFN	RGZ	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS41B49IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS41B49IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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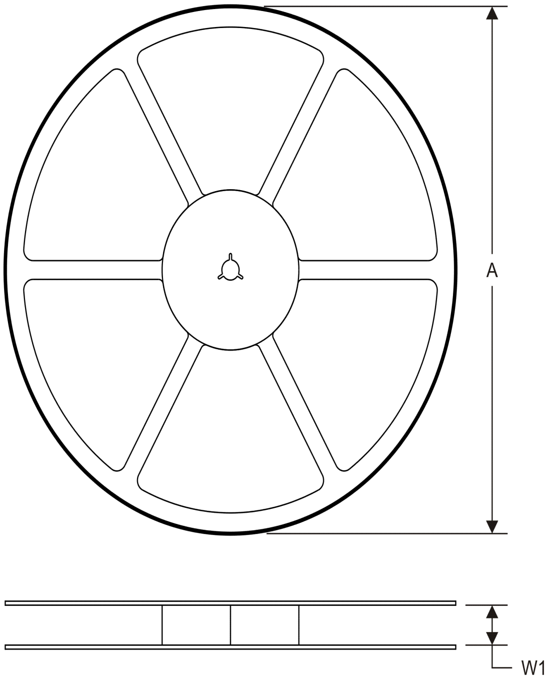
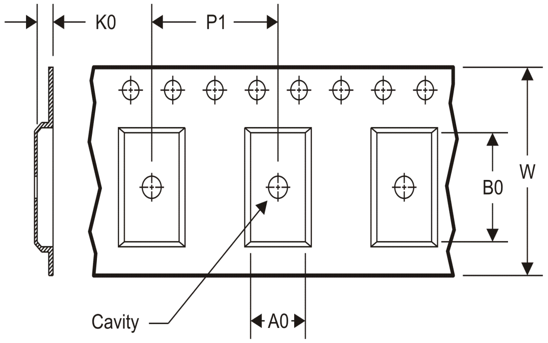
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



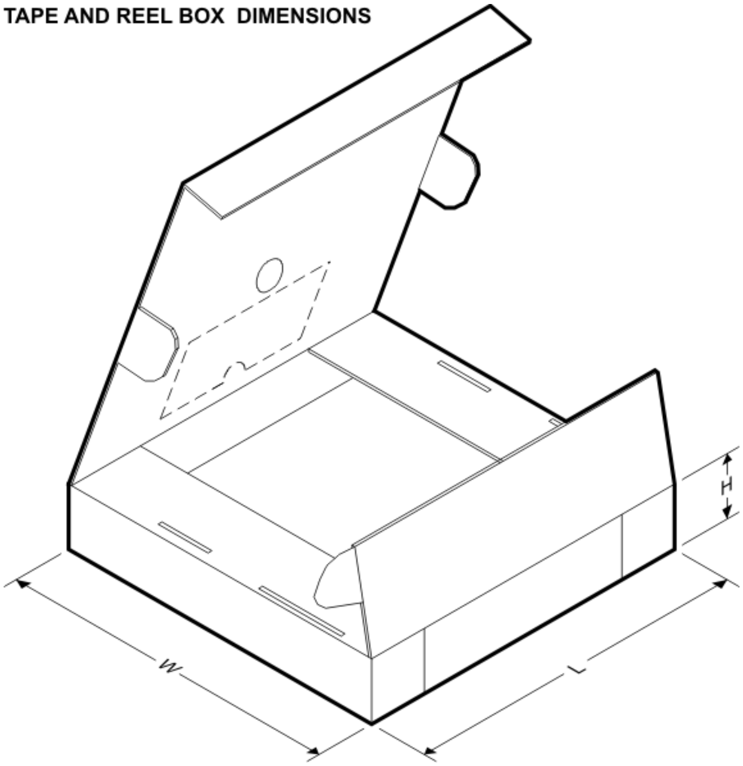
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS41B29IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS41B29IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS41B49IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS41B49IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

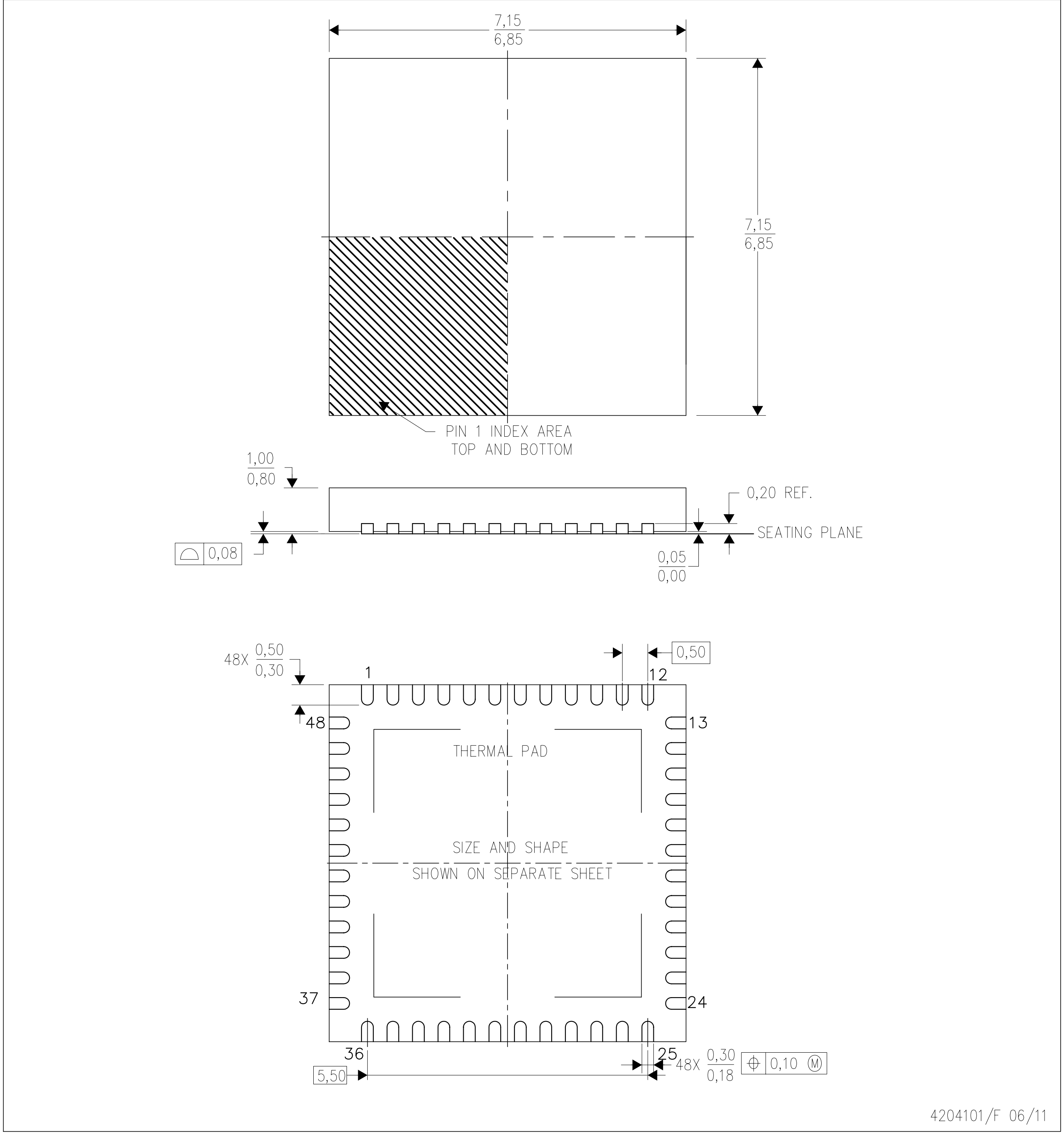
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS41B29IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS41B29IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
ADS41B49IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS41B49IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

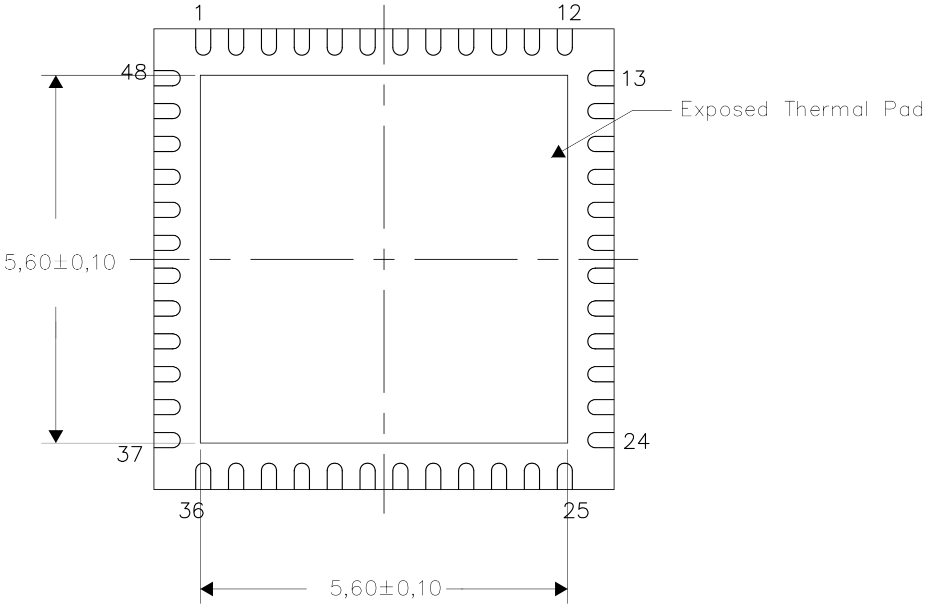
RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



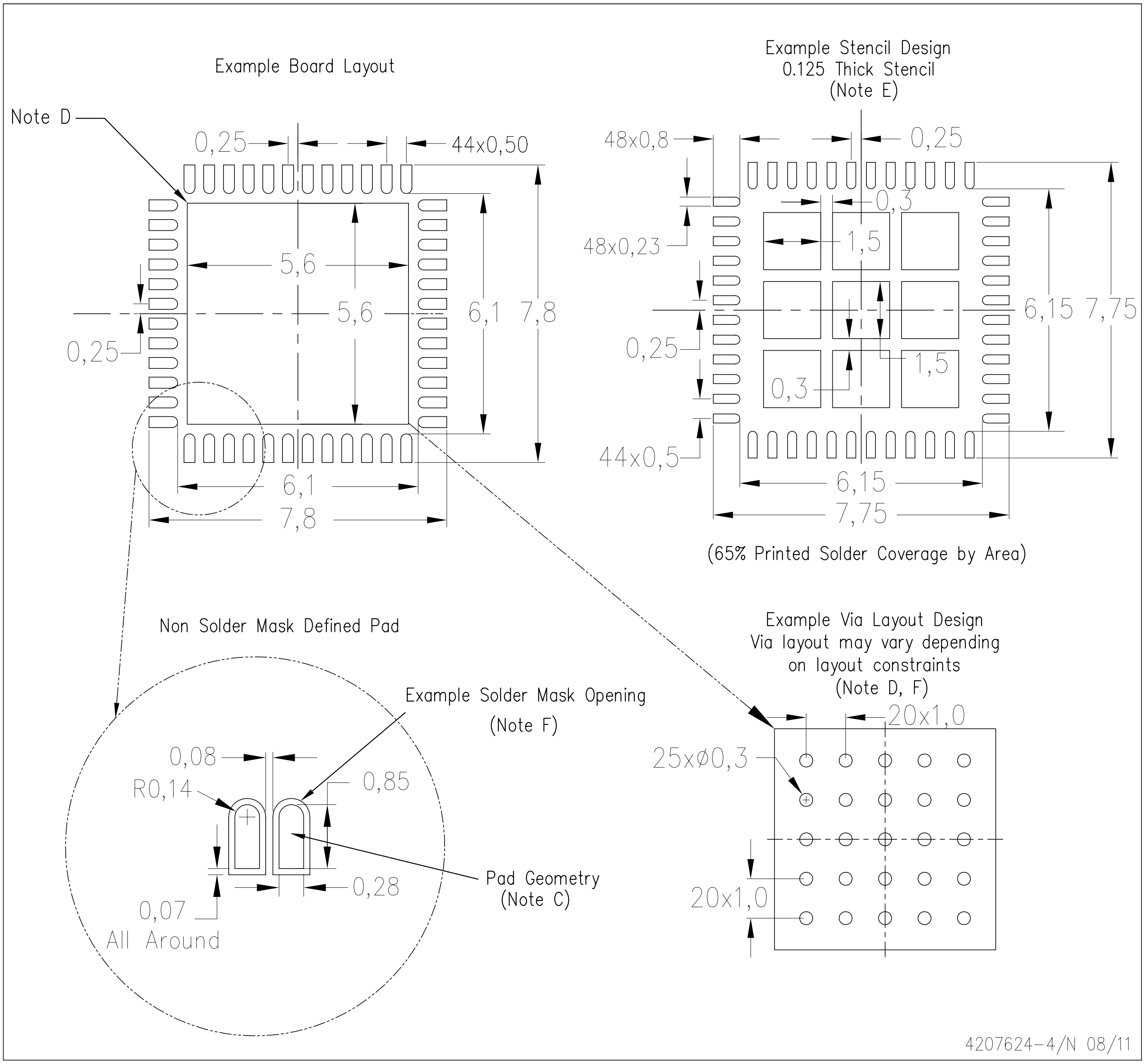
Bottom View

Exposed Thermal Pad Dimensions

4206354-5/R 08/11

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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