LM2698 SIMPLE SWITCHER® 1.35A Boost Regulator

Check for Samples: LM2698

FEATURES

- **1.9A, 0.2Ω, Internal Switch (typical)**
- **Operating Voltage as Low as 2.2V**
- **600kHz/1.25MHz Adjustable Frequency Operation**
- **Switchers Made Simple® Software**
- **8-Lead VSSOP package**

APPLICATIONS

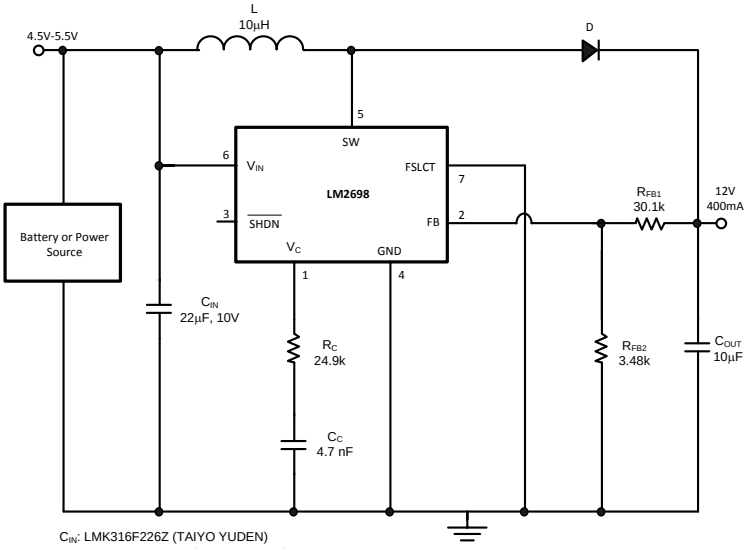
- **3.3V to 5V, 5V to 12V Conversion**
- **Distributed Power**
- **Set-Top Boxes**
- **DSL Modems**
- **Diagnostic Medical Instrumentation**
- **Boost Converters**
- **Flyback Converters**
- **SEPIC Converters**

DESCRIPTION

The LM2698 is a general purpose PWM boost converter. The 1.9A, 18V, 0.2ohm internal switch enables the LM2698 to provide efficient power conversion to outputs ranging from 2.2V to 17V. It can operate with input voltages as low as 2.2V and as high as 12V. Current-mode architecture provides superior line and load regulation and simple frequency compensation over the device's 2.2V to 12V input voltage range. The LM2698 sets the standard in power density and is capable of supplying 12V at 400mA from a 5V input. The LM2698 can also be used in flyback or SEPIC topologies.

The LM2698 SIMPLE SWITCHER® features a pin selectable switching frequency of either 600kHz or 1.25MHz. This promotes flexibility in component selection and filtering techniques. A shutdown pin is available to suspend the device and decrease the quiescent current to 5µA. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. Switchers Made Simple® software is available to ensure a quick, easy and assured design. The LM2698 is available in a low profile 8-lead VSSOP (DGK) package.

Typical Application Circuit



Connection Diagram

Top View

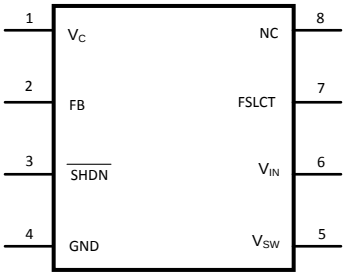


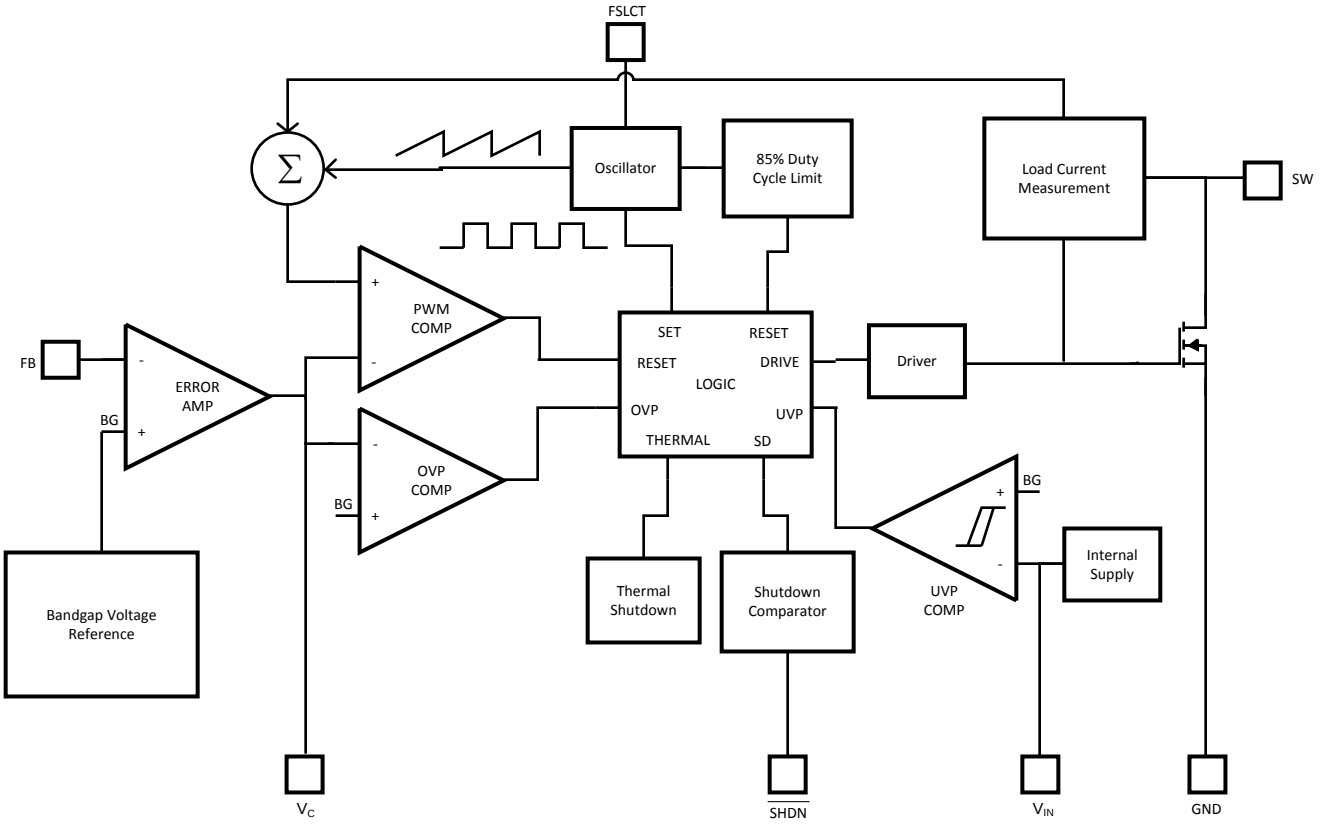
Figure 1. 8-Lead Plastic VSSOP

Pin Functions

Pin Description

Pin	Name	Function
1	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	Output voltage feedback input.
3	$\overline{SHDN}$	Shutdown control input, active low.
4	GND	Analog and power ground.
5	V_{SW}	Power switch input. Switch connected between SW pin and GND pin.
6	V_{IN}	Analog power input.
7	FSLCT	Switching frequency select input. V_{IN}= 1.25MHz. Ground = 600kHz.
8	NC	Connect to ground.

Block Diagram



ORDERING INFORMATION(1)

ORDER NUMBER	PACKAGE TYPE	PACKAGE QUANTITY
LM2698MM-ADJ	VSSOP	1000
LM2698MM-ADJ/NOPB		1000
LM2698MMX-ADJ		3500
LM2698MMX-ADJ/NOPB		3500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

V_{IN}	$-0.3V \le V_{IN} \le 12V$
SW Voltage	$-0.3V \le V_{SW} \le 18V$
FB Voltage	$-0.3V \le V_{FB} \le 7V$
V_C Voltage	$0.965 < V_C < 1.565$
$\overline{SHDN}$ Voltage (2)	$-0.3V \le V_{SHDN} \le 7V$
FSLCT (2)	$-0.3V \le V_{FSLCT} \le 12V$
Maximum Junction Temperature	150°C
Power Dissipation (3)	Internally Limited
Lead Temperature	300°C
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (4)	
Human Body Model (5)	2kV
Machine Model	200V

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be specified. For assured specifications and test conditions, see the Electrical Characteristics.
(2) Shutdown and voltage frequency select should not exceed V_{IN}.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = $(T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.
(5) ESD susceptibility using the human body model is 500V for V_C.

Operating Conditions

Operating Junction Temperature Range (1)	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Supply Voltage	2.2V to 12V
SW Voltage	$0 \le V_{SW} \le 17.5V$

(1) All limits are specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C)Unless otherwise specified. V_{IN} =2.2V and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_Q	Quiescent Current	FB = 0V (Not Switching)		1.3	**2.0**	mA
		$V_{\overline{SHDN}}$ = 0V		5	**10**	µA
V_{FB}	Feedback Voltage		**1.2285**	1.26	**1.2915**	V
I_{CL}	Switch Current Limit	V_{IN} = 2.7V (3)	**1.35**	1.9	**2.4**	A
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	2.2V ≤ V_{IN} ≤ 12.0V		0.013	**0.1**	%/V
I_B	FB Pin Bias Current (4)			0.5	**20**	nA
V_{IN}	Input Voltage Range		**2.2**		**12**	V
g_m	Error Amp Transconductance	ΔI = 5µA	**40**	135	**290**	µmho
A_V	Error Amp Voltage Gain			120		V/V
D_{MAX}	Maximum Duty Cycle	FSLCT = Ground	**78**	85		%
D_{MIN}	Minimum Duty Cycle	FSLCT = Ground		15		%
		FSLCT = V_{IN}		30		
f_S	Switching Frequency	FSLCT = Ground	**480**	600	**720**	kHz
		FSLCT = V_{IN}	**1**	1.25	**1.5**	MHz
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = V_{IN}		0.01	**0.1**	µA
		$V_{\overline{SHDN}}$ = 0V		−0.5	**-1**	
I_L	Switch Leakage Current	V_{SW} = 18V		0.01	**3**	µA
$R_{DS(ON)}$	Switch $R_{DS(ON)}$	V_{IN} = 2.7V, I_{SW} = 1A		0.2	**0.4**	Ω
TH_{SHDN}	$\overline{SHDN}$ Threshold Voltage	Output High		0.6	**0.9**	V
		Output Low	**0.3**	0.6		V
UVP	On Threshold		**1.95**	2.05	**2.2**	V
	Off Threshold		**1.85**	1.95	**2.1**	V
θ_{JA}	Thermal Resistance	Junction to Ambient (5)		235		°C/W
		Junction to Ambient (6)		225		
		Junction to Ambient (7)		220		
		Junction to Ambient (8)		200		
		Junction to Ambient (9)		195		

(1) All limits are specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) This is the switch current limit at 0% duty cycle. The switch current limit will change as a function of duty cycle. See Typical performance Characteristics section for I_{CL} vs. V_{IN}
(4) Bias current flows into FB pin.
(5) Junction to ambient thermal resistance (no external heat sink) for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit. See "Scenario 'A'" in the Power Dissipation section.
(6) Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0191 sq. in. of copper heat sinking. See "Scenario 'B'" in the Power Dissipation section.
(7) Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0465 sq. in. of copper heat sinking. See "Scenario 'C'" in the Power Dissipation section.
(8) Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.2523 sq. in. of copper heat sinking. See "Scenario 'D'" in the Power Dissipation section.
(9) Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0098 sq. in. of copper heat sinking on the top layer and 0.0760 sq. in. of copper heat sinking on the bottom layer, with three 0.020 in. vias connecting the planes. See "Scenario 'E'" in the Power Dissipation section.

Typical Performance Characteristics

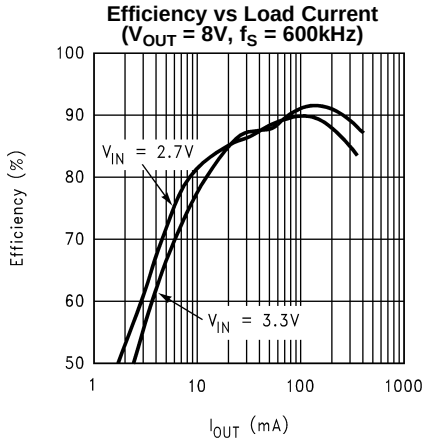


Figure 2.

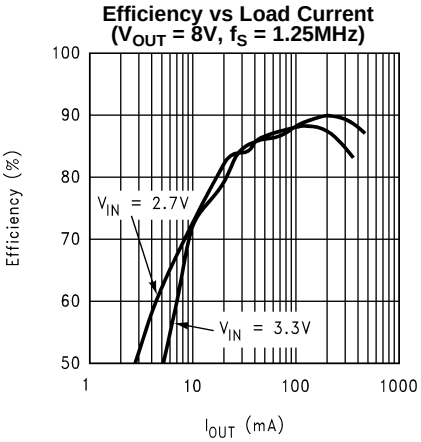


Figure 3.

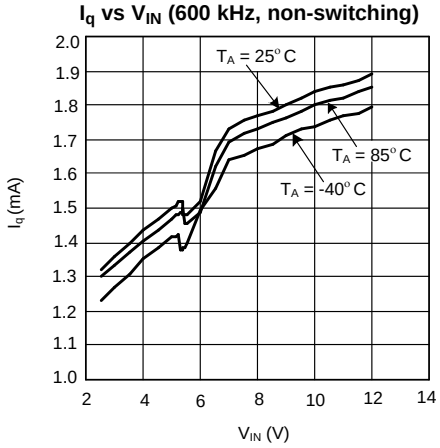


Figure 4.

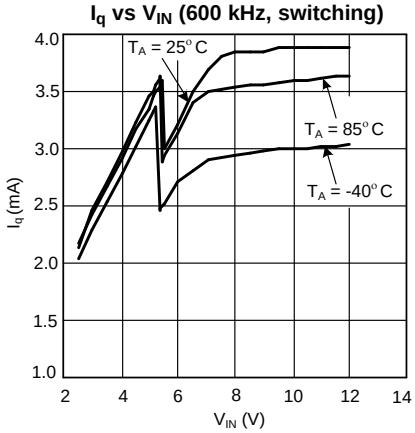


Figure 5.

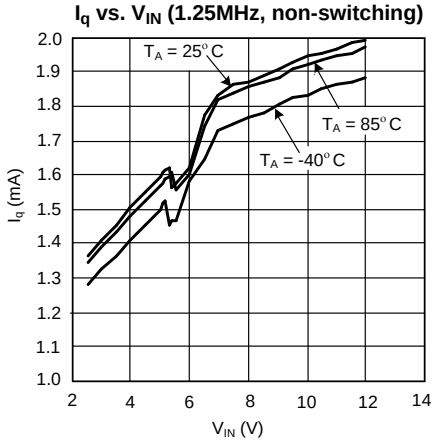


Figure 6.

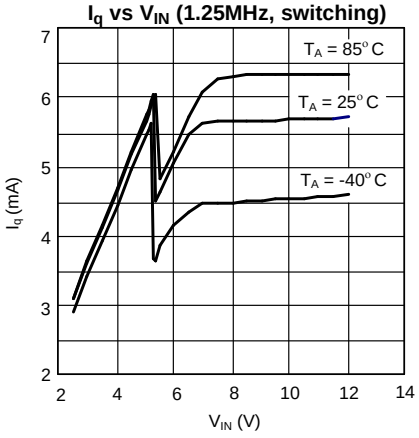


Figure 7.

Typical Performance Characteristics (continued)

$I_{q(SHDN)}$ vs V_{IN}

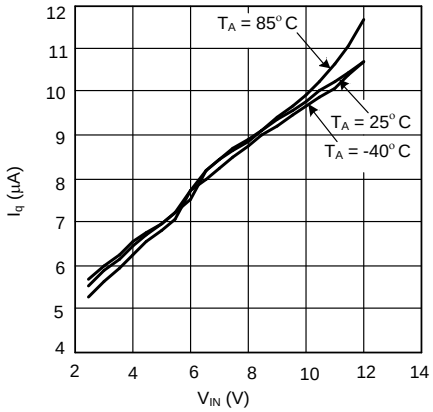


Figure 8.

$R_{DS(ON)}$ vs V_{IN}

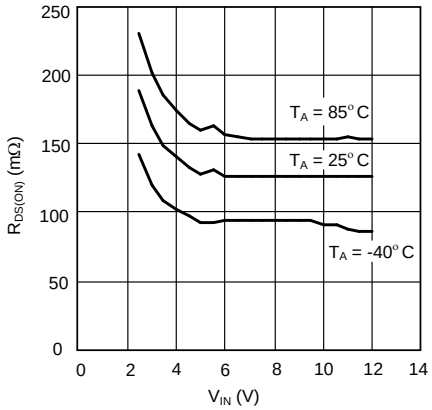


Figure 9.

Switching Frequency vs V_{IN} (600kHz)

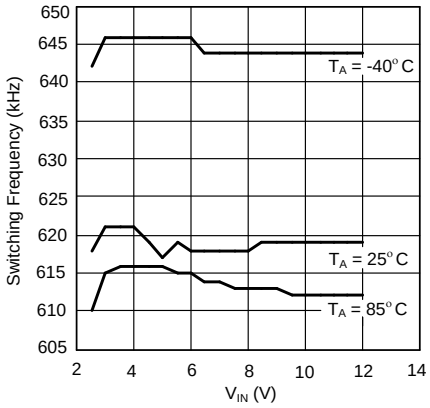


Figure 10.

Switching Frequency vs V_{IN} (1.25MHz)

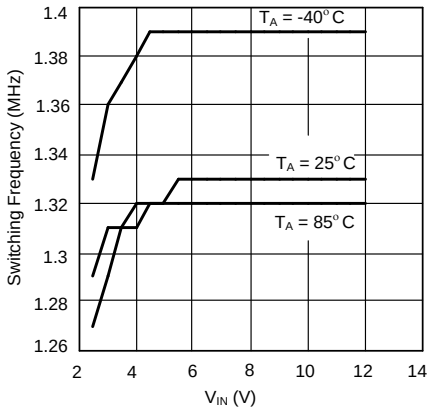


Figure 11.

I_{CL} vs. Ambient Temperature
V_{IN} = 3.3V, V_{OUT} = 8V

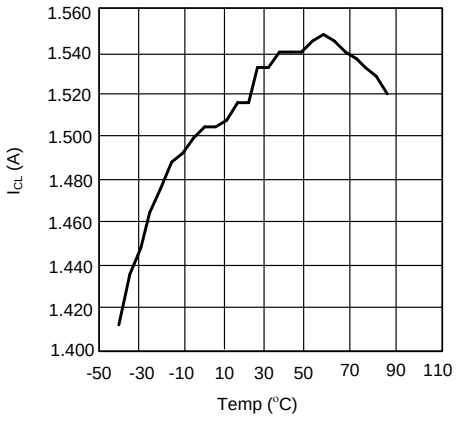


Figure 12.

I_{CL} vs. V_{IN}

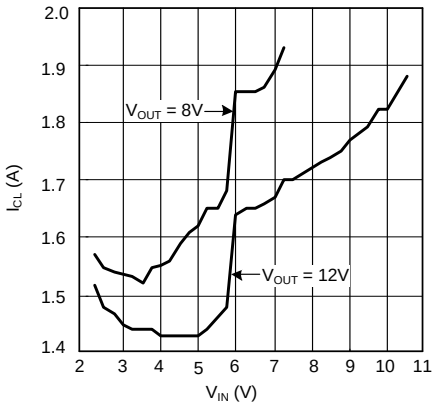


Figure 13.

Operation

Continuous Conduction Mode

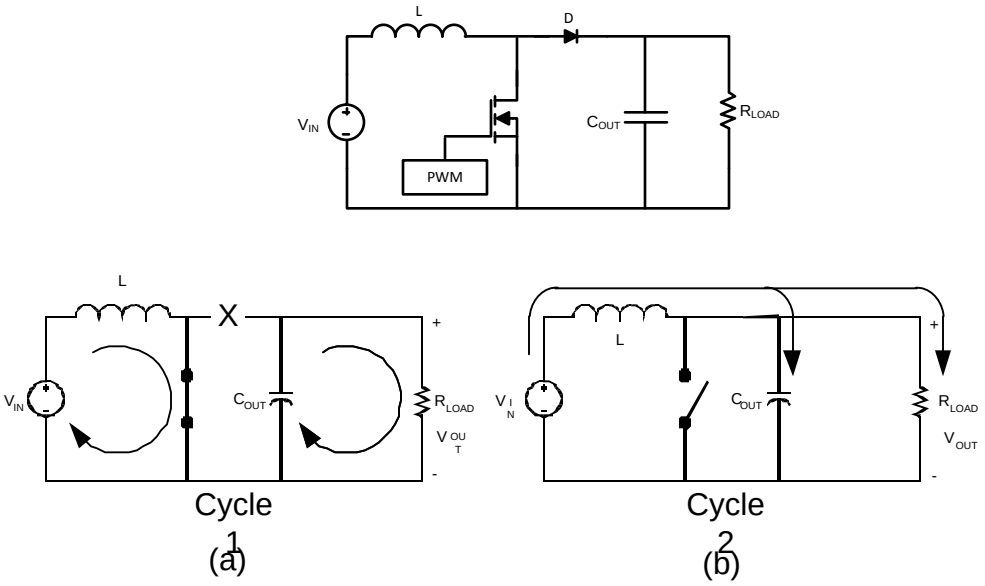


Figure 14. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

The LM2698 is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 14 (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in Figure 14 (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined as:

$$V_{OUT} = \frac{V_{IN}}{1-D} \tag{1}$$

where D is the duty cycle of the switch.

Inductor

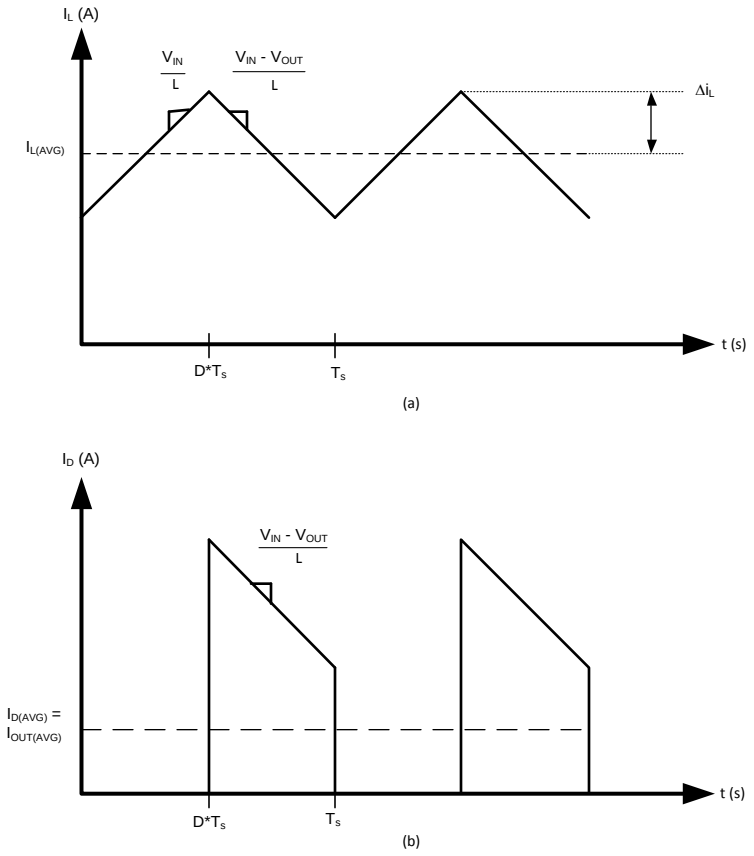


Figure 15. (a) Inductor Current (b) Diode Current

The inductor is one of the two energy storage elements in a boost converter. Figure 15 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified as:

$$V_L(t) = L \frac{di_L(t)}{dt} \quad (2)$$

If $V_{L(t)}$ is constant, di_L / dt must be constant, thus the current in the inductor changes at a constant rate. This is the case in DC/DC converters since the voltages at the input and output can be approximated as a constant. The current through the inductor of the LM2698 boost converter is shown in Figure 15(a). The important quantities in determining a proper inductance value are $I_{L(AVG)}$ (the average inductor current) and Δi_L (the inductor current ripple). If Δi_L is larger than $I_{L(AVG)}$, the inductor current will drop to zero for a portion of the cycle and the converter will operate in discontinuous conduction mode. If Δi_L is smaller than $I_{L(AVG)}$, the inductor current will stay above zero and the converter will operate in continuous conduction mode (CCM). All the analysis in this datasheet assumes operation in continuous conduction mode. To operate in CCM:

$$I_{L(AVG)} > \Delta i_L \quad (3)$$

$$\frac{I_{OUT(AVG)}}{1-D} > \frac{V_{IN} \times D}{2 \times f_S \times L} \quad (4)$$

$$L > \frac{V_{IN} \times D \times (1-D)}{2 \times f_S \times I_{OUT(AVG)}} \quad (5)$$

Choose the minimum I_{OUT} to determine the minimum L for CCM operation. A common choice is to set Δi_L to 30% of $I_{L(AVG)}$.

The inductance value will also affect the stability of the converter. Because the LM2698 utilizes current mode control, the inductor value must be carefully chosen. See the Compensation section for recommended inductance values.

Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter,

$$I_{L(AVG)} = \frac{I_{OUT(AVG)}}{1-D} \quad (6)$$

and

$$I_{L(Peak)} = I_{L(AVG)} + \Delta i_L,$$

where

$$\Delta i_L = \frac{DV_{IN}}{2Lf_s} \quad (7)$$

A core size with ratings higher than these values should be chosen. If the core is not properly rated, saturation will dramatically reduce overall efficiency.

Current Limit

The current limit in the LM2698 is referenced to the peak switch current. The peak currents in the switch of a boost converter will always be higher than the average current supplied to the load. To determine the maximum average output current that the LM2698 can supply, use:

$$I_{OUT(MAX)} = (I_{CL} - \Delta i_L)*(1-D) = (I_{CL} - \Delta i_L)*V_{IN}/V_{OUT} \quad (8)$$

Where I_{CL} is the switch current limit (see Electrical Charateristics table and Typical Performance Curves). Hence, as V_{IN} increases, the maximum current that can be supplied to the load increases, as shown in Figure 16.

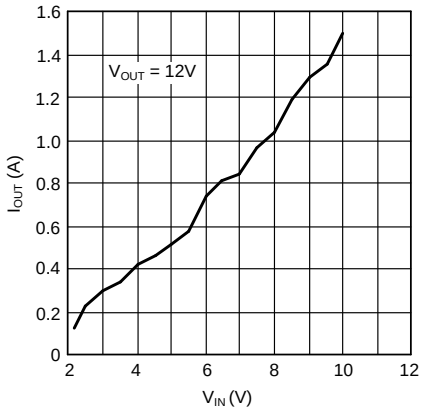


Figure 16. Maximum Output Current vs Input Voltage

Diode

The diode in a boost converter such as the LM2698 acts as a switch to the output. During the first cycle, when the transistor is closed, the diode is reverse biased and current is blocked; the load current is supplied by the output capacitor. In the second cycle, the transistor is open and the diode is forward biased; the load current is supplied by the inductor.

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. To improve efficiency, a low forward drop Schottky diode is recommended.

Input Capacitor

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the inductor gets smaller, the input ripple increases. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta i_L/\sqrt{3} = \frac{1}{2\sqrt{3}}\left(\frac{V_{in}V_o - V_{in}^2}{f_s L V_o}\right) \quad (9)$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not so critical in boost applications, a 10 µF or higher value, good quality capacitor prevents any impedance interactions with the input supply.

A 0.1µF or 1µF ceramic bypass capacitor is also recommended on the V_{IN} pin (pin 6) of the IC. This capacitor must be connected very close to pin 6 to effectively filter high frequency noise. When operating at 1.25 MHz switching frequency, a minimum bypass capacitance of 0.22 µF is recommended.

Output Capacitor

The output capacitor in a boost converter provides all the output current when the switch is closed and the inductor is charging. As a result, it sees very large ripple currents. The output capacitor should be capable of handling the maximum RMS current. The RMS current in the output capacitor is:

$$I_{COUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}^2\frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]} \quad (10)$$

where,

$$\Delta i_L = \frac{DV_{IN}}{2Lf_s} \quad (11)$$

and

$$D = (V_{OUT} - V_{IN})/V_{OUT} \quad (12)$$

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic, and polymer tantalum, Sanyo OS-CON, or multi-layer ceramic capacitors are recommended at the output.

Compensation

This section presents a step-by-step procedure to design the compensation network at pin 1 (V_c) of the LM2698. These design methods will produce a conservative and stable control loop.

There is a minimum inductance requirement in any current mode converter. This is a function of V_{OUT}, duty cycle, and switching frequency, among other things. Figure 18 plots the recommended inductance range vs. duty cycle for V_{OUT} = 12V. The two lines represent the upper and lower bounds of the recommended inductance range. The simplified compensation procedure that follows assumes that the inductance never drops below the Q = 5 line. Figure 18 plots the equation:

$$L = \frac{V_{OUT} \times R_{DSON}}{Se}\left(\frac{1}{\pi Q} + D - 0.5\right) \quad (13)$$

where,

R_{DSON} = 0.15,

Se = 0.072*f_S,

and Q = 0.5 and 5

Use Q = 5 to calculate the minimum inductance recommended for a stable design. Choosing an inductor between the Q = 0.5 and Q = 5 values provides a good tradeoff between size and stability. Note that as V_{IN} drops less than 5V, $R_{DS(ON)}$ increases, as shown in the Typical Performance Characteristics section ($R_{DS(ON)}$ vs.V_{IN} curve). The worst case $R_{DS(ON)}$ should be used when choosing the inductance. To view plots for different Vout, multiply the Y axis by a factor of V_{OUT}/12, or plot Equation 13 for the respective output voltage.

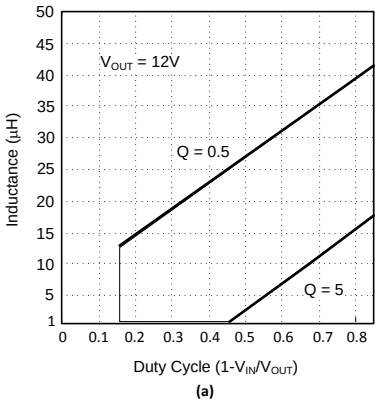


Figure 17. Minimum Inductance Requirements for (a) f_S = 600kHz

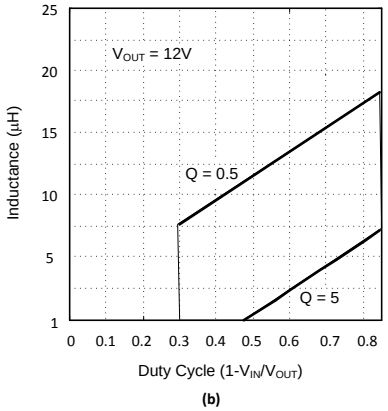


Figure 18. Minimum Inductance Requirements for (b) f_S = 1.25MHz

The goal of the compensation network is to provide the best static and dynamic performance while insuring stability over line and load variations. The relationship of stability and performance can be best analyzed by plotting the magnitude and phase of the open loop frequency response in the form of a bode plot. A typical bode plot of the LM2698 open loop frequency response is shown in Figure 19.

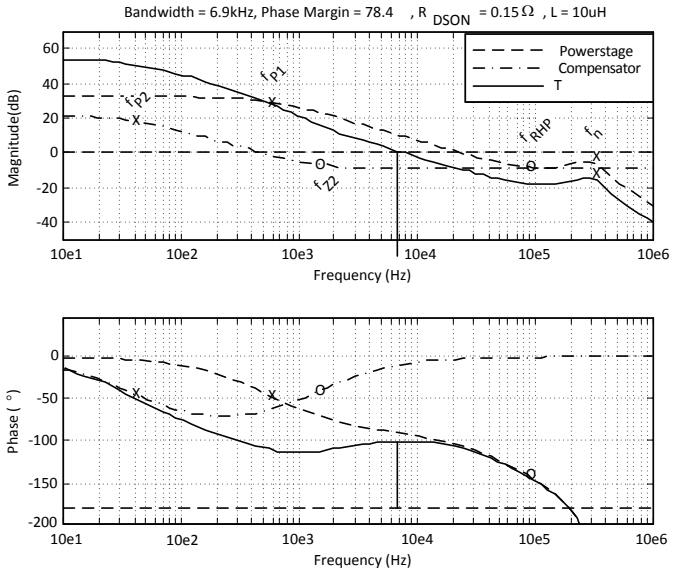


Figure 19. Bode plot of the LM2698 Frequency Response using the Typical Application Circuit

Poles are marked with an 'X', and zeros are marked with a 'O'. The bolded '**O**' labeled 'f_{RHP}' is a right-half plane zero. Right half plane zeros act like normal zeros to the magnitude (+20dB/decade slope influence) and like poles to the phase (−90° shift). Three curves are shown. The powerstage curve is the frequency response of the powerstage, which includes the switch, diode, inductor, output capacitor, and load. The compensator curve is the frequency response of the compensator, which is the error amp combined with the compensation network. T is the product of the powerstage and the compensator and is the complete open loop frequency response. The power stage response is fixed by line and load constraints, while the compensator is set by the external compensation network at pin 1. The compensator can be designed in a few simple steps as follows.

Quick Compensator Design

Calculate:

$$\omega_{PI(MAX)} \approx \frac{1}{C_{OUT} R_{LOAD(MIN)}} \text{ (rad/s)} \quad (14)$$

where,

$$R_{LOAD(MIN)} = \frac{V_{OUT}}{I_{OUT(MAX)}} \quad (15)$$

$$\omega_{RHP(MIN)} = \frac{R_{LOAD(MIN)} \left(\frac{V_{IN(MIN)}}{V_{OUT}}\right)^2}{L} \text{ (rad/s)} \quad (16)$$

$$\text{Set } \omega_{P2} = 2\pi(40)\text{(rad/s)} \approx \frac{1}{C_{C1} R_{OUT}} \text{ (rad/s)} \quad (17)$$

where R_{OUT} = 875kΩ

Choose C_{C1} = 4.7nF

$$\omega_{z2} = 10 \times \omega_{P1(max)} \frac{A_{DC} \omega_{P2}}{\omega_{RHP(MIN)}} = \frac{1}{C_{C1} R_C} \text{ (rad/s),} \quad (18)$$

Choose

$$R_C = \frac{\omega_{RHP(MIN)}}{10 \times A_{DC} C_{C1} \omega_{P1(max)} \omega_{P2}} \Omega \quad (19)$$

Where,

$$A_{DC} = \frac{118 * R_{LOAD(MIN)}}{R_{DSON(MIN)}} \times \frac{(1 - D_{MAX})}{\frac{(1 - D_{MAX})^3 R_{LOAD(MIN)}}{2Lf_S} \left(1 + \frac{0.144 * f_S L}{V_{IN} R_{DSON(MIN)}}\right) + 1 + D_{MAX}} \quad (20)$$

If the output capacitor is of high ESR (0.1Ω or higher), it may be necessary to use C_{C2}. A rule of thumb is that if $1/(2\pi C_{OUT} ESR)$ (Hz) is lower than $f_S/2$ (Hz), C_{C2} should be used. Choose C_{C2} such that:

$$(R_C + R_{OUT})(C_{OUT} ESR) / (R_C R_{OUT}) \text{ (F)} \quad (21)$$

where R_{OUT} = output impedance of the error amp (875 kΩ).

Improving Transient Response Time

The above compensator design provides a loop gain with high phase margin for a large stability margin. The transient response time of this loop is limited by the lower mid-frequency gain necessary to achieve a high phase margin. If it is desired to increase the transient response time, C_{C1} may be decreased. Decreasing C_{C1} by 2x, 4x, and 6x will yield increasingly shorter transient response times, however the loop phase margin will become progressively lower as C_{C1} is decreased. When optimizing the loop gain for transient response time, it is recommended to keep the phase margin above 40°.

Additional Comments on the Open Loop Frequency Response

The procedure used here to pick the compensation network will provide a good starting point. In most cases, these values will be sufficient for a stable design. It is always recommended to check the design in a real test setup. This is easy to do with the aid of a dynamic load. Set the high and low load values to your system requirements and switch between the two at about 1kHz. View the output voltage with an oscilloscope using AC coupling, and zoom in enough to see the waveform react to the load change. Use the following table to determine if your design is stable. Remember to use worst case conditions ($V_{IN(MIN)}$, $R_{OUT(MIN)}$, $R_{OUT(MAX)}$).

Response	Conclusion	What to Change
Underdamped, weak attenuation	Nearing instability	Make C_{C1} larger
Underdamped, strong attenuation	Stable	Nothing
Critically damped	Stable	Nothing
Overdamped	Stable	Nothing

APPLICATION INFORMATION

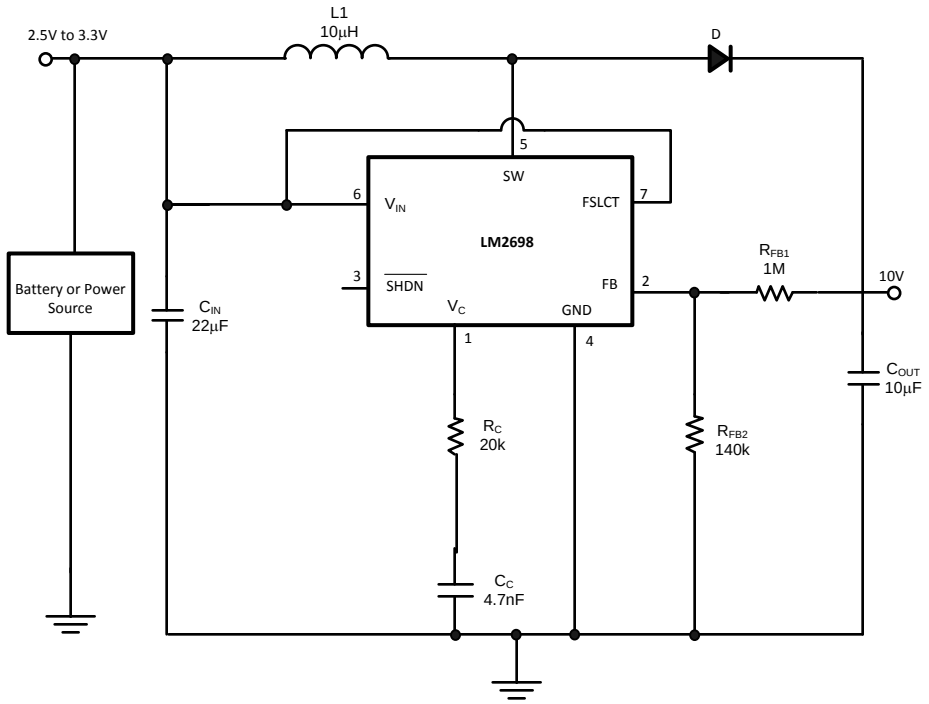


Figure 20. 3.3V to 10V Boost Converter

1.25MHz Boost Converter

Figure 20 shows the LM2698 boosting 3.3V to 10V at 300mA. As discussed in the Compensation section, the $R_{DS(ON)}$ of the internal FET in the LM2698 raises as the input voltage drops below 5V (see Typical Performance Characteristics). The minimum input voltage for this application is 2.5V, at which point the $R_{DS(ON)}$ is approximately 200mΩ. Substituting these values in for Equation 13, it is found that either a 10 µH (1.25MHz operation) or a 22 µH (600kHz operation) is necessary for a stable design. The circuit is operated at 1.25MHz to allow for a smaller inductance. From the Compensator Design equations, R_C is calculated to be 18.6kΩ, and a 20kΩ resistor is used.

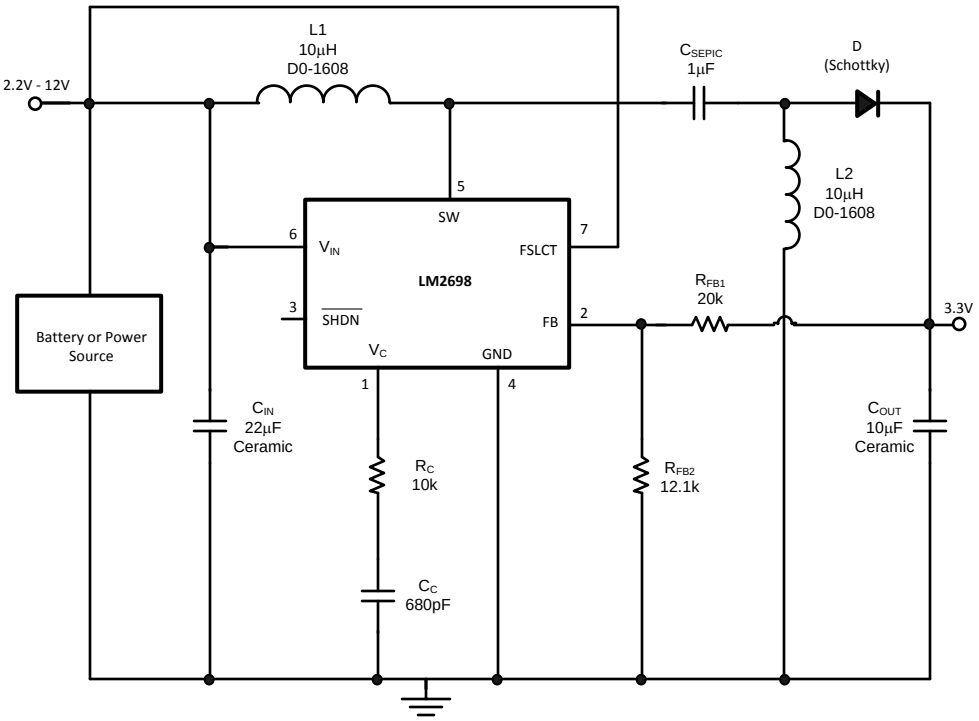


Figure 21. 3.3V SEPIC Converter

3.3V SEPIC

The LM2698 can be used to implement a SEPIC technology. The advantages of the SEPIC topology are that it can step up or step down an input voltage, and it has low input current ripple.

The conversion ratio for the SEPIC is :

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{D'} \tag{22}$$

where

$$D' = 1-D \tag{23}$$

Solving for D yields:

$$D = \frac{1}{1 + V_{IN} / V_{OUT}} \tag{24}$$

To avoid subharmonic oscillations, it is recommended that inductors L1 and L2 be the same inductance. Currents conducted by the inductors are:

$I_1 = I_{OUT}(V_{OUT}/V_{IN})$

$\Delta i_1 = V_{IN}D/(2*L1*fs)$

$I_2 = I_{OUT}$

$\Delta i_1 = V_{IN}D/(2*L2*fs)$

The switch sees a maximum current of $I_1 + I_2 + \Delta i_1 + \Delta i_2$. If L1 = L2 = L, the maximum switch current is given by:

$$I_{OUT}(1 + V_{OUT}/V_{IN}) + V_{IN}D/(L*fs) \tag{25}$$

The maximum load current is limited by this relationship to the switch current.

The polarity of C_{SEPIC} will change between each cycle, so a ceramic capacitor should be used here. A high quality, low ESR capacitor will directly improve efficiency because all the load current passes through C_{SEPIC}.

C_{IN} should be chosen using the same relationship as in the boost converter (see the C_{IN} section). C_{IN} must be able to provide the necessary RMS current.

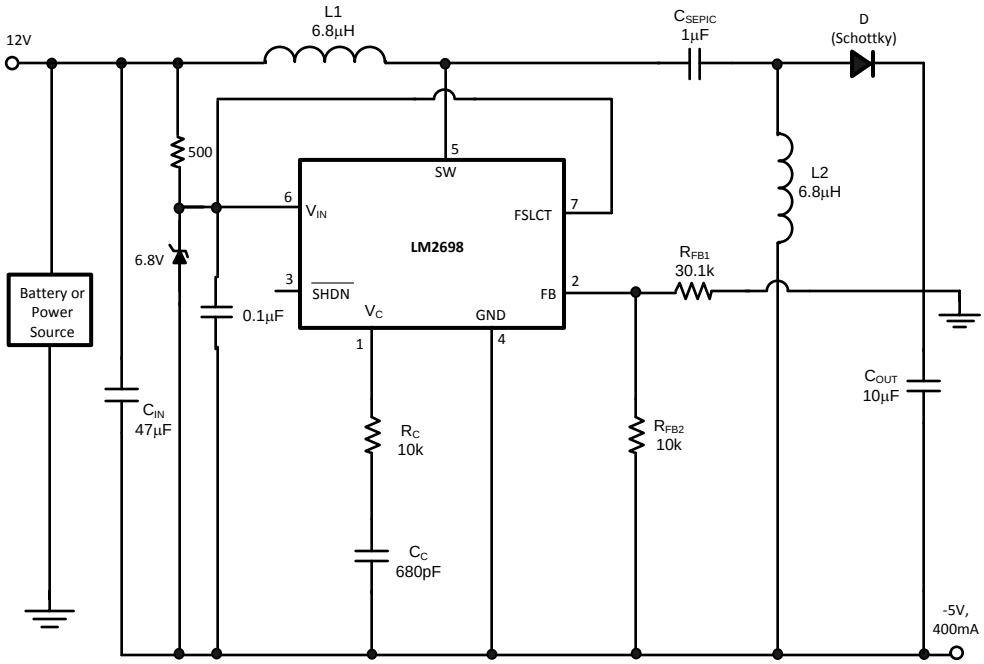


Figure 22. Level-Shifted SEPIC Converter

Level-Shifted SEPIC

The circuit shown in Figure 22 is similar to the SEPIC shown in Figure 21, except that it is level shifted to provide a negative output voltage. This is achieved by connecting the ground of the LM2698 to the output. The circuit analysis for the level-shifted SEPIC is the same as the SEPIC. The voltage at the input of the LM2698 will need to be clamped if the absolute value of the output voltage plus the input voltage exceeds 12V, the absolute maximum rating for the V_{IN} pin. The simplest way to do this is with a zener diode, as shown in Figure 22. Likewise, if the FSLCT pin is pulled high to operate at 1.25 MHz, its voltage must not exceed 12V. To prevent any high frequency noise from entering the LM2698's internal circuitry, a high frequency bypass capacitor must be placed as close to pin 6 as possible. A good choice for this capacitor is a 0.1µF ceramic capacitor.

Layout Consideration

The GND pin and the NC pin is recommended to be connected by a short trace as shown below.

Power Dissipation

The output power of the LM2698 is limited by its maximum power dissipation. The maximum power dissipation is determined by the formula

$$P_D = (T_{jmax} - T_A)/\theta_{JA} \quad (26)$$

where T_{jmax} is the maximum specified junction temperature (125°C), T_A is the ambient temperature, and θ_{JA} is the thermal resistance of the package. θ_{JA} is dependant on the layout of the board as shown below.

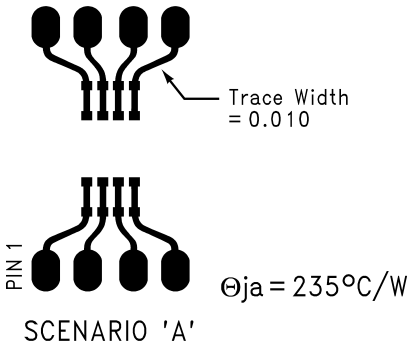


Figure 23.

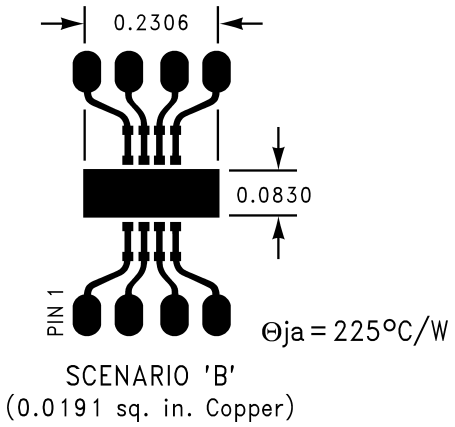


Figure 24.

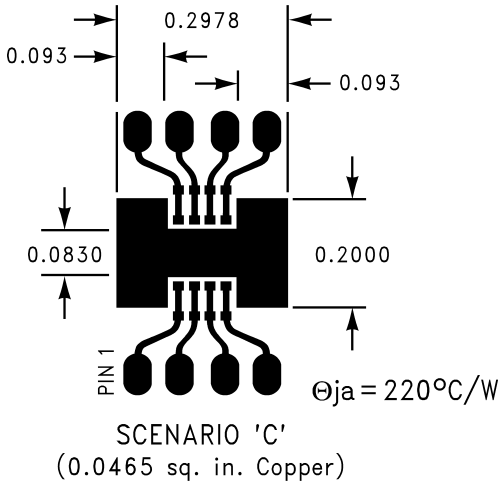


Figure 25.

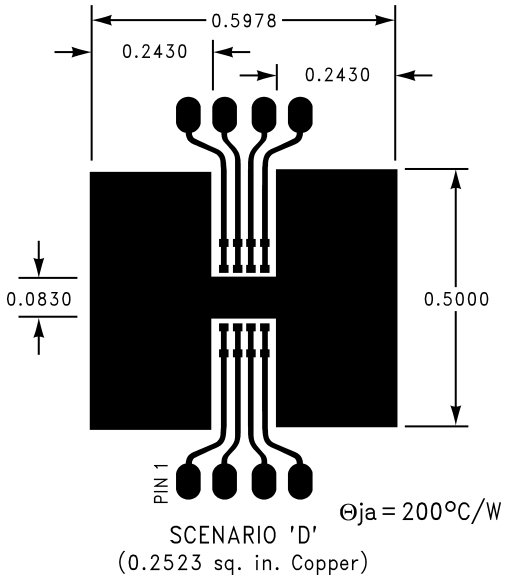


Figure 26.

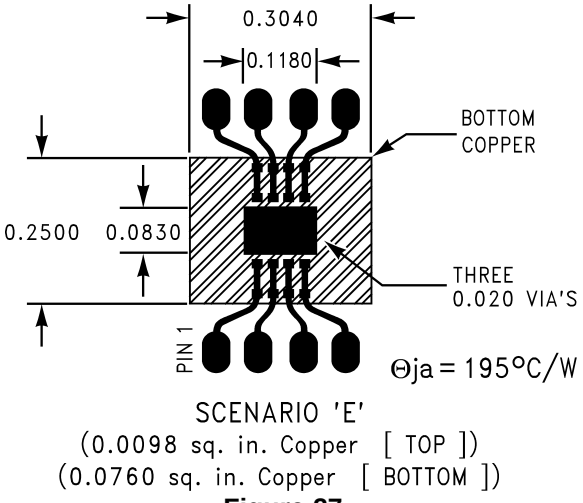


Figure 27.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2698MM-ADJ/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S22B	Samples
LM2698MMX-ADJ/NOPB	ACTIVE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	S22B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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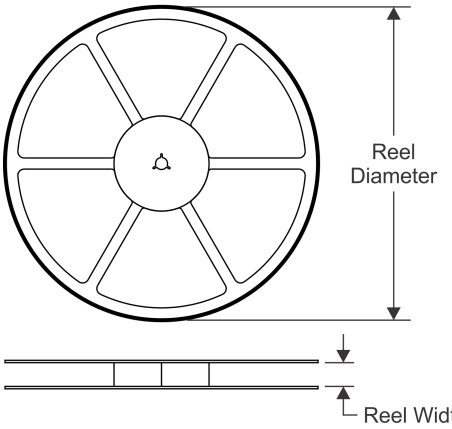
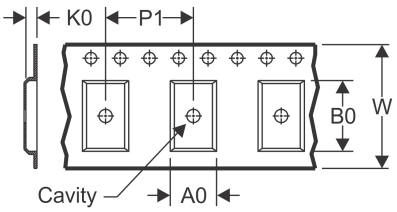
REEL DIMENSIONS

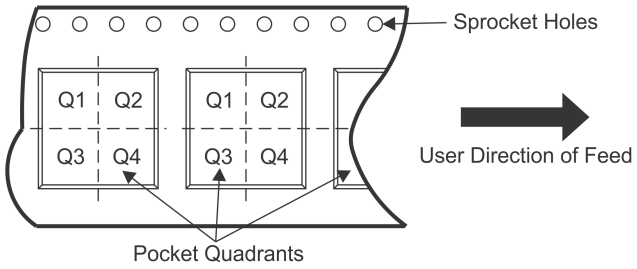


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

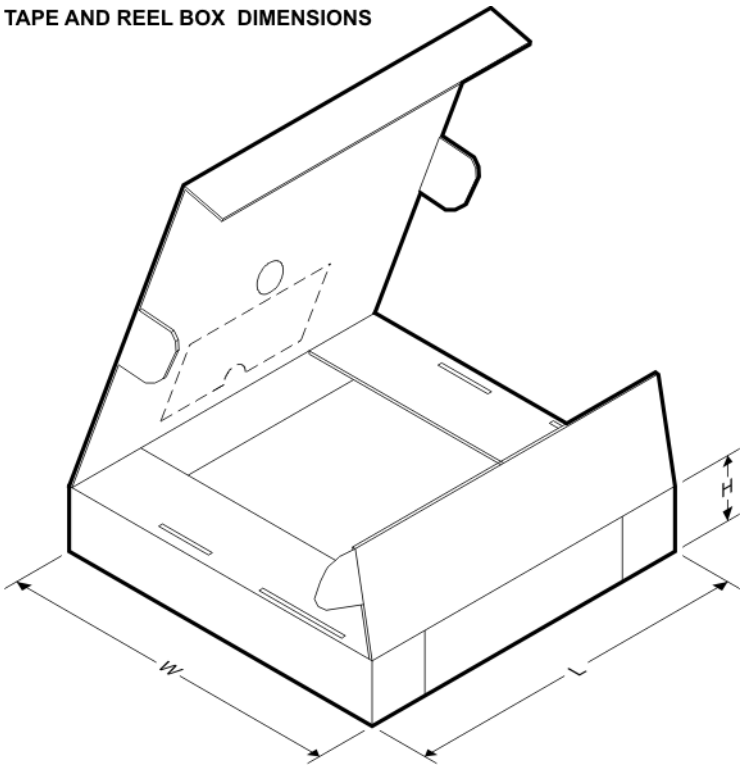
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2698MM-ADJ/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

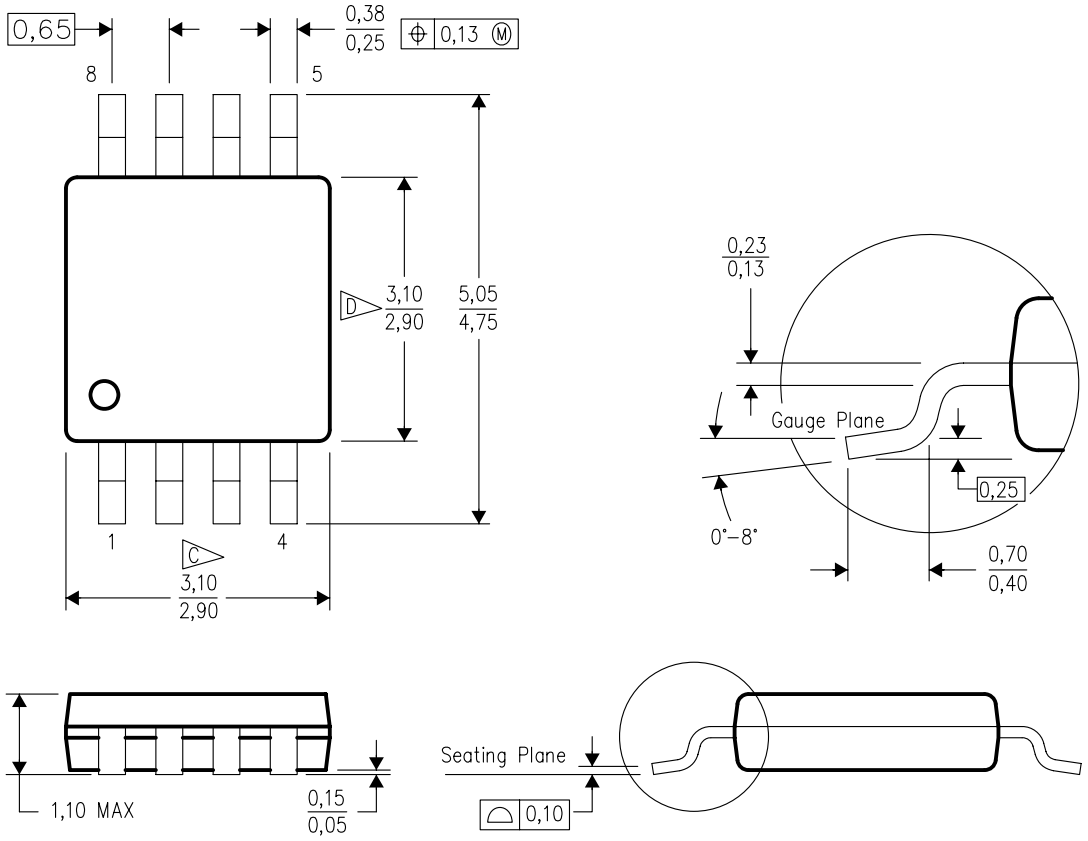
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2698MM-ADJ/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0

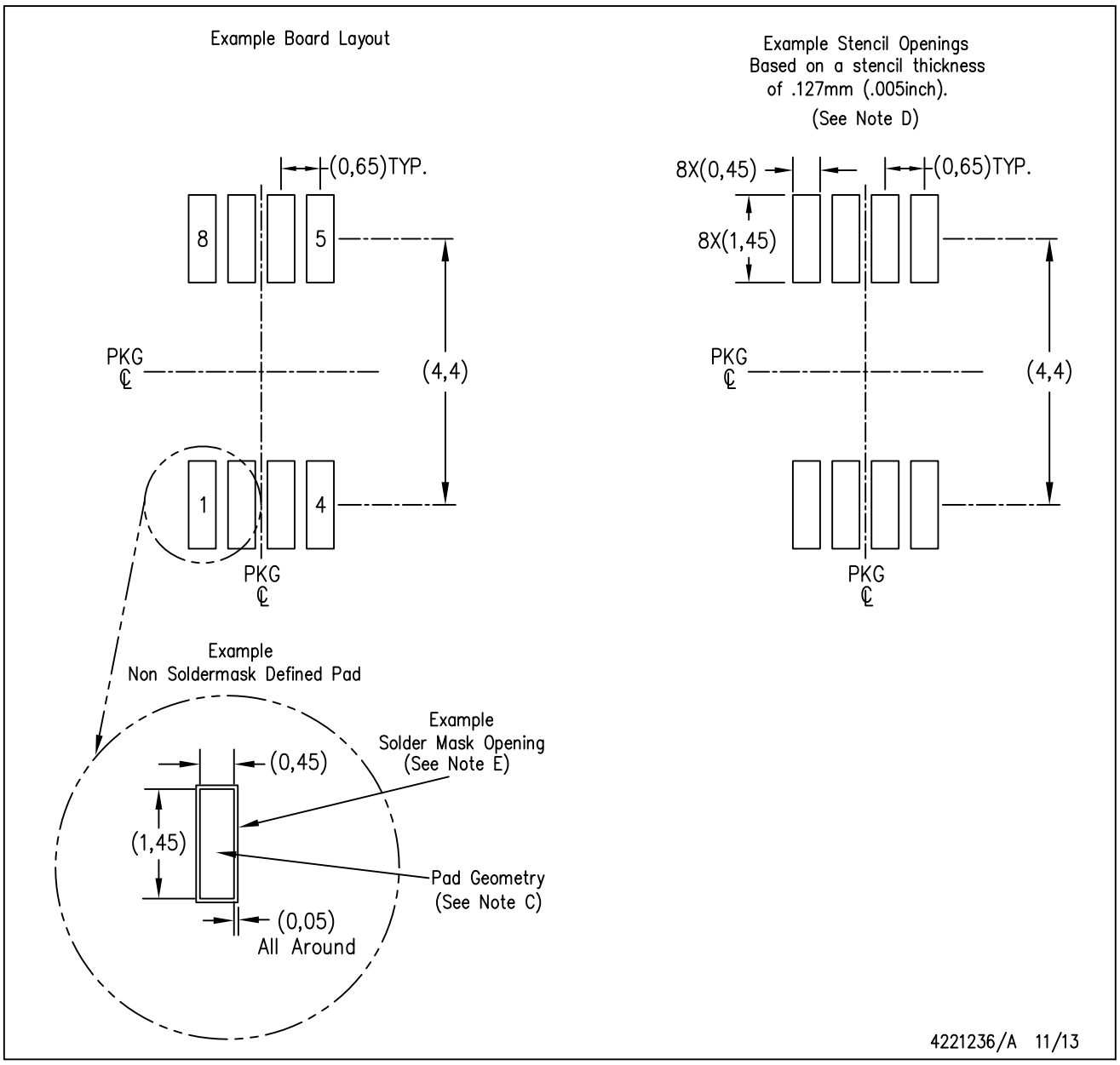
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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