BURR-BROWN®

PCM1717

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SoundPLUS Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

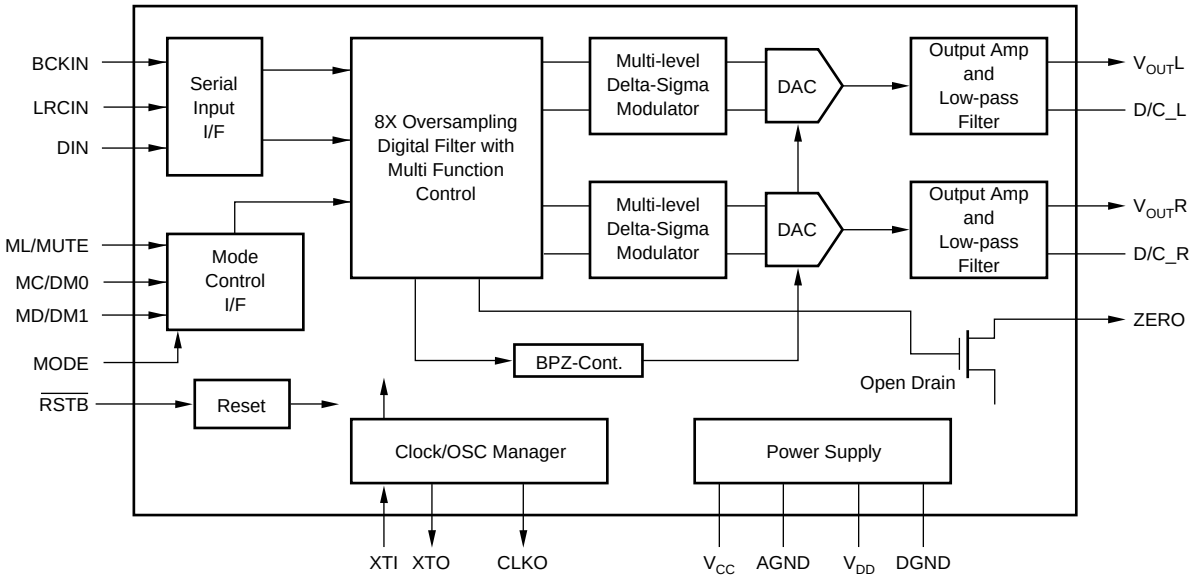
- ACCEPTS 16- OR 18-BIT INPUT DATA
- COMPLETE STEREO DAC:
  - 8X Oversampling Digital Filter
  - Multi-Level Delta-Sigma DAC
  - Analog Low Pass Filter
  - Output Amplifier
- HIGH PERFORMANCE:
  - –90dB THD+N
  - 96dB Dynamic Range
  - 100dB SNR
- SYSTEM CLOCK: 256fs or 384fs
- WIDE POWER SUPPLY: +2.7V to +5.5V
- SELECTABLE FUNCTIONS:
  - Soft Mute
  - Digital Attenuation (256 Steps)
  - Digital De-emphasis
  - Output Mode: L, R, Mono, Mute
- SMALL SSOP-20 PACKAGE

DESCRIPTION

The PCM1717 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1717 is fabricated on a highly advanced 0.6µ CMOS process. PCM1717 accepts 16- or 18-bit normal input data format, or 16- or 18-bit I^2S data format.

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, and digital de-emphasis. The digital filter features –35dB stop band attenuation and ±0.17dB ripple in the pass band.

PCM1717 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size, and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive, and CD-Karaoke systems.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SBAS038

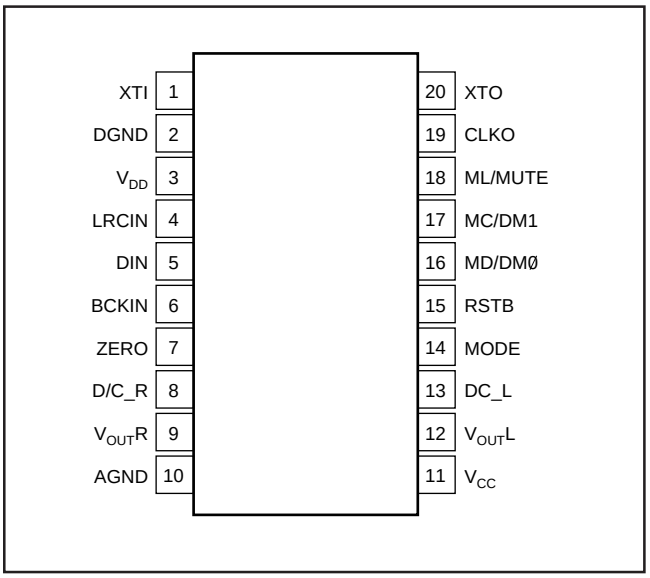
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, and 16-bit input data, SYSCLK = 384fs, unless otherwise noted. Measurement bandwidth is 20kHz.

PARAMETER	CONDITIONS	PCM1717E MIN	PCM1717E TYP	PCM1717E MAX	UNITS
RESOLUTION		16		18	Bits
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Input Logic Level:					
V_{IH}(2)		70% of V_{DD}			V
V_{IL}(2)				30% of V_{DD}	V
V_{IH}(3)		70% of V_{DD}			V
V_{IL}(3)				30% of V_{DD}	V
V_{IH}(4)		64% of V_{DD}			V
V_{IL}(4)				28% of V_{DD}	V
Input Logic Current:					
I_{IH}(5)				–6.0	µA
I_{IL}(5)				–120	µA
I_{IH}(6)				–2	µA
I_{IL}(6)				0.02	µA
I_{IH}(4)	V_{IN} = 3.2V			40	µA
I_{IL}(4)	V_{IN} = 1.4V			–40	µA
Output Logic Level: ($+V_{DD}$ = +5V)					
V_{OH}(7)	I_{OH} = –5mA	3.8			V
V_{OL}(7)	I_{OL} = +5mA			1.0	V
V_{OL}(8)	I_{OL} = +5mA			1.0	V
Interface Format			Selectable Normal, I²S		
Data Format			16/18 Bits MSB First Binary Two's Complement		
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	256fs/384fs	8.192/12.288	11.2896/16.9344	12.288/18.432	MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mismatch Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2 V_{CC} at Bipolar Zero		±30		mV
DYNAMIC PERFORMANCE(1)	V_{CC} = +5V, f = 991Hz				
THD+N at FS (0dB)			–90	–80	dB
THD+N at –60dB			–34		dB
Dynamic Range	EIAJ, A-weighted	90	96		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	92	100		dB
Channel Separation		90	97		dB
Level Linearity Error (–90dB)			±0.5		dB
DYNAMIC PERFORMANCE(1)	V_{CC} = +3V, f = 991Hz				
THD+N at FS (0dB)			–86		dB
Dynamic Range	EIAJ, A-weighted		91		dB
Signal-To-Noise Ratio	EIAJ, A-weighted		94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple				±0.17	dB
Stop Band Attenuation		–35			dB
Pass Band				0.445	fs
Stop Band		0.555			fs
De-emphasis Error	(fs = 32kHz ~ 48kHz)	–0.2		+0.55	dB
Delay Time (Latency)			11.125/fs		sec
ANALOG OUTPUT					
Voltage Range	FS (0dB) OUT		62% of V_{CC}		Vp-p
Load Impedance		5			kΩ
Center Voltage			50% of V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range:	$+V_{CC}$	+2.7		+5.5	VDC
	$+V_{DD}$	+2.7		+5.5	VDC
Supply Current: $+I_{CC}$ $+I_{DD}$(9)	$+V_{CC}$ = $+V_{DD}$ = +5V		18.0	25.0	mA
	$+V_{CC}$ = $+V_{DD}$ = +3V		9.0	15.0	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5V		90	125	mW
	$+V_{CC}$ = $+V_{DD}$ = +3V		27	45	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting. (2) Pins 4, 5, 6, 14: LRCIN, DIN, BCKIN, FORMAT. (3) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (Schmitt trigger input). (4) Pin 1: XTI. (5) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (if pull-up resistor is used). (6) Pins 4, 5, 6: LRCIN, DIN, BCKIN (if pull-up resistor is not used). (7) Pin 19: CLKO. (8) Pin 7: ZERO. (9) No load on pins 19 (CLKO) and 20 (XTO).

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	200mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

PIN	NAME	FUNCTION
Data Input Interface Pins		
4	LRCIN	Sample Rate Clock Input. Controls the update rate (fs).
5	DIN	Serial Data Input. MSB first, right justified (Sony format) or I²S (Philips). Contains a frame of 16- or 18-bit data.
6	BCKIN	Bit Clock Input. Clocks in the data present on DIN input.
Mode Control and Clock Signals		
1	XTI	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
14	MODE	Operation Mode Select. For Software Mode, tie Mode "HIGH". For Hardware Mode, tie Mode "LOW".
16	MD/DM0	Mode Control for Data Input or De-emphasis. When "HIGH" MD is selected, and a "LOW" selects DMØ.
17	MC/DM1	Mode Control for BCKIN or De-emphasis. When "HIGH", MC is selected, and a "LOW" selects DM1.
18	ML/MUTE	Mode Control for Strobe Clock or Mute. When "HIGH", ML is selected, and a "LOW" selects mute.
19	CLKO	Buffered Output of Oscillator. Equivalent to XTI.
20	XTO	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 1) of the crystal oscillator. When using an external clock, leave XTO open.
Operational Controls and Flags		
7	ZERO	Infinite Zero Detection Flag, open drain output. When the zero detection feature is muting the output, ZERO is "LOW". When non-zero input data is present, ZERO is in a high impedance state. When the input data is continuously zero for 65.536 BCKIN cycles, zero will be low.
15	RSTB	Resets DAC operation with an active "LOW" pulse.
Analog Output Functions		
8	D/C_R	Right Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
9	$V_{OUT}R$	Right Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
12	$V_{OUT}L$	Left Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
13	D/C_L	Left Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
Power Supply Connections		
2	DGND	Digital Ground.
3	V_{DD}	Digital Power Supply (+5V).
10	AGND	Analog Ground.
11	V_{CC}	Analog Power Supply (+3V).

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1717E	SSOP-20	334-1	–25°C to +85°C	PCM1717E	PCM1717E	Rails
"	"	"	"	"	PCM1717E/2K	Tape and Reel

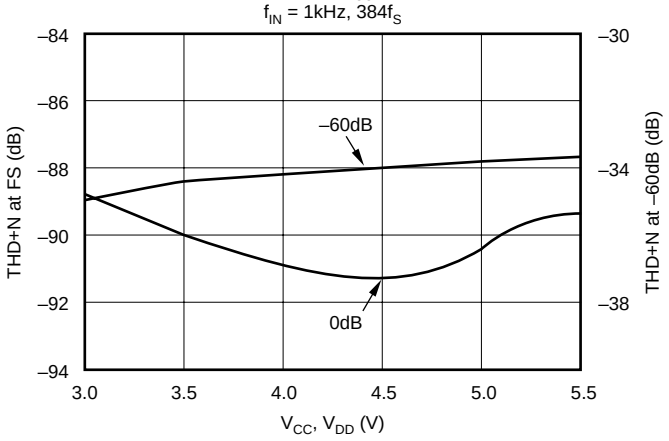
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1717E/2K" will get a single 2000-piece Tape and Reel.

TYPICAL PERFORMANCE CURVES

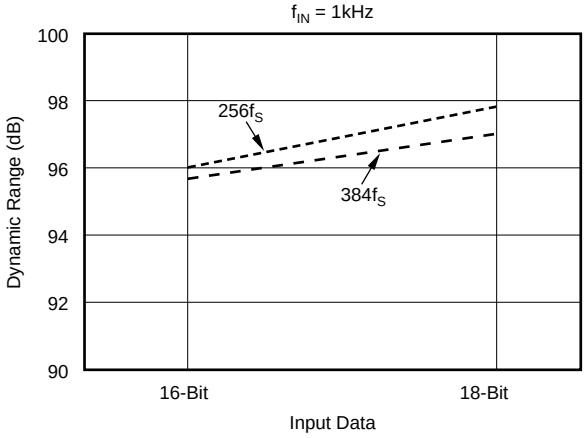
At T_A = +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, and 16-bit input data, SYSCLK = 384fs, unless otherwise noted.

DYNAMIC PERFORMANCE

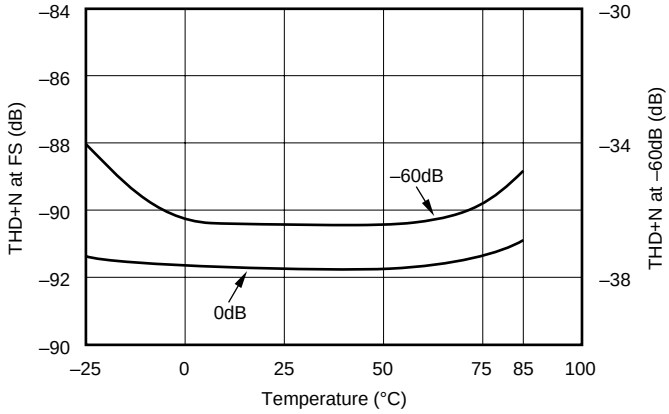
THD+N vs V_{CC}, V_{DD}
f_{IN} = 1kHz, 384f_S



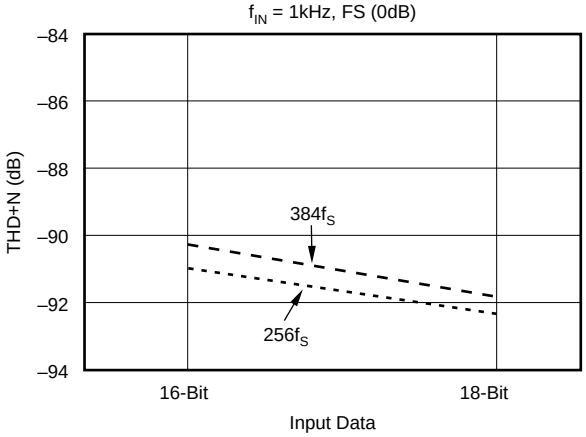
DYNAMIC RANGE vs INPUT DATA
f_{IN} = 1kHz



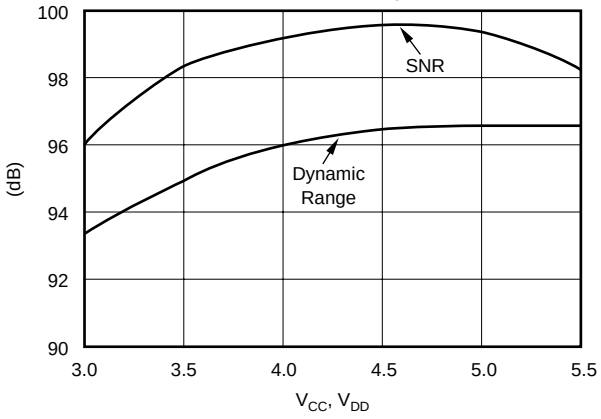
THD+N vs TEMPERATURE
f_{IN} = 1kHz, 384f_S



THD+N vs INPUT DATA
f_{IN} = 1kHz, FS (0dB)



DYNAMIC RANGE AND SNR vs V_{CC}, V_{DD}
f_{IN} = 1kHz, 384f_S

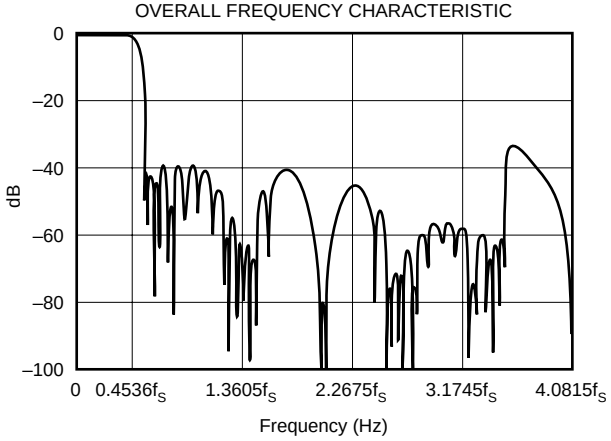


TYPICAL PERFORMANCE CURVES

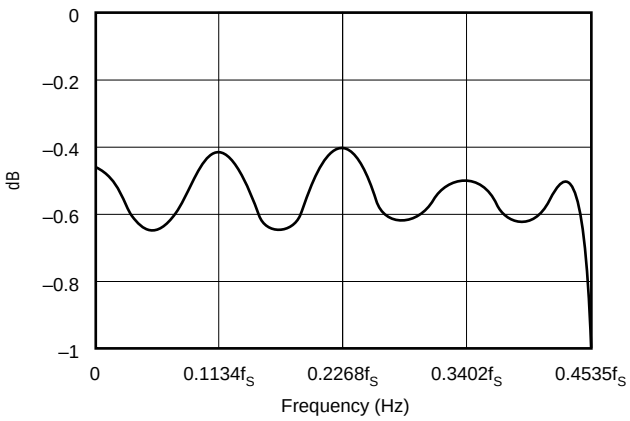
At T_A = +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, and 16-bit input data, SYSCLK = 384fs, unless otherwise noted.

DIGITAL FILTER

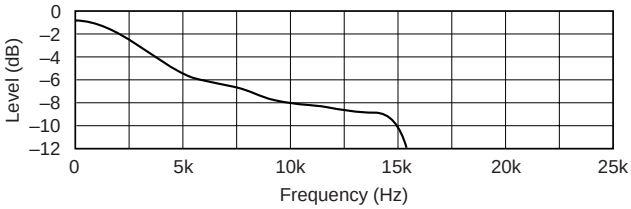
OVERALL FREQUENCY CHARACTERISTIC



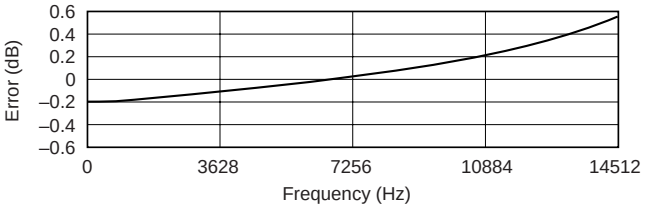
PASSBAND RIPPLE CHARACTERISTIC



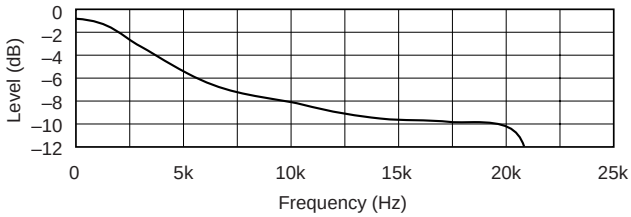
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



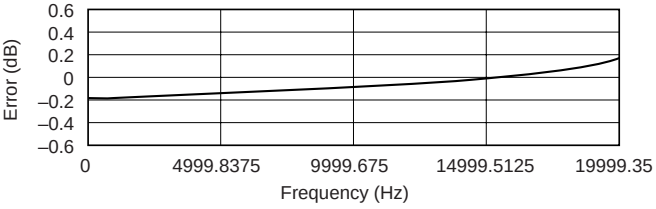
DE-EMPHASIS ERROR (32kHz)



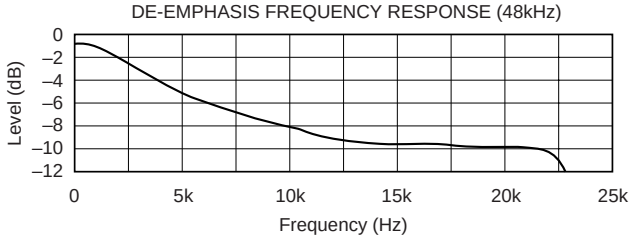
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



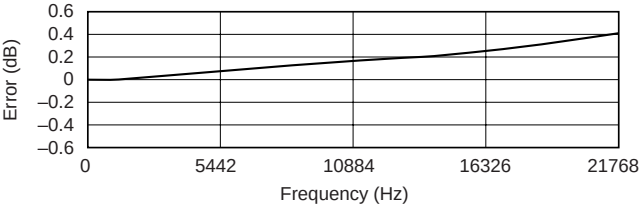
DE-EMPHASIS ERROR (44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



DE-EMPHASIS ERROR (48kHz)



SYSTEM CLOCK

The system clock for PCM1717 must be either $256f_S$ or $384f_S$, where f_S is the audio sampling frequency (typically 32kHz, 44.1kHz, or 48kHz). The system clock is used to operate the digital filter and the modulator.

The system clock can be either a crystal oscillator placed between XTI (pin 1) and XTO (pin 20), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1717 has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$ or $384f_S$. The system clock should be synchronized with LRCIN (pin 4) clock. LRCIN (left-right clock) operates at the sampling frequency fs. In the event these clocks are not synchronized, PCM1717 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6 bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1717 on pins 4, 5, and 6—LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1717 can accept both normal and I²S data formats. Normal data format is MSB first, two's complement, right-justified. I²S data is compatible with Philips serial data protocol. In the I²S format, the data is 16- or 18-bit, selectable by bit 0 on Register 3 (Software Control Mode). In the Hardware Mode, PCM1717 can only function with 16-bit normal data. Figures 5 through 9 illustrate timing and input formats.

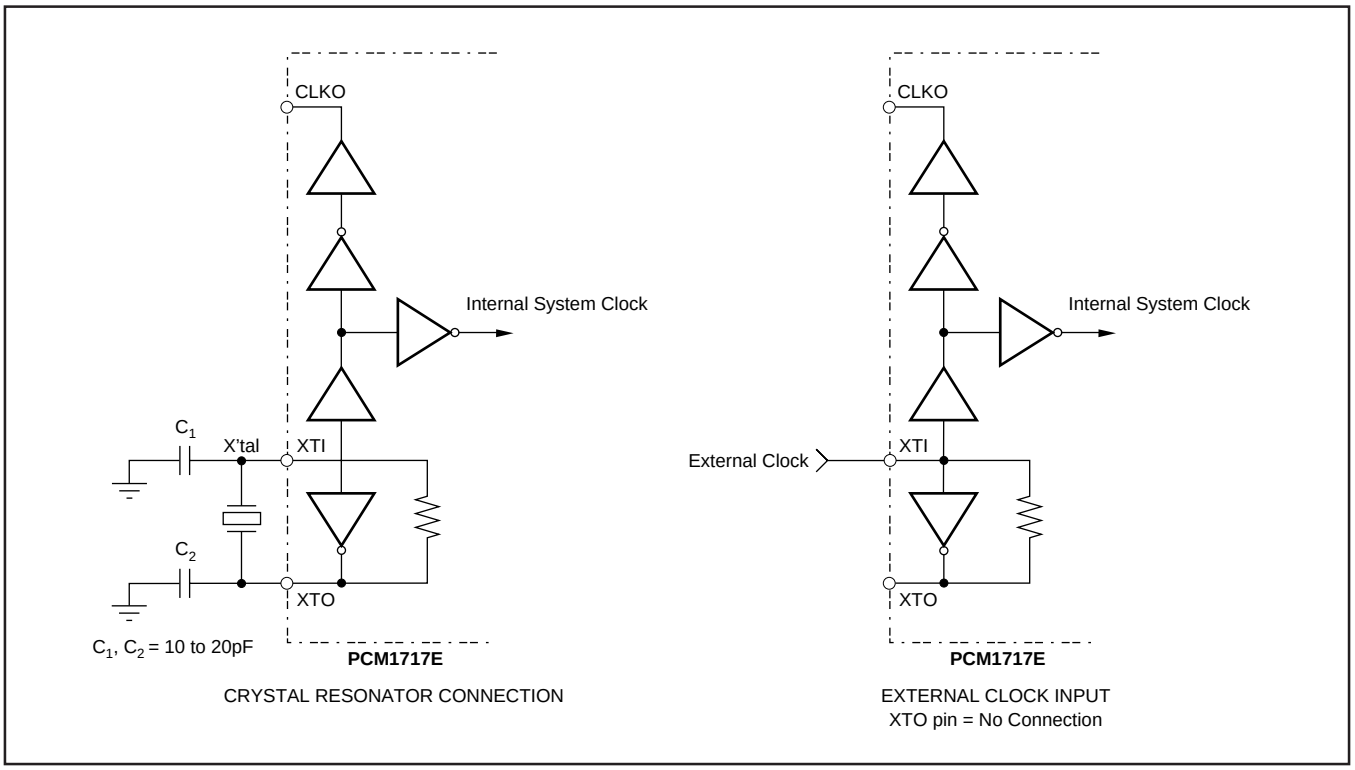
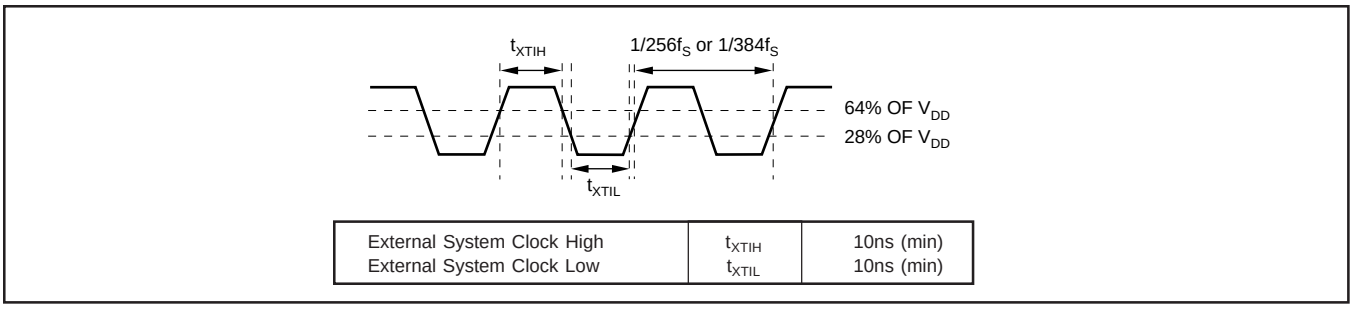


FIGURE 1. Internal Clock Circuit Diagram and Oscillator Connection.



External System Clock High	t_{XTIH}	10ns (min)
External System Clock Low	t_{XTIL}	10ns (min)

FIGURE 2. External Clock Timing Requirements.

Reset

PCM1717 has both internal power on reset circuit and the RSTB-pin (pin 15) which accepts external forced reset by RSTB = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 3 illustrates the timing of internal power on reset.

For the RSTB-pin, PSTB-pin accepts external forced reset by RSTB = L. During RSTB = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialize (1024 system clocks count after RSTB = H.) Figure 4 illustrates the timing of RSTB-pin reset.

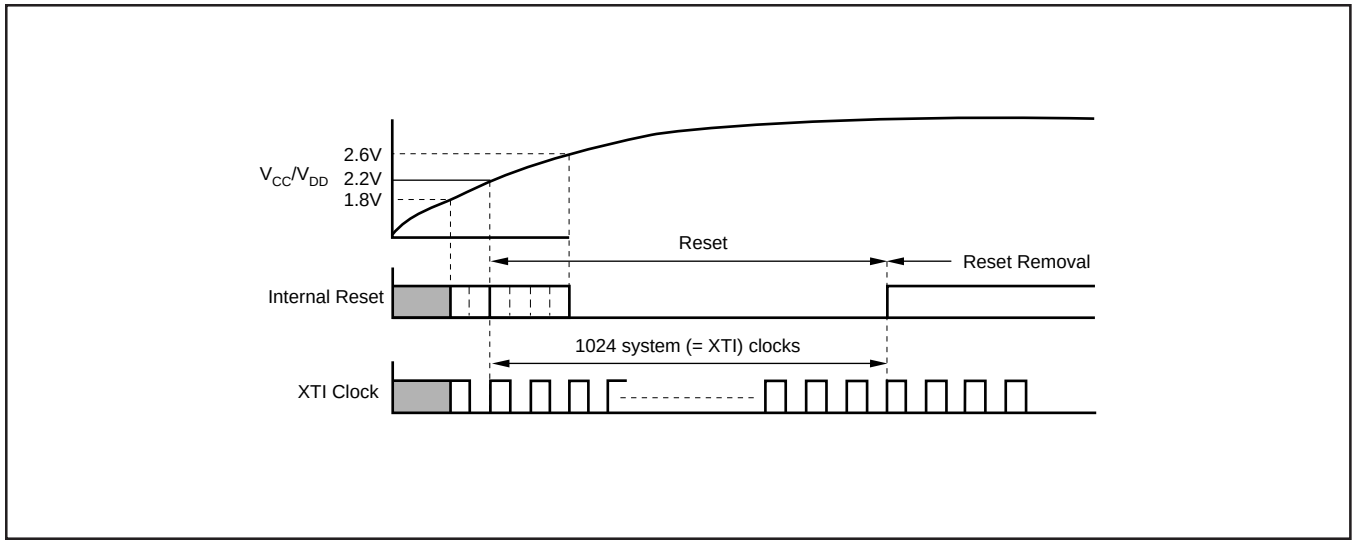


FIGURE 3. Internal Power-On Reset Timing.

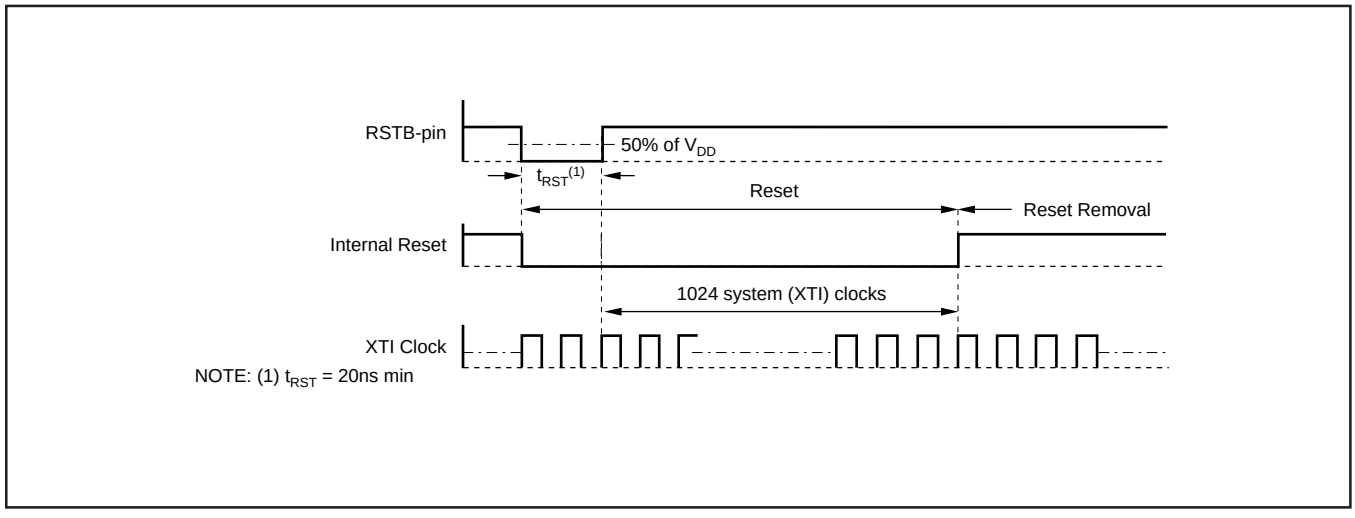


FIGURE 4. RSTB-Pin Reset Timing.

OPERATIONAL CONTROL

PCM1717 can be controlled in two modes. Software Mode allows the user to control operation with a 16-bit serial register. Hardware Mode allows the user to hard-wire operation of PCM1717 using four parallel wires. The MODE pin determines which mode PCM1717 is in; a LOW level on pin 14 places PCM1717 in Hardware Mode, and a HIGH on pin 14 places PCM1717 in Software Mode.

MODE (Pin 14)	Selected Mode	Pin 16	Pin 17	Pin 18
"HIGH"	Software Mode	MD	MC	ML
"LOW"	Hardware Mode	DM0	DM1	MUTE

Table I indicates which functions are selectable within the user's chosen mode. All of the functions shown are selectable in the Software Mode, but only soft mute and de-emphasis control may be selected in the Hardware Mode.

FUNCTION	SOFTWARE MODE SELECTABLE	DEFAULT	HARDWARE MODE SELECTABLE	DEFAULT
Input Data Format	Yes		No	
Normal Format		Normal	Normal Only	Normal
I^2S Format				
Input Resolution	Yes		No	
16 Bits		16 Bits	16 Bits Only	16 Bits
18 Bits				
LRCIN Polarity	Yes		No	
L/R = High/Low		L/R = H/L	L/R = H/L	L/R = H/L
L/R = Low/High			Only	
De-emphasis Control	Yes		Yes	
32kHz		OFF		OFF
44.1kHz				
48kHz				
OFF				
Soft Mute	Yes	OFF	Yes	OFF
Digital Attenuation	Yes	0dB	No	0dB
Analog Output Mode	Yes	Stereo	No	Stereo
Infinite Zero Detection	Yes	Disabled	No	Disabled
DAC Operation Control	Yes	ON	No	ON

TABLE I. Feature Selections by Mode.

HARDWARE MODE

(Pin 14 = "0")

This mode is controlled by logic levels present on pins 15, 16, 17 and 18. Hardware Mode allows for control of soft mute, digital de-emphasis and disable ONLY. Other functions such as attenuation, I/O format and infinite zero detect can only be controlled in the Software Mode.

SOFT MUTE (Pin 18)

A LOW level on pin 18 will force both channels to be muted; a HIGH level on pin 18 will allow for normal operation.

DIGITAL DE-EMPHASIS (Pins 16 and 17)

Pins 16 and 17 are used as a two-bit parallel register to control de-emphasis modes:

PIN 16	PIN 17	MODE
0	0	De-emphasis disabled
1	0	De-emphasis enabled at 48kHz
0	1	De-emphasis enabled at 44.1kHz
1	1	De-emphasis enabled at 32kHz

RESET MODE (Pin 15)

A LOW level on pin 15 will force the digital filters, modulators and mode controls into a reset (disable) mode. While this pin is held low, the output of PCM1717 will be forced to $V_{CC}/2$ (Bipolar Zero). Bringing pin 15 HIGH will initialize all DAC functions, and allow for normal operation.

SOFTWARE MODE

(Pin 14 = "1")

The Software Mode uses a three-wire interface on pins 16, 17 and 18. Pin 17 (MC) is used to clock in the serial control data, pin 18 (ML) is used to synchronize the serial control data, and pin 16 (MD) is used to latch in the serial control register. There are four distinct registers, with bits 9 and 10 (of 16) determining which register is in use.

REGISTER CONTROL (Bits 9, 10)

REGISTER	B9 (A0)	B10 (A1)
0	0	0
1	1	0
2	0	1
3	1	1

Control data timing is shown in Figure 6. ML is used to latch the data from the control registers. After each register's contents are checked in, ML should be taken low to latch in the data. A "res" in the register indicates that location is reserved for factory use. When loading the registers, the "res" bits should be set LOW.

REGISTER 0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0-7 (AL0-AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20\log_{10} (ATT\_DATA/255)]\ dB$$

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation. The attenuation level is given by:

ATT = 20log (y/256) (dB), where y = x, when $0 \le x \le 254$

y = x + 1, when x = 255

X is the user-determined step number, an integer value between 0 and 255.

Example:

let x = 255

$$ATT = 20\log\left(\frac{255+1}{256}\right) = 0\text{dB}$$

let x = 254

$$ATT = 20\log\left(\frac{254}{256}\right) = -0.068\text{dB}$$

let x = 1

$$ATT = 20\log\left(\frac{1}{256}\right) = -48.16\text{dB}$$

let x = 0

$$ATT = 20\log\left(\frac{0}{256}\right) = -\infty$$

REGISTER 1

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0-7 (AR0-AR7) control the level of attenuation.

REGISTER 2

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	res	res	res	res	IZD	OPE	DM1	DM0	MUTE

Register 2 is used to control soft mute, digital de-emphasis, disable, and infinite zero detect. Bit 0 is used for soft mute; a HIGH level on bit 0 will cause the output to be muted. Bits 1 and 2 are used to control digital de-emphasis as shown below:

BIT 1 (DM0)	BIT 2 (DM1)	DE-EMPHASIS
0	0	De-emphasis disabled
1	0	De-emphasis enabled at 48kHz
0	1	De-emphasis enabled at 44.1kHz
1	1	De-emphasis enabled at 32kHz

Bits 3 (OPE) and 4 (IZD) are used to control the infinite zero detection features. Tables II through IV illustrate the relationship between IZD, OPE, and RSTB (reset control):

	DATA INPUT	DAC OUTPUT
IZD = 1	Zero	Forced to BPZ(1)
	Other	Normal
IZD = 0	Zero	Zero(2)
	Other	Normal

TABLE II. Infinite Zero Detection (IZD) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
OPE = 1	Zero	Forced to BPZ(1)	Enabled
	Other	Forced to BPZ(1)	Enabled
OPE = 0	Zero	Controlled by IZD	Enabled
	Other	Normal	Enabled

TABLE III. Output Enable (OPE) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
RSTB = "HIGH"	Zero	Controlled by OPE and IZD	Enabled
	Other	Controlled by OPE and IZD	Enabled
RSTB = "LOW"	Zero	Forced to BPZ(1)	Disabled
	Other	Forced to BPZ(1)	Disabled

TABLE IV. Reset (RSTB) Function.

NOTE: (1) ΔΣ is disconnected from output amplifier. (2) ΔΣ is connected to output amplifier.

OPE controls the operation of the DAC: when OPE is "LOW", the DAC will convert all non-zero input data. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will only be forced to zero only if IZD is "HIGH". When OPE is "HIGH", the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IZD controls the operation of the zero detect feature: when IZD is "LOW", the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is "HIGH", the zero detect feature is enabled. If the input data is continuously zero for 65,536 cycle of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1717 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

REGISTER 3

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	res	PL3	PL2	PL1	PL0	ATC	IW	LRP	IIS

Register 3 is used to select the I/O data formats. Bit 0 (IIS) is used to control the input data format. If the input data source is normal (16- or 18-bit, MSB first, right-justified), set bit 0 "LOW". If the input format is IIS, set bit 0 "HIGH".

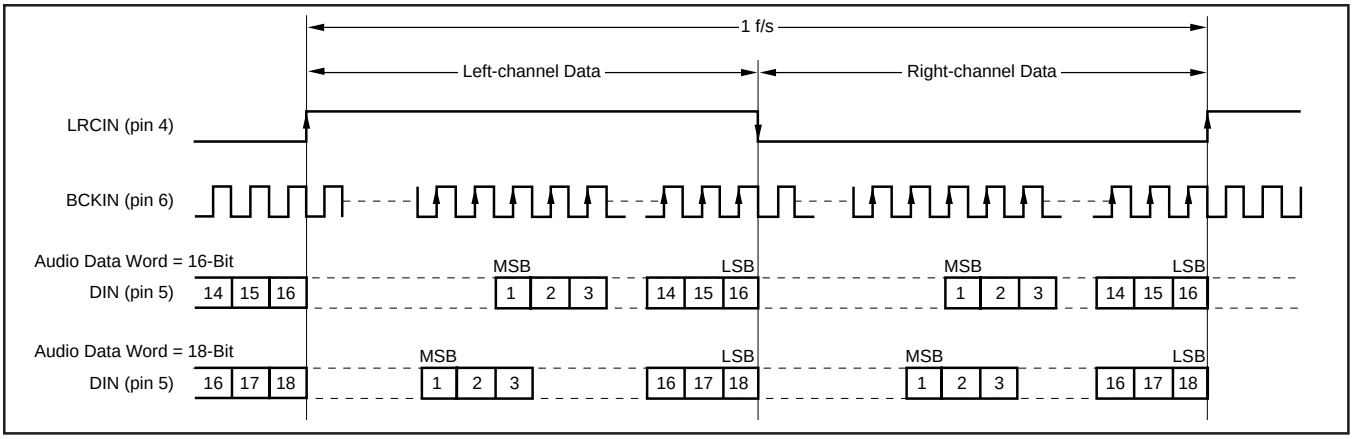


FIGURE 5. “Normal” Data Input Timing.

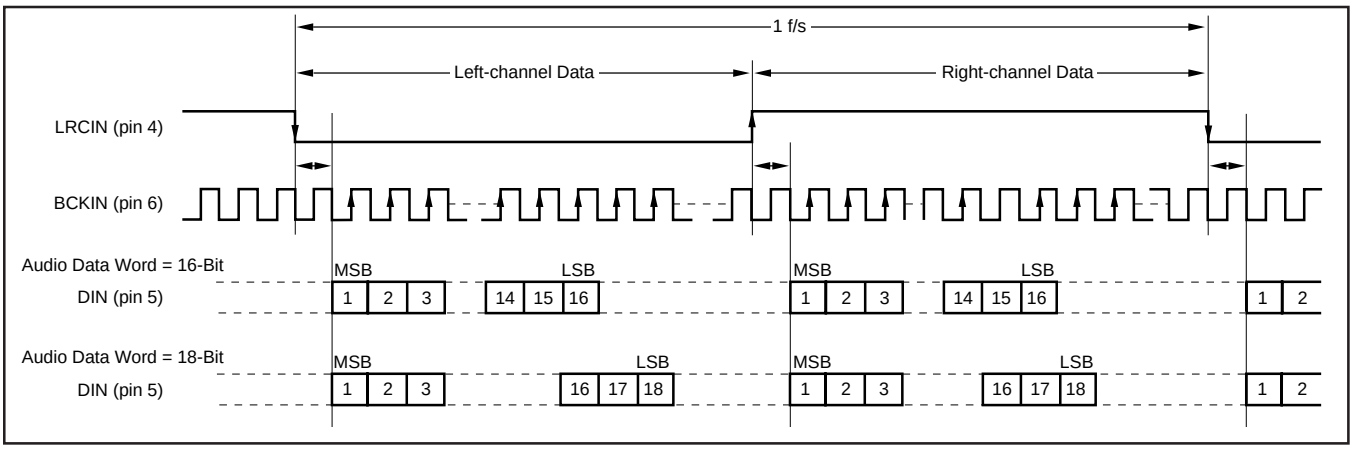
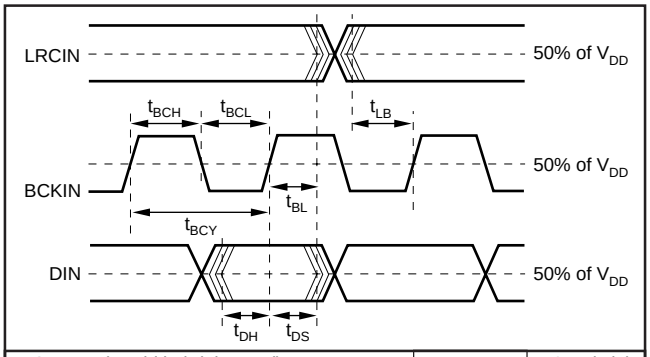


FIGURE 6. “I²S” Data Input Timing.



BCKIN Pulsewidth (High Level)	t_{BCH}	50ns (min)
BCKIN Pulsewidth (Low Level)	t_{BCL}	50ns (min)
BCKIN Pulse Cycle Time	t_{BCY}	100ns (min)
BCKIN Rising Edge → LRCIN Edge	t_{BL}	30ns (min)
LRCIN Edge → BCKIN Rising Edge	t_{LB}	30ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)

FIGURE 7. Data Input Timing.

Bit 1 is used to select the polarity of LRCIN (sample rate clock). When bit 1 is LOW, a HIGH state on LRCIN is used for the left channel, and a LOW state on LRCIN is used for the right channel. When bit 1 is HIGH the polarity of LRCIN is reversed.

Bit 2 is used to select the input word length. When bit 2 is LOW, the input word length is set for 16 bits; when bit 2 is HIGH, the input word length is set for 18 bits.

Bit 3 is used as an attenuation control. When bit 3 is set HIGH, the attenuation data on Register 0 is used for both channels, and the data in Register 1 is ignored. When bit 3 is LOW, each channel has separate attenuation data.

Bits 4 through 7 are used to determine the output format, as shown in Table V:

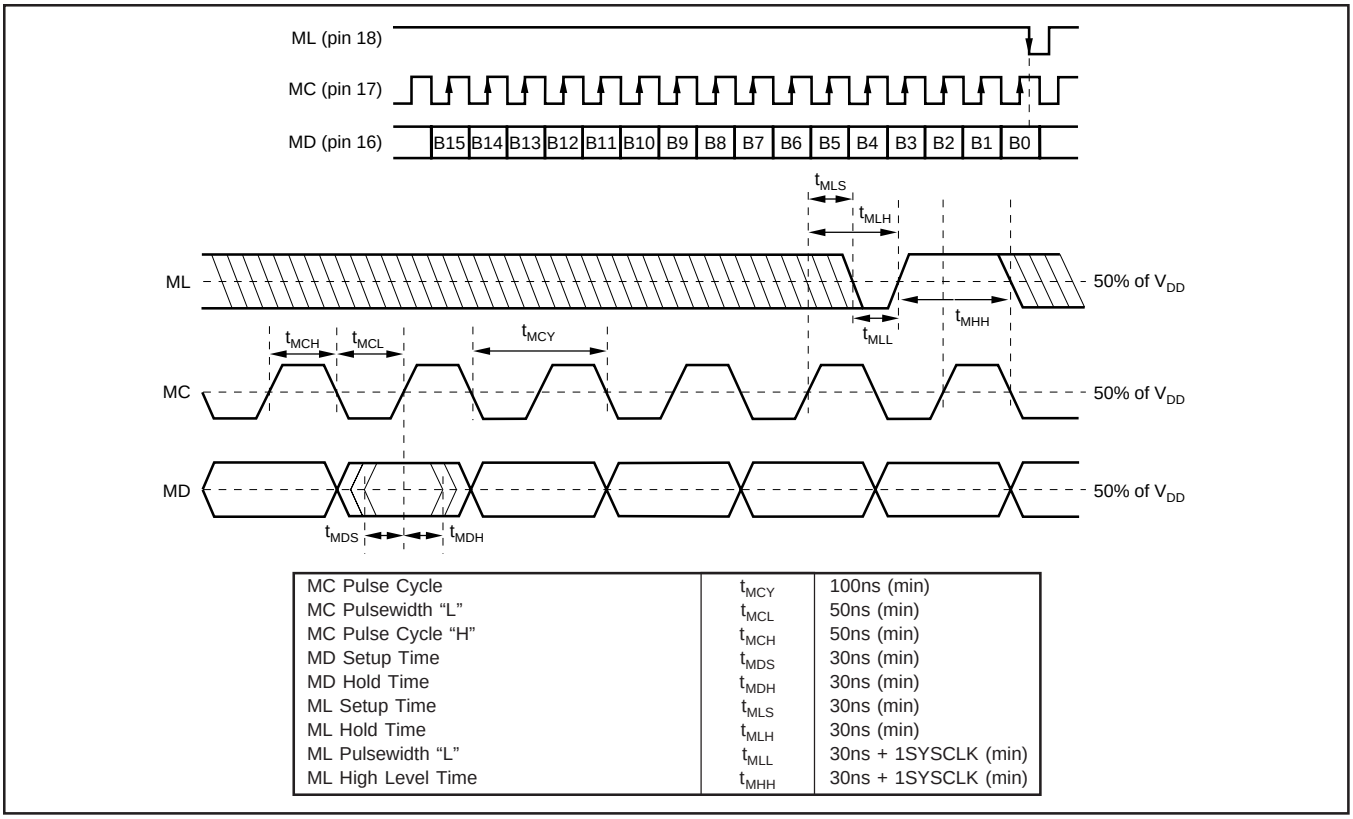
PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE V. PCM1717 Output Mode Control.

REGISTER RESET STATES

After reset, each register is set to a predetermined state:

Register 0	0000 0000 1111 1111
Register 1	0000 0010 1111 1111
Register 2	0000 0100 0000 0000
Register 3	0000 0110 1001 0000



MC Pulse Cycle	t_{MCY}	100ns (min)
MC Pulsewidth “L”	t_{MCL}	50ns (min)
MC Pulse Cycle “H”	t_{MCH}	50ns (min)
MD Setup Time	t_{MDS}	30ns (min)
MD Hold Time	t_{MDH}	30ns (min)
ML Setup Time	t_{MLS}	30ns (min)
ML Hold Time	t_{MLH}	30ns (min)
ML Pulsewidth “L”	t_{MLL}	30ns + 1SYSCLK (min)
ML High Level Time	t_{MHH}	30ns + 1SYSCLK (min)

FIGURE 8. Control Data Timing in Software Mode Control.

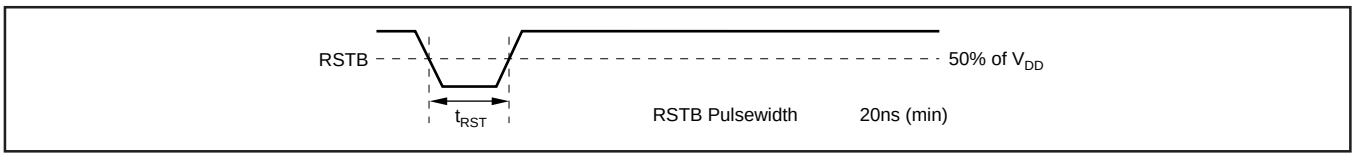


FIGURE 9. External Reset Timing.

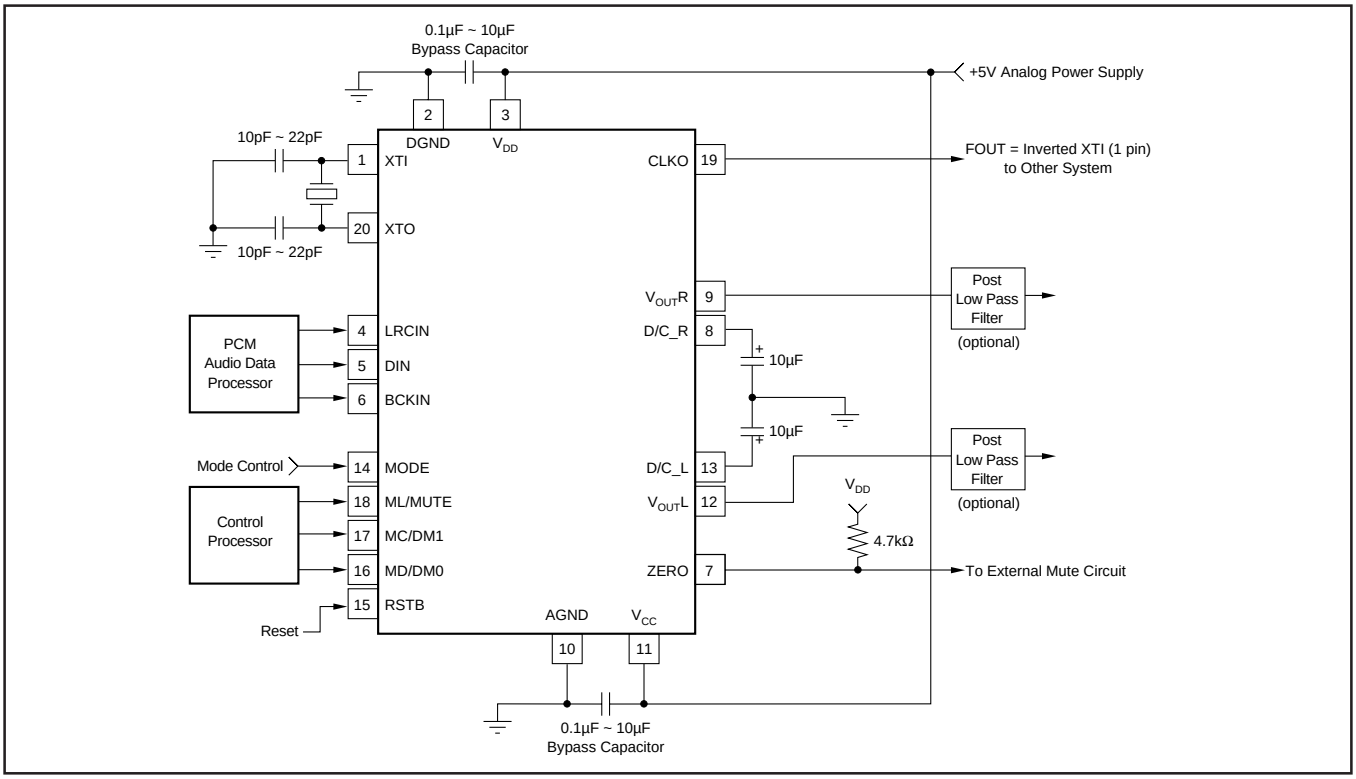


FIGURE 10. Typical Connection Diagram of PCM1717.

POWER SUPPLY CONNECTIONS

PCM1717 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 11.

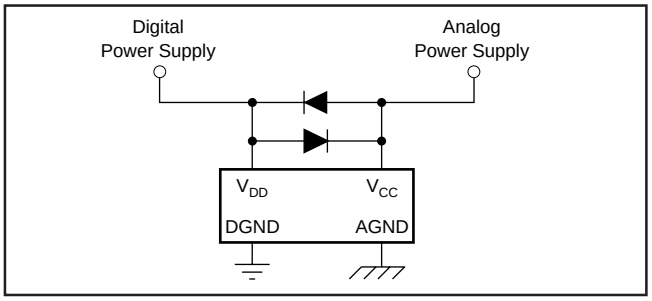


FIGURE 11. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 10 for optimal values of bypass capacitors.

THEORY OF OPERATION

The delta-sigma section of PCM1717 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 12. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $48f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 13.

Multi Level
Delta Sigma

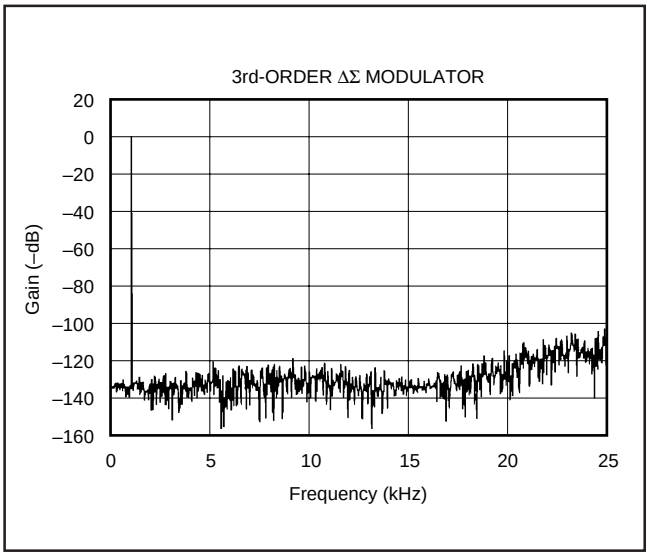


FIGURE 13. Quantization Noise Spectrum.

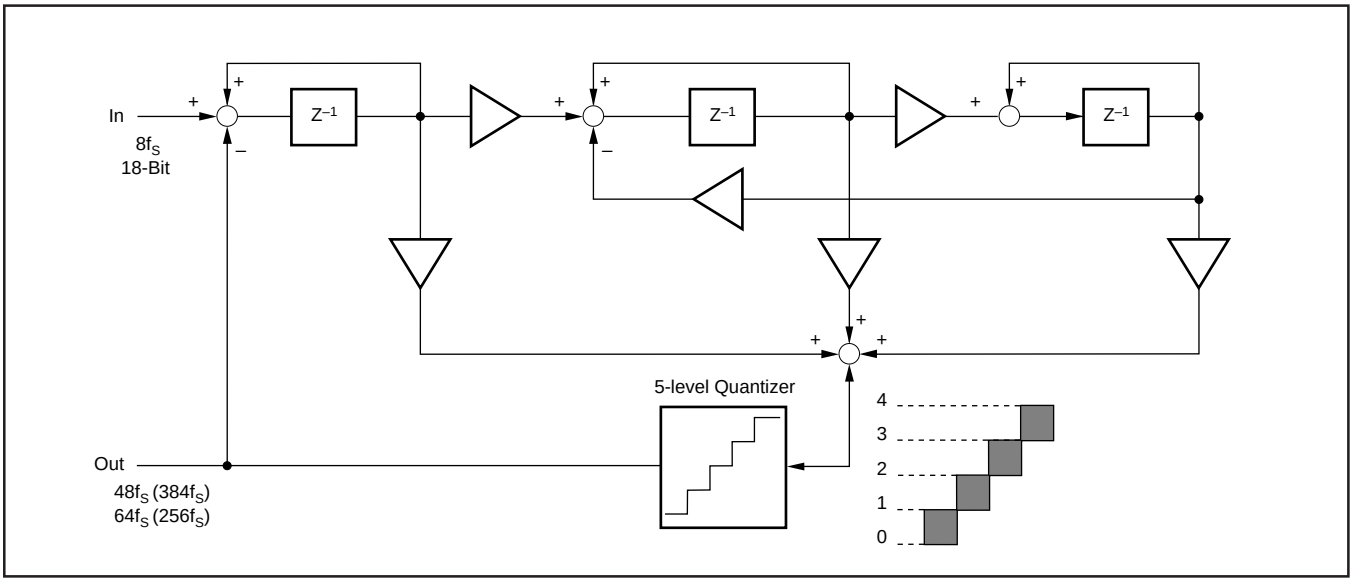


FIGURE 12. 5-Level ΔΣ Modulator Block Diagram.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1717:

$$T_D = 11.125 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 11.125/44.1kHz = 251.4µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

INTERNAL RESET

When power is first applied to PCM1717, an automatic reset function occurs after 1,024 cycles of XTI clock. Refer to Table I for default conditions. During the first 1,024 cycles of XTI clock, PCM1717 cannot be programmed (Software Control). Data can be loaded into the control registers during this time, and after 1,204 cycles of XTI clock, a "LOW" on ML (pin 18) will initiate programming.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1717 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 14. The higher frequency rolloff of the filter is shown in Figure 15. If the user's application has the PCM1717 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 16. For some applications, a passive RC filter or 2nd-order filter may be adequate.

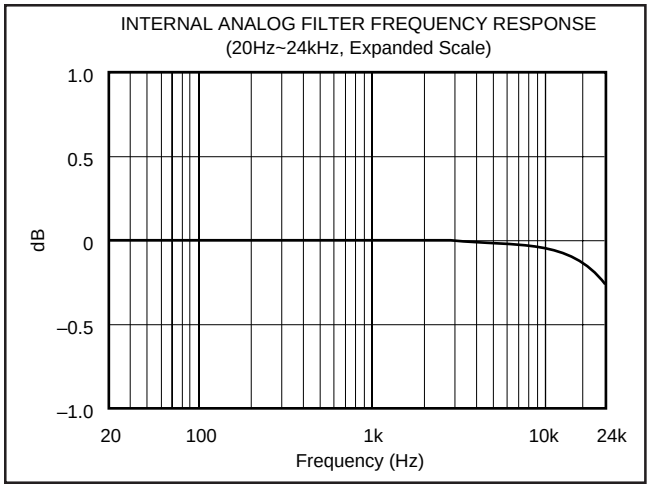


FIGURE 14. Low Pass Filter Frequency Response.

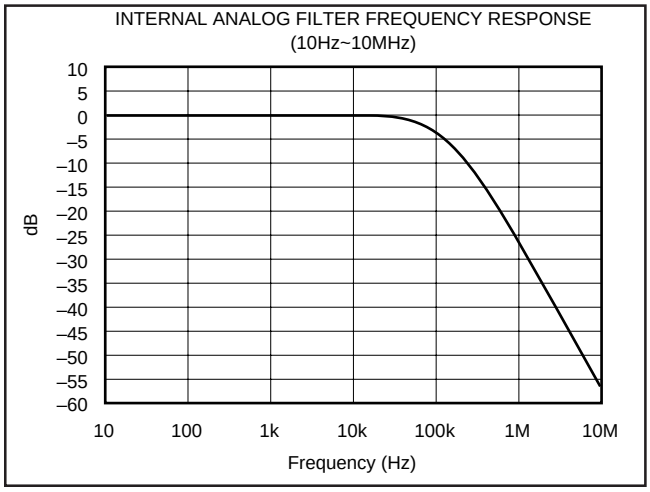


FIGURE 15. Low Pass Filter Frequency Response.

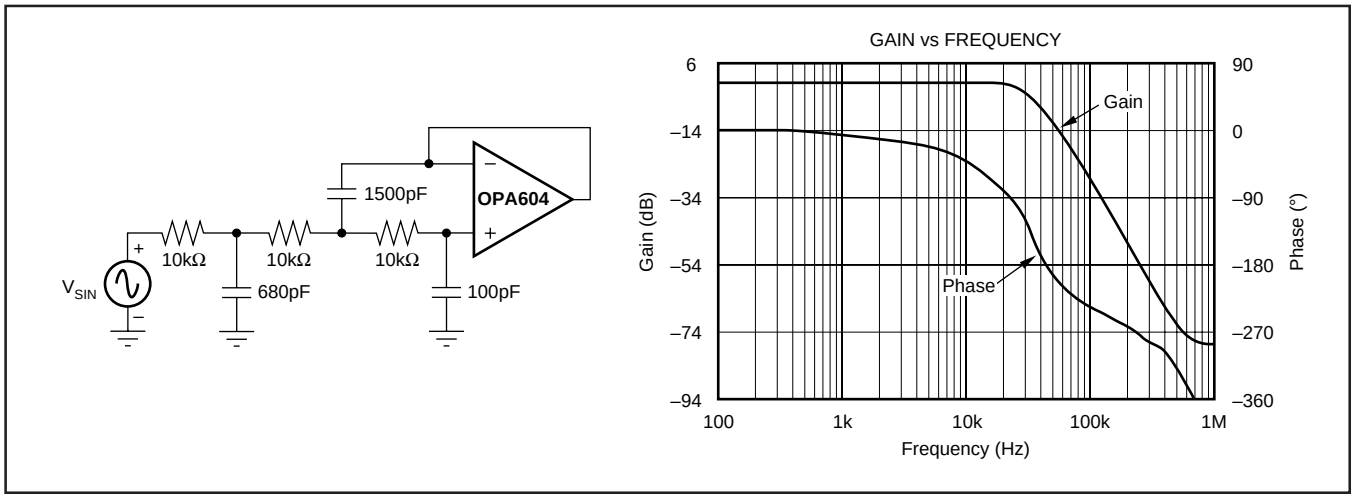


FIGURE 16. 3rd-Order LPF.

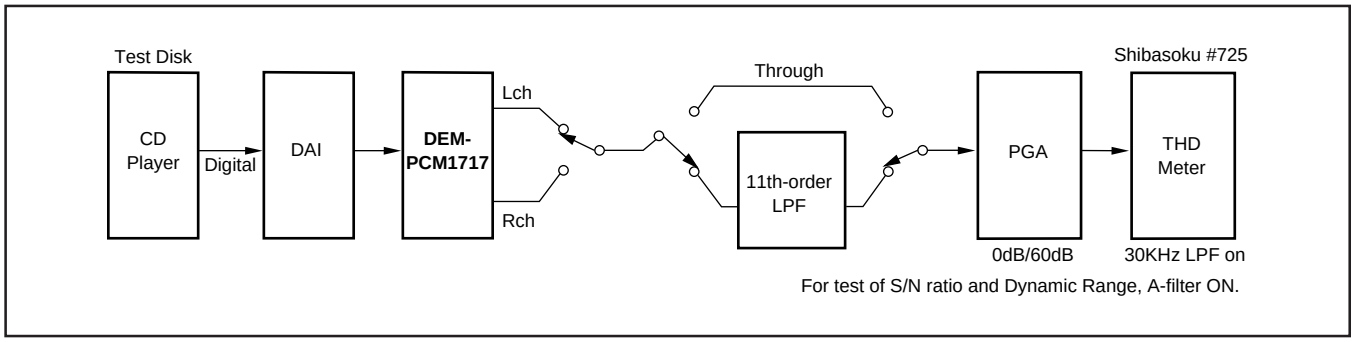


FIGURE 17. Test Block Diagram.

TEST CONDITIONS

Figure 17 illustrates the actual test conditions applied to PCM1717 in production. The 11th-order filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the 3rd-order filter shown in Figure 16 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –89dB when the external 20kHz 11th-order filter is used.

EVALUATION FIXTURES

Three evaluation fixtures are available for PCM1717.

DEM-PCM1717

This evaluation fixture is primarily intended for quick evaluation of the PCM1717's performance. DEM-PCM1717 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1717 does not contain a receiver chip or an external low pass filter. DEM-PCM1717 requires a single +5V power supply.

OUT-OF-BAND NOISE CONSIDERATIONS

Delta-sigma DACs are by nature very sensitive to jitter on the master clock. Phase noise on the clock will result in an increase in noise, ultimately degrading dynamic range. It is difficult to quantify the effect of jitter due to problems in synthesizing low levels of jitter. One of the reasons delta-sigma DACs are prone to jitter sensitivity is the large quantization noise when the modulator can only achieve two discrete output levels (0 or 1). The multi-level delta-sigma DAC has improved theoretical SNR because of multiple output states. This reduces sensitivity to jitter. Figure 18 contrasts jitter sensitivity between a one-bit PWM type DAC and multi-level delta-sigma DAC. The data was derived using a simulator, where clock jitter could be completely synthesized.

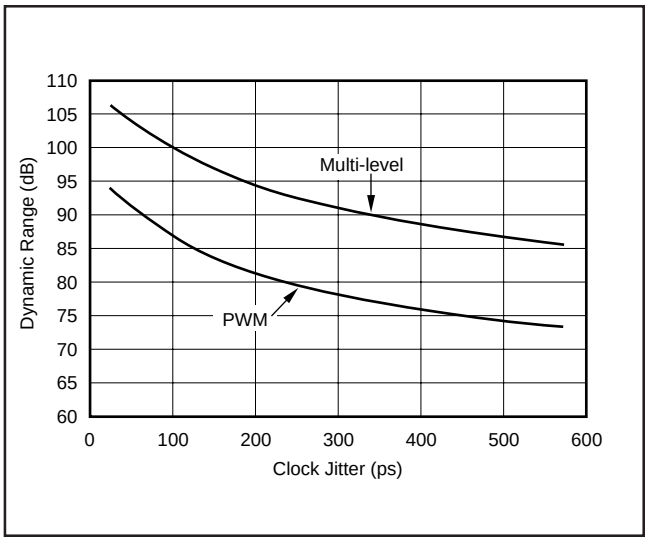


FIGURE 18. Simulation Results of Clock Jitter Sensitivity.

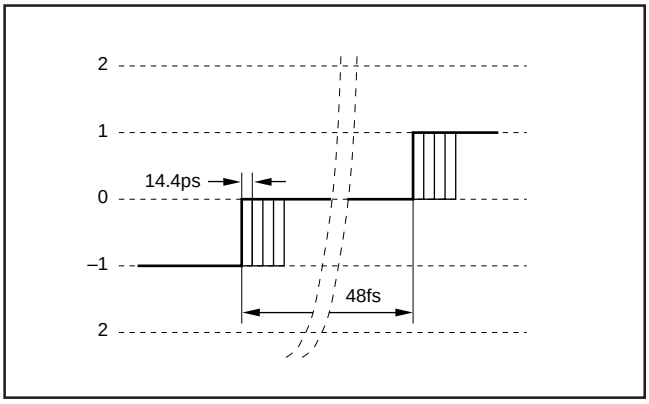


FIGURE 19. Simulation Method for Clock Jitter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PCM1717E	NRND	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1717E-3	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
PCM1717E-3G4	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
PCM1717E/2K	NRND	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1717E/2KG4	NRND	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1717EG	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
PCM1717EG4	NRND	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1717EGE6	NRND	SSOP	DB	20		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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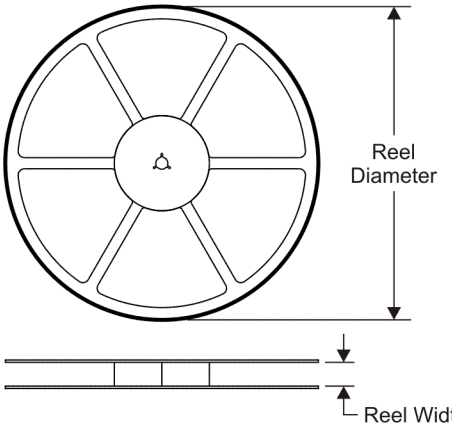
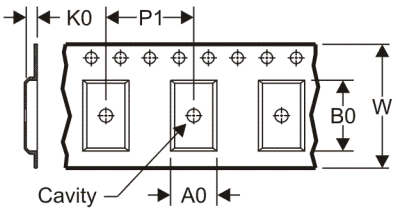
REEL DIMENSIONS

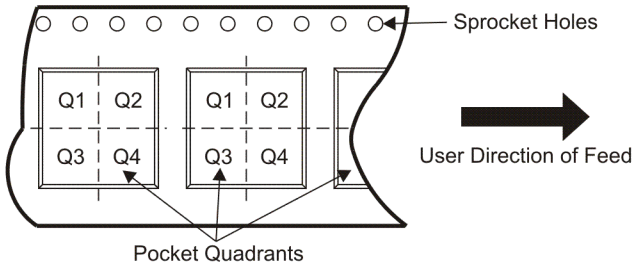


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

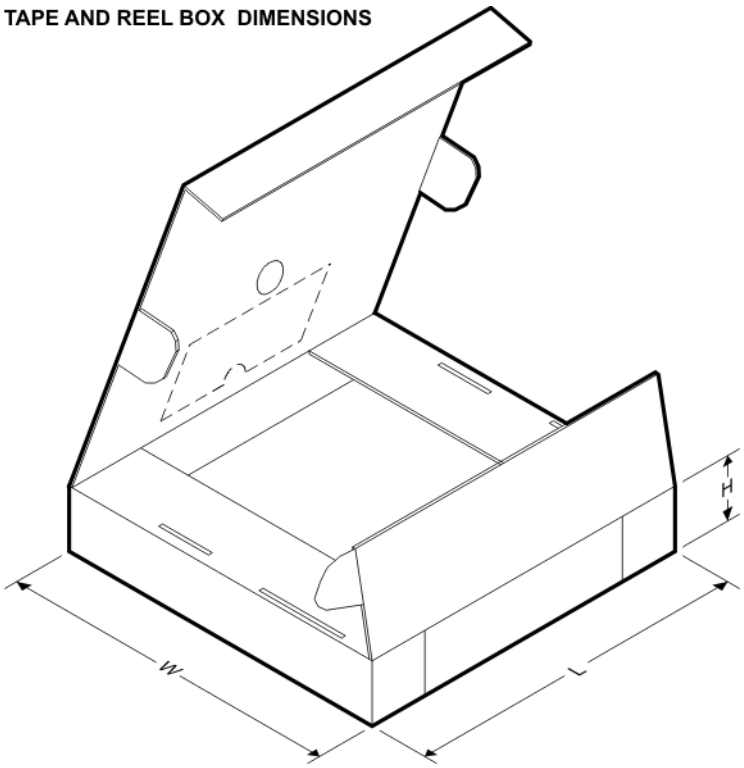
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1717E/2K	SSOP	DB	20	2000	330.0	17.4	8.5	7.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1717E/2K	SSOP	DB	20	2000	336.6	336.6	28.6

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