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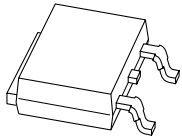
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Kind regards,

Team Nexperia



PHD38N02LT

N-channel TrenchMOS logic level FET

Rev. 02 — 2 February 2007

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low on-state resistance
- 2.5 V gate drive

1.3 Applications

- Linear regulator for Double-Data Rate (DDR) memory

1.4 Quick reference data

- $V_{DS} \leq 20\text{ V}$
- $I_D \leq 44.7\text{ A}$
- $R_{DS(on)} \leq 16\text{ m}\Omega$
- $P_{tot} \leq 57.6\text{ W}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	SOT428 (DPAK)	mbb076
2	drain (D) [1]		
3	source (S)		
mb	mounting base; connected to drain (D)		

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 2. Ordering information

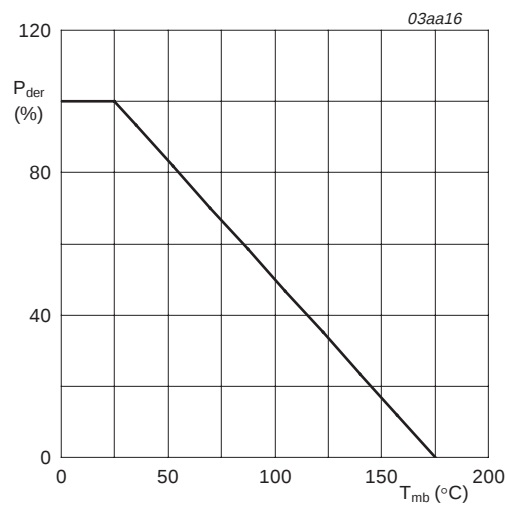
Type number	Package		
	Name	Description	Version
PHD38N02LT	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 3. Limiting values

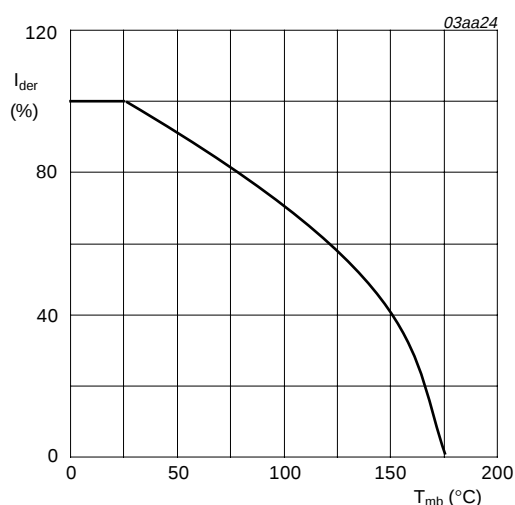
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_J \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage		-	± 12	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 2 and 3	-	44.7	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 2	-	31.6	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	179	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	57.6	W
T_{stg}	storage temperature		-55	+175	°C
T_J	junction temperature		-55	+175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	44.7	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	179	A



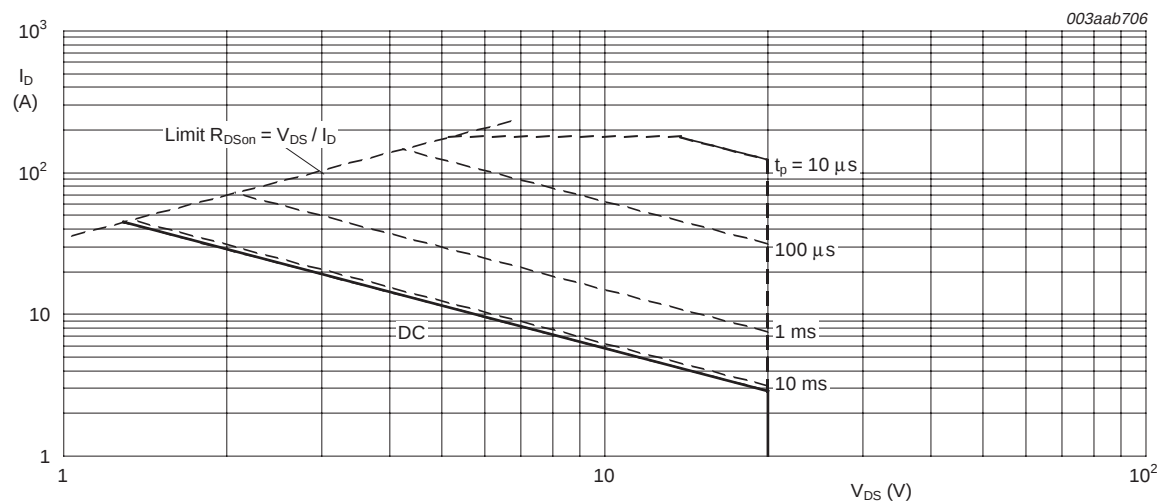
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25$ °C; I_{DM} is single pulse; $V_{GS} = 5$ V

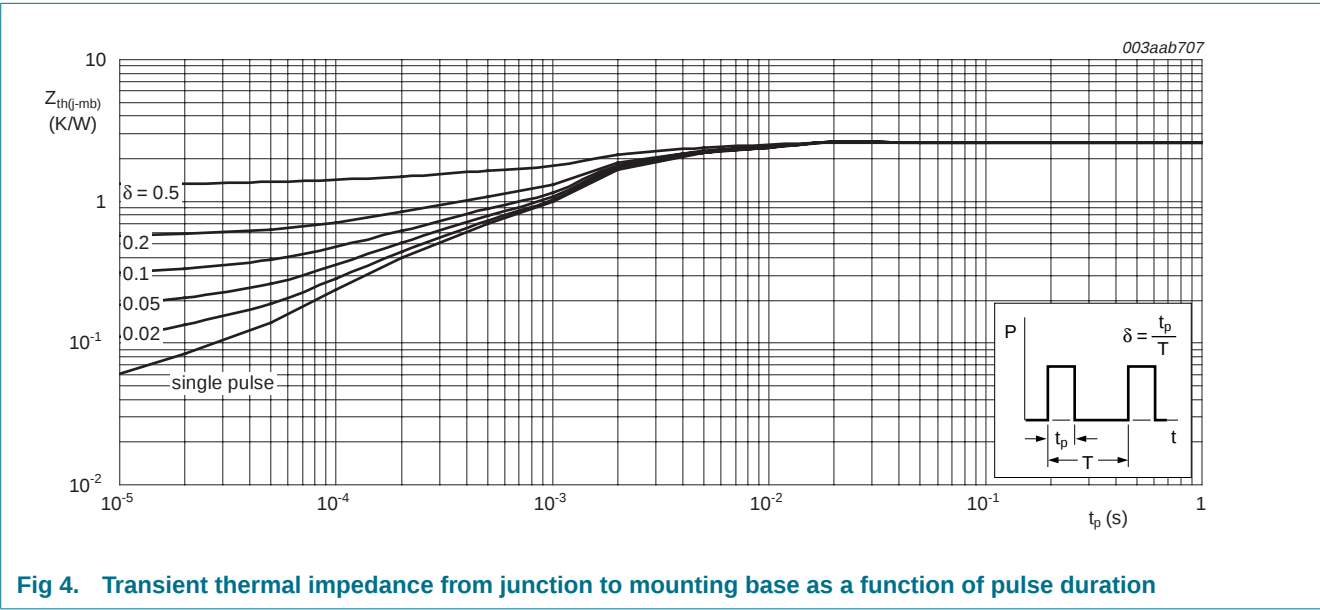
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT428	minimum footprint	-	75	-	K/W
		SOT404 minimum footprint	[1] -	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

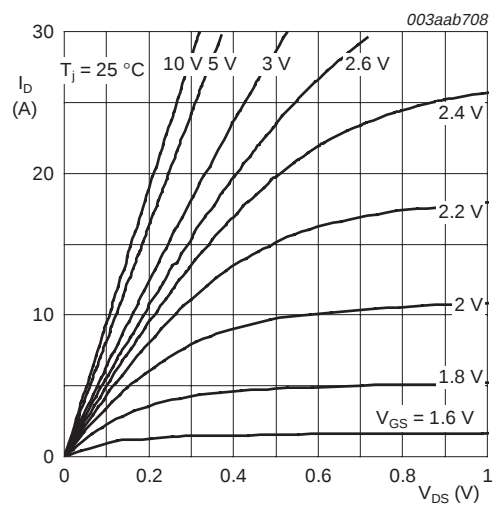


6. Characteristics

Table 5. Characteristics

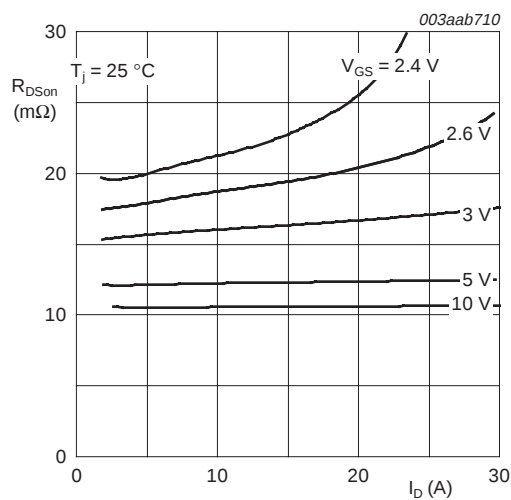
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	20	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	0.5	1.0	1.5	V
		$T_j = 175\text{ }^{\circ}\text{C}$	0.3	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	1.8	V
I_{DSS}	drain leakage current	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	0.05	1.0	μA
		$T_j = 175\text{ }^{\circ}\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 12\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	13.5	16	m Ω
		$T_j = 175\text{ }^{\circ}\text{C}$	-	24.3	28.8	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 10\text{ V}$; $V_{GS} = 5\text{ V}$; see Figure 11 and 12	-	15.1	-	nC
Q_{GS}	gate-source charge		-	4.5	-	nC
Q_{GD}	gate-drain charge		-	4.2	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; see Figure 14	-	800	-	pF
C_{oss}	output capacitance		-	260	-	pF
C_{rss}	reverse transfer capacitance		-	190	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{GS} = 10\text{ V}$; $R_G = 5.6\text{ }\Omega$	-	4	-	ns
t_r	rise time		-	12.5	-	ns
$t_{d(off)}$	turn-off delay time		-	30	-	ns
t_f	fall time		-	23	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 13	-	0.98	1.2	V



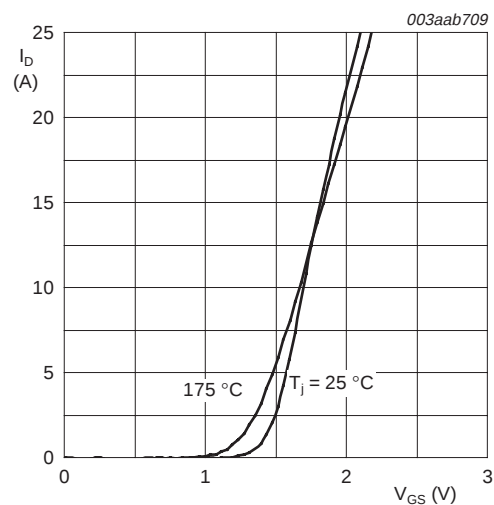
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



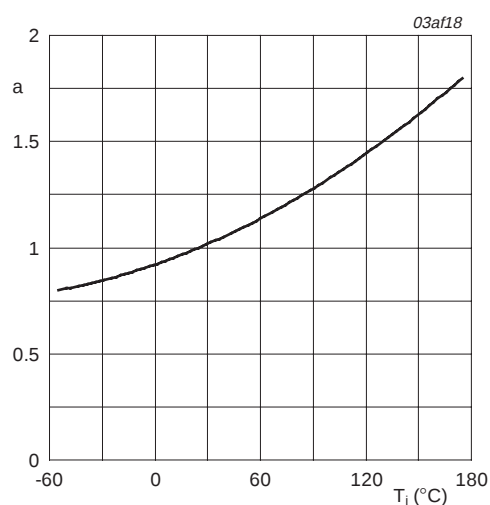
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



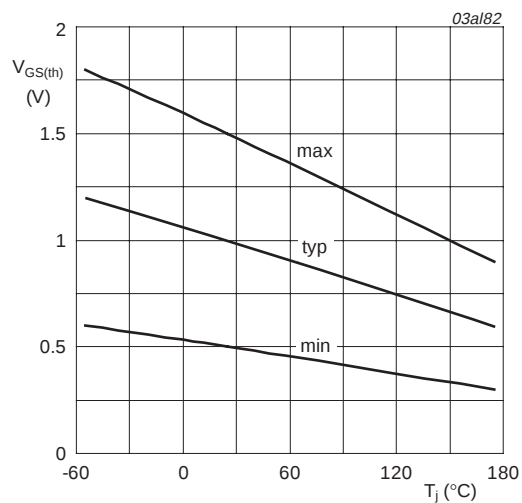
T_j = 25 °C and 175 °C; V_{DS} > I_D × R_{DSon}

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



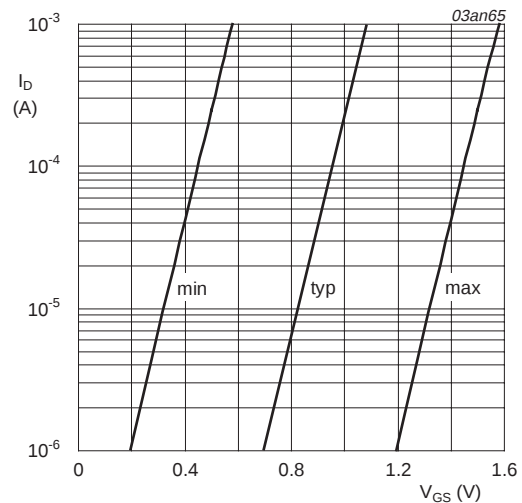
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



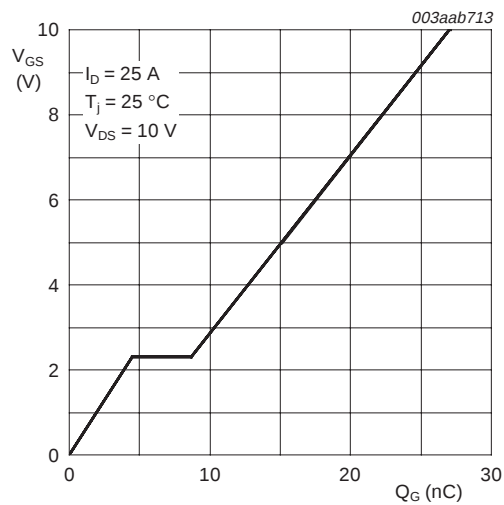
$I_D = 0.25 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}$; $V_{DS} = 10 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

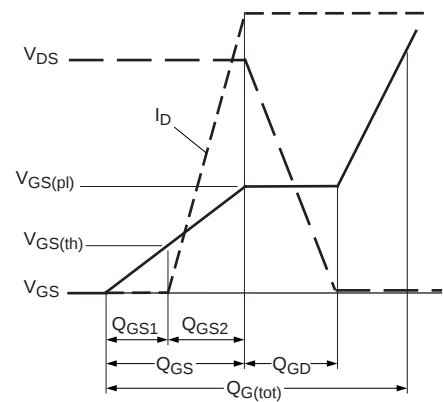
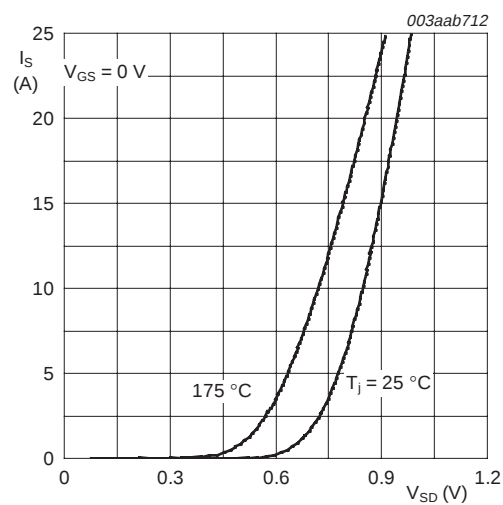
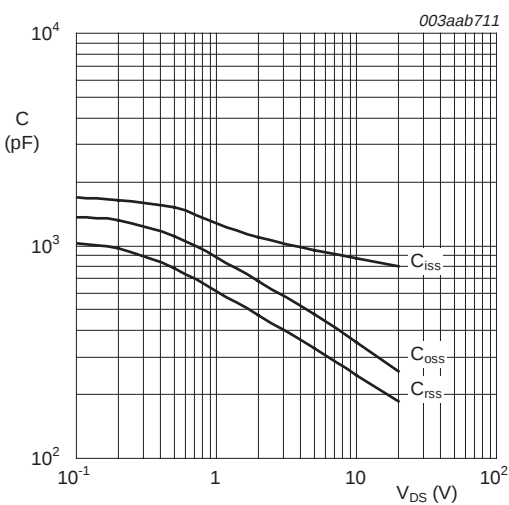


Fig 12. Gate charge waveform definitions



$T_J = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

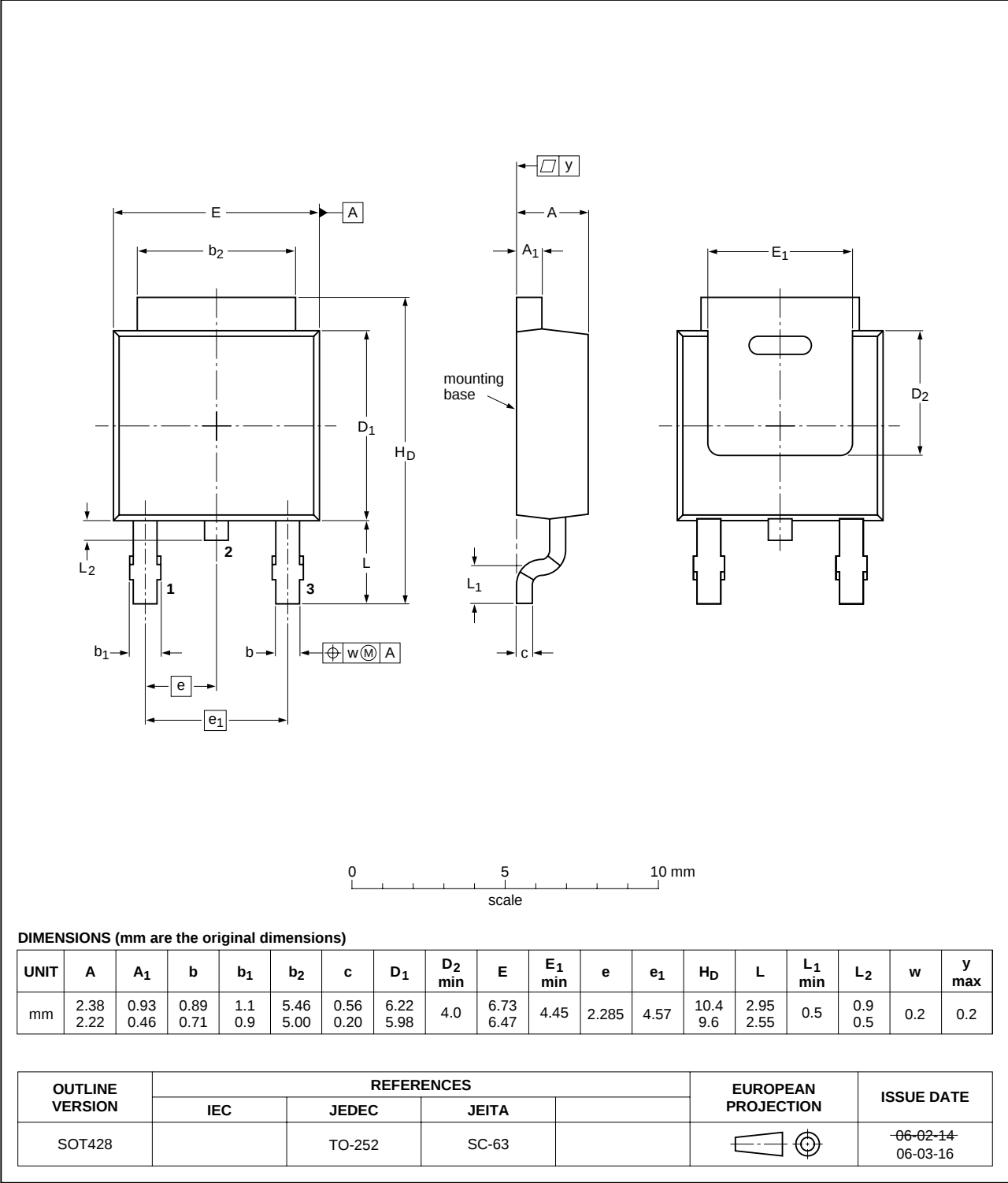


Fig 15. Package outline SOT428 (DPAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD38N02LT_2	20070202	Product data sheet	-	PHB_PHD38N02LT-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • PHB38N02LT has been discontinued.			
PHB_PHD38N02LT-01 (9397 750 11614)	20030630	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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