

MAX 10 FPGA Development Kit

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The Altera® MAX® 10 FPGA Development Kit provides a full featured design platform built around a 50 K logic elements (LEs) MAX 10 FPGA, optimized for system level integration with on-die analog-to-digital converter (ADC), dual-configuration flash, and DDR3 memory interface support. The board features on-board USB-Blaster™ II, high-speed mezzanine card (HSMC) and PMOD expansion, high-definition multimedia interface (HDMI) output, and dual Ethernet for industrial Ethernet applications. The MAX 10 FPGA Development Kit provides the perfect system-level prototyping solution for industrial, automotive, consumer, and many other market applications.

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With this development board, you can:

- Develop designs for the 10M50D, F484 package FPGA
- Measure the performance of the MAX 10 FPGA analog-to-digital block conversion
- Interface MAX 10 FPGAs to DDR3 memory at 300 MHz performance
- Run embedded Linux using the Nios® II processor
- Interface to daughtercards and peripherals using HSMC and PMOD connectors
- Measure FPGA power (V_{CC_CORE} and V_{CC_IO}) using the power monitor graphical user interface (GUI)
- Reuse the kit's PCB board and schematic as a model for your design

Ordering Information

Table 1. MAX 10 FPGA Development Kit Ordering Code and Pricing Information		
Ordering Code	Price	Ordering Information
DK-DEV-10M50-A	Open for pre-orders. Contact your local Altera distributor to place your pre-order.

Development Kit Contents

The MAX 10 FPGA Development Kit includes the following:

- RoHS- and CE-compliant MAX 10 FPGA Development board
 - Featured devices
 - MAX 10 FPGA (10M50D, dual supply, F484 package)
 - [Enpirion® EN2342QI](#) 4 A PowerSoC Voltage-Mode Synchronous Step-Down Converter with Integrated Inductor
 - [Enpirion EN6337QI](#) 3 A High-Efficiency PowerSoC DC-DC Step-Down Converters with Integrated Inductor
 - [Enpirion EP5358xUI](#) 600 mA PowerSoC DC-DC Step-Down Converters with Integrated Inductor
 - MAX II CPLD – EPM1270M256C4N (On-board USB Blaster II)
 - Programming and Configuration
 - Embedded USB-Blaster II (JTAG)
 - Optional JTAG direct via 10-pin header
 - Memory devices
 - 64Mx16 1 Gb DDR3 SDRAM with soft memory controller
 - 128Mx8 1 Gb DDR3 SDRAM with soft memory controller
 - 512Mb QSPI Flash
 - Communication ports
 - Two Gigabit Ethernet (GbE) RJ-45 ports
 - One mini-USB2.0 UART
 - One HDMI video output
 - One universal HSMC connector (see [HSMC expansion cards](#))
 - Two 12-pin PMOD connectors (see [PMOD expansion cards](#))
 - Analog
 - Two MAX 10 FPGA ADC SMA inputs
 - 2x10 ADC header
 - Potentiometer input to ADC
 - One external 16 bit digital-to-analog converter (DAC) device with SMA output
 - Clocking
 - 25 MHz single-ended, external oscillator clock source
 - Silicon labs clock generator with programmable frequency GUI
 - Switches, push buttons, jumpers, and status LEDs
 - Mini-USB cable for on-board USB-Blaster II
 - 2A Power Supply and cord
 - Free [Quartus® II Web Edition design software](#) (download software and license from website)
 - Complete documentation
 - User manual, bill of materials, schematic, and board files

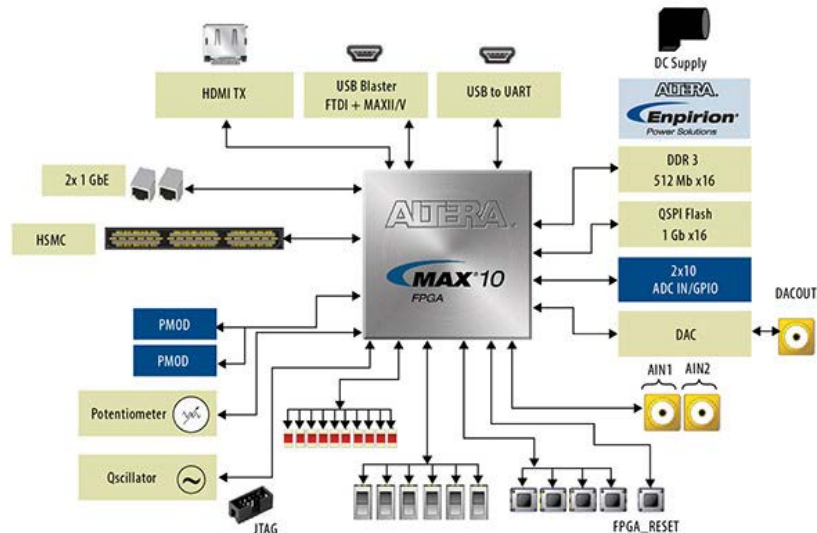
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Figure 1. MAX 10 FPGA Development Board



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Figure 2. MAX 10 FPGA Development Board Block Diagram



Documentation

Table 2. MAX 10 FPGA Development Kit Documents (Available Soon)	
Document	Description
User Guide	Information about the MAX 10 FPGA Development Kit hardware and board setup including how to use included software.
Complete kit document installation (Windows PC only)	Full installation of all files, including the user manual, BOM, layout, PCB, schematics, and other documents or files.

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Related Links

- [MAX 10 FPGA training videos](#)
- [Design Store - MAX 10 FPGA reference designs](#)
- [MAX 10 FPGA documentation](#)
- Online training:
 - [Basics of Programmable Logic](#)
 - [The Quartus II Software Design Series Foundation](#)
 - [The Quartus II Software Interactive Tutorial](#)

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