

ADCV0831

ADCV0831 8 Bit Serial I/O Low Voltage Low Power ADC with Auto Shutdown in a SOT Package



Literature Number: SNAS014

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General Description

The ADCV0831 is a low voltage 8-bit successive approximation A/D converter with serial I/O. The I/O is a 3-wire serial interface compatible with NSC's MICROWIRE™ & Motorola's SPI standards. It easily interfaces with standard shift registers or microprocessors.

Low voltage and auto shutdown features make the ADCV0831 ideal for portable battery operated electronic devices. The main benefits are most apparent in small portable electronic devices. The tiny A/D converter can be placed anywhere on the board.

Applications

- Digitizing automotive sensors
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Test systems
- Embedded diagnostics

Features

- Tiny 6-pin SOT 23 package
- Serial digital data link requires few I/O pins
- Auto Shutdown
- 0V to 3V analog input range with single 3V power supply
- TTL/CMOS input/output compatible

Key Specifications

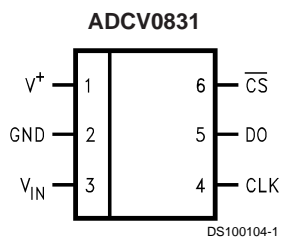
(For 3V supply, typical, unless otherwise noted.)

- Resolution: 8 bits
- Conversion time ($f_C = 700$ kHz): 16 μ s
- Low power dissipation: 720 μ W
- Single supply: 2.7V to 5V_{DC}
- Linearity error: ± 1.5 LSB over temperature
- No missing codes over temperature
- Shutdown supply current 10nA

Ordering Information

| Temperature Range (0°C ≤ T _j ≤ +70°C) | Package | Supplied As |
|-----------------------------------------------------|---------|------------------------|
| ADCV0831M6 | MA06A | 1k Units Tape and Reel |
| ADCV0831M6X | MA06A | 3k Units Tape and Reel |

Connection Diagram



Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | 5.5V |
| Voltage at Inputs and Outputs | -0.3V to $V_{CC} + 0.3V$ |
| Input Current at Any Pin (Note 4) | ± 5 mA |
| Package Input Current (Note 4) | ± 20 mA |
| Power Dissipation at $T_A = 25^\circ\text{C}$ (Note 5) | 470 mW |
| ESD Susceptibility (Note 6) | 2000V |

| | |
|--------------------------------------|-----------------|
| Soldering Temperature (Note 7) | |
| Convection Infrared (15 sec.) | 215°C |
| Wave Soldering (4 sec.) (Note 7) | 260°C |
| Storage Temperature | -65°C to +150°C |
| Thermal Resistance (θ_{JA}) | 265°C/W |

Operating Ratings (Notes 2, 3)

| | |
|-----------------------------|--------------------------------------------------|
| Temperature Range | $0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$ |
| Supply Voltage (V_{CC}) | 2.7V _{DC} to 5V |

Electrical Characteristics

The following specifications apply for $V_{CC} = 3V_{DC}$, and $f_{CLK} = 500$ kHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 8) | Limits (Note 9) | Units |
|--------------|----------------------------|-------------------------------|------------------|-------------------------------------------------------------------|---------------------|
| | Integral Linearity Error | | ± 0.6 | ± 1.5 | LSB (max) |
| | Offset Error | | ± 0.1 | ± 1.5 | LSB (max) |
| | Full Scale Error | | ± 0.3 | ± 1.5 | LSB (max) |
| | Resolution | | | 8 | Bits (min) |
| V_{IN} | Analog Input Voltage | | | ($V_{CC} + 0.05$) ($GND - 0.05$) | V (max) V (min) |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 3V$ | | 2.0 | V (min) |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 3V$ | | 0.8 | V (max) |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{IN} = 3V$ | 0.01 | 1 | μA (max) |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{IN} = 0V$ | 0.01 | -1 | μA (max) |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $I_{out} = -360\mu\text{A}$ | 2.8 | 2.4 | V (min) |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $I_{out} = 1.6$ mA | 0.24 | 0.4 | V (max) |
| I_{OUT} | TRI-STATE® Output Current | $V_{OUT} = 0V$ | 0.01 | 3.0 | μA (max) |
| I_{SOURCE} | Output Source Current | $V_{OUT} = 0V$ | 2.6 | 1.0 | mA (min) |
| I_{SINK} | Output Sink Current | $V_{OUT} = 3V$ | 7.4 | 3.0 | mA (min) |
| I_{CC} | Supply Current | $\overline{CS} = \text{HIGH}$ | 0.01 | 30 | μA (max) |
| | | $\overline{CS} = \text{LOW}$ | 200 | 400 | μA (max) |

AC Electrical Characteristics

The following specifications apply for $V_{CC} = +3 V_{DC}$, and $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 8) | Limits (Note 9) | Units | |
|------------------|-------------------------------------------------------------------------------------------|---------------------------------------|------------------|------------------------|------------------------|----------|
| f_{CLK} | Clock Frequency | | 10 | 700 | kHz (max) kHz (min) | |
| t_{SET-UP} | \overline{CS} falling edge to CLK rising edge | | 25 | | ns | |
| | Clock Duty Cycle | | | 40 60 | % (min) % (max) | |
| T_C | Conversion Time | | | 11 | Clock Periods | |
| t_{pd} | CLK Falling Edge to Data Valid | Low to High | $C_L = 100$ pF | 142 | 250 | ns (max) |
| | | High to Low | | 70 | | |
| t_{1H}, t_{OH} | \overline{CS} Rising Edge to Data Output TRI-STATE (see TRI-STATE Test Circuits) | $C_L = 100$ pF, $R_L = 2$ k Ω | 75 | 250 | ns (max) | |
| | | $C_L = 100$ pF, $R_L = 10$ k Ω | 50 | | | |

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = +3 V_{DC}$, and $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | Typical (Note 8) | Limits (Note 9) | Units |
|-----------|------------------------------|------------|------------------|-----------------|-------|
| C_{IN} | Capacitance of Logic Inputs | | 5 | | pF |
| C_{OUT} | Capacitance of Logic Outputs | | 5 | | pF |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND = 0 V_{DC} , unless otherwise specified.

Note 4: When the input voltage V_{IN} at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 k Ω resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or Linear Data Book section "Surface Mount" for other methods of soldering surface mount devices.

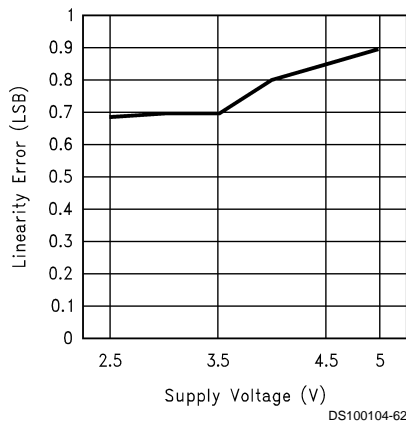
Note 8: Typicals are at $T_J = 25^\circ C$ and represent the most likely parametric norm.

Note 9: Guaranteed to National's AOQL (Average Outgoing Quality Level).

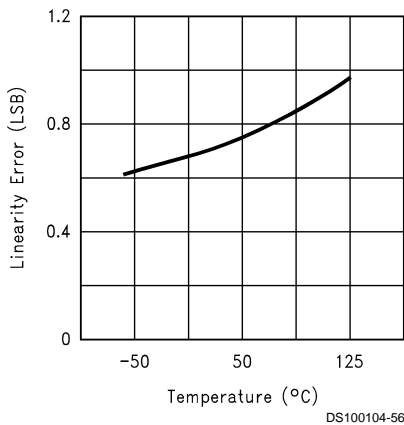
Typical Performance Characteristics

The following specifications apply for $V_{CC} = 3V$, unless otherwise specified

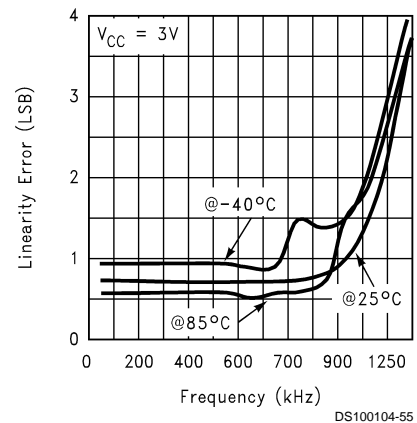
Integral Linearity Error vs Supply Voltage



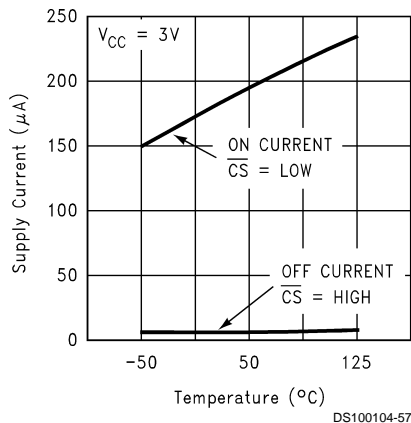
Linearity Error vs Temperature



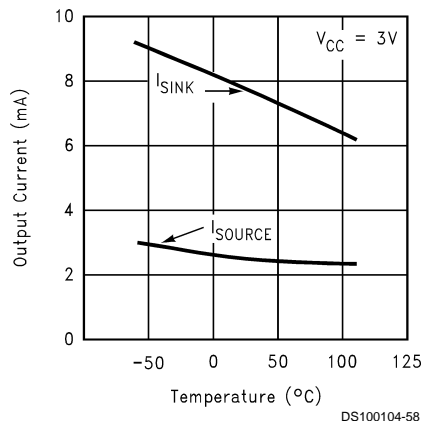
Linearity Error vs Clock Frequency



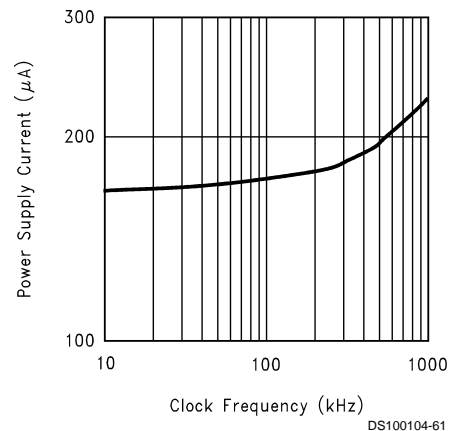
Power Supply Current vs Temperature



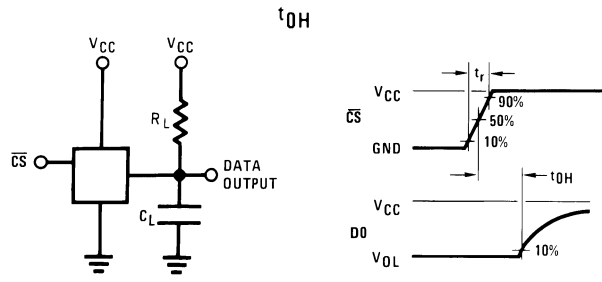
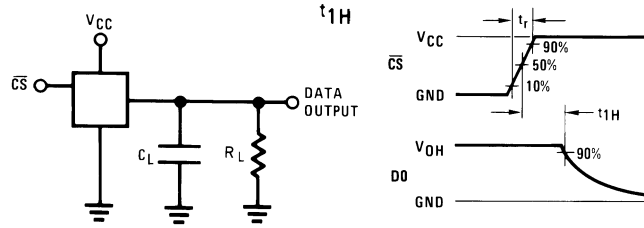
Output Current vs Temperature



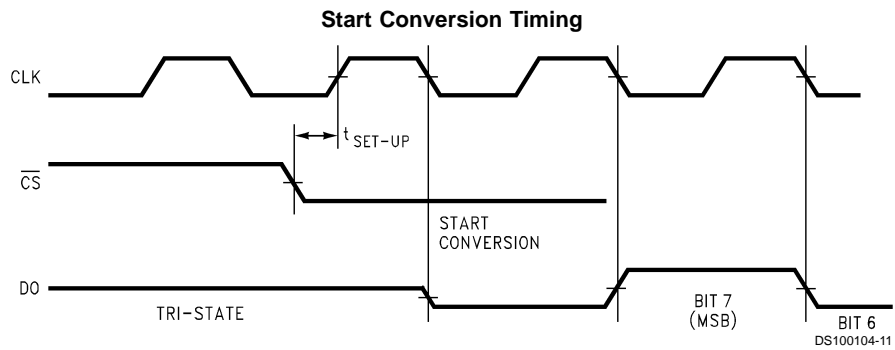
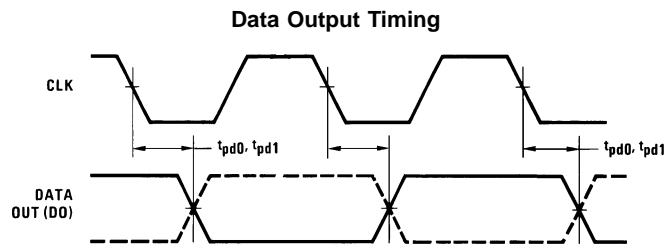
Power Supply Current vs Clock Frequency



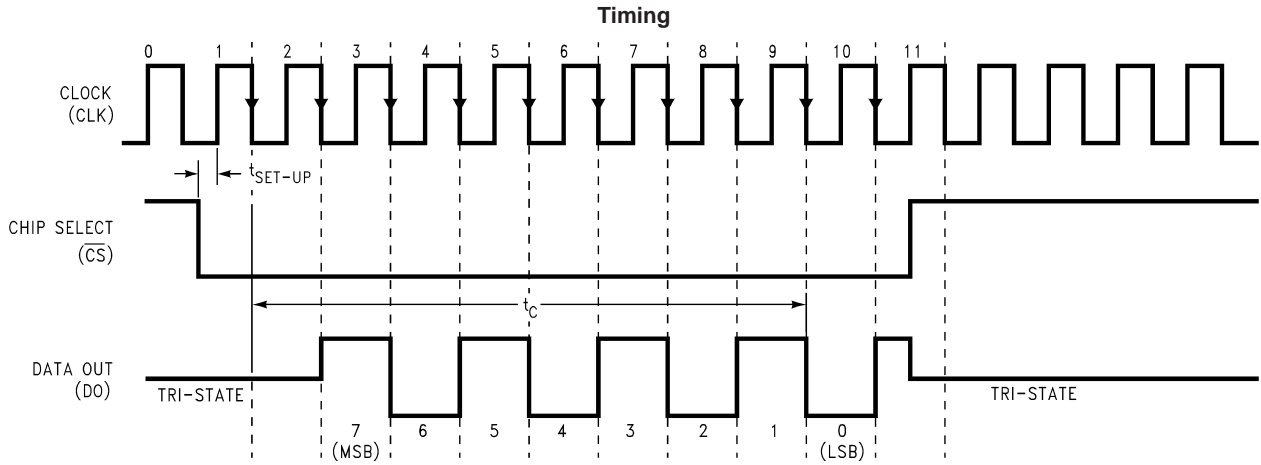
TRI-STATE Test Circuits and Waveforms



Timing Diagrams



Timing Diagrams (Continued)



DS100104-12

Functional Description

The design of this converter utilizes a comparator structure with built-in sample-and-hold which provides for V_{IN} to be converted by a successive approximation routine.

The analog input voltage can range from 50mV below ground to 50mV above V_{CC} without degrading conversion accuracy.

The ADC0831 is intended to work with a CPU which strobes data on the clock's rising edge. The ADC0831 strobes data on the clock's falling edge so that the data output is stable when the CPU reads it in.

When the Chip Select pin is high, the output is TRI-STATE and the ADC0831 is in shutdown mode and draws less than 30 μ A of current. During shutdown the digital logic draws no current at CMOS logic levels, and the analog circuitry is turned off. When the Chip Select pin goes low, all the analog circuitry turns on, and the conversion process begins.

1.0 THE DIGITAL INTERFACE

The most important characteristic of this converter is the serial data link with the controlling processor. Using a serial communication format offers three very significant system improvements. It allows many functions to be included in a small package, it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor, and can transmit highly noise immune digital data back to the host processor.

To understand the operation of this converter it is best to refer to the Timing Diagrams and to follow a complete conversion sequence.

1. A conversion is initiated by pulling the \overline{CS} (chip select) line low. This line must be held low for the entire conversion.
2. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages in a resistor ladder (last 8 bits). After each comparison the comparator's output is shifted to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
3. After 11 clock periods the conversion is completed.
4. All internal registers are cleared when the \overline{CS} line is high. See Data Input Timing under Timing Diagrams. If another conversion is desired \overline{CS} must make a high to low transition.

2.0 REFERENCE CONSIDERATIONS

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is the system power supply. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

Since there is no separate reference and analog supply pins, the analog side is very sensitive. The PC layout of the ADC0831 is very critical. The ADC0831 should be used with an analog ground plane and single-point grounding techniques. The Gnd pin should be tied directly to the ground plane. One supply bypass capacitor (0.1 μ F) is recommended to decouple all the digital signals on the supplies. The lead length of the capacitor should be as short as possible.

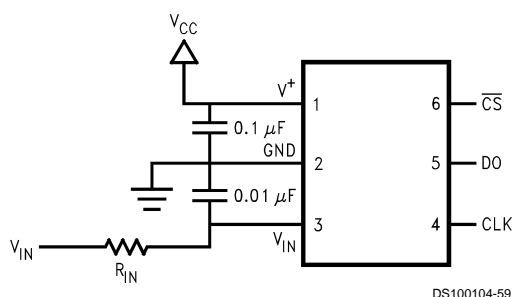
3.0 THE ANALOG INPUT

The most important feature of this converter is that it can be located right at the analog signal source through just a few wires. It can communicate with a processor with a highly noise immune serial bit stream. This greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The input has a sample and hold, therefore a capacitor (0.01 μ F) is needed at the input pin in order to swamp out any feedthrough signal coming from the sample and hold circuitry.

The input capacitor lead length is not as critical as the supply decoupling capacitor, as long as the capacitor is large enough to swamp out any sample and hold feedthrough.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. Bypass capacitors should not be used if the source resistance is greater than 1k Ω . The worst-case leakage current of $\pm 1\mu$ A over temperature will create a 1mV input error with a 1k Ω source resistance. An op-amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

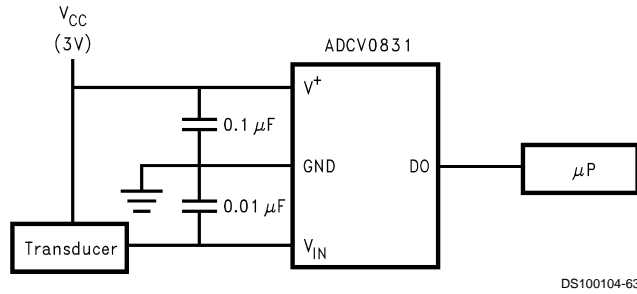


Recommended Power Supply Bypassing

Applications

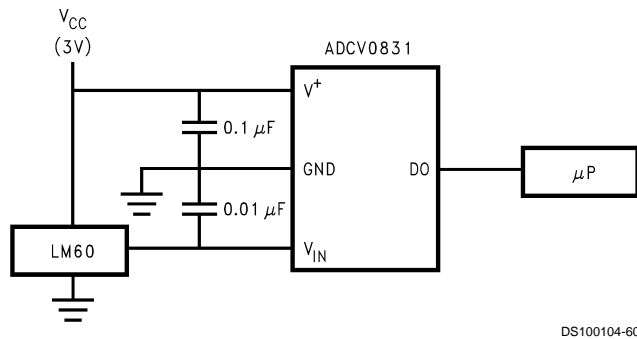
The ADCV0831 is ideal for applications operating with ratiometric transducers. The ADCV0831 can measure the signal produced by the transducer and produce a corresponding code to the microprocessor. The microprocessor can then control the system producing the signal.

Operating with Ratiometric Transducers



The ADCV0831 can be used in low-cost remote temperature sensor system. For a temperature sensor, the LM60 is an excellent companion to the ADCV0831, since it can operate off 3V supply. The LM60 linear scale factor is 6.25mV/°C. Therefore, the ADCV0831 can digitize a couple of degrees change in temperature and provide the output to the microprocessor, which in turn can adjust the system environment. For higher accuracy, a low-offset op-amp can be used to gain up the LM60 output.

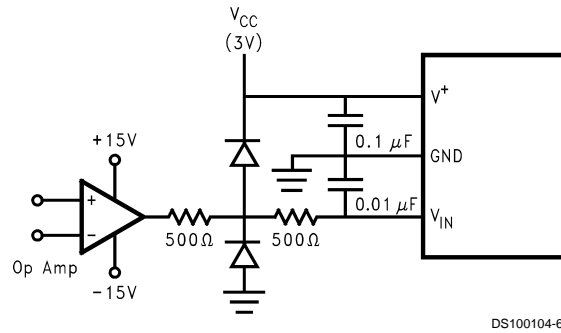
Low-Cost Remote Temperature Sensor



Applications (Continued)

When the input of the ADCV0831 is driven by an op-amp operating at a supply voltage greater than 5V, it is a good idea to protect the input of the ADCV0831 from exceeding the supply voltage. Two diodes can be added to the input one to supply and one to the ground pin.

Protecting the input

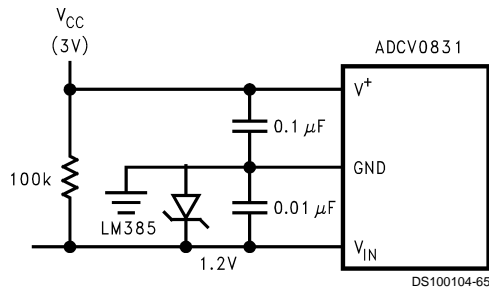


DS100104-64

Note: Diodes are IN914

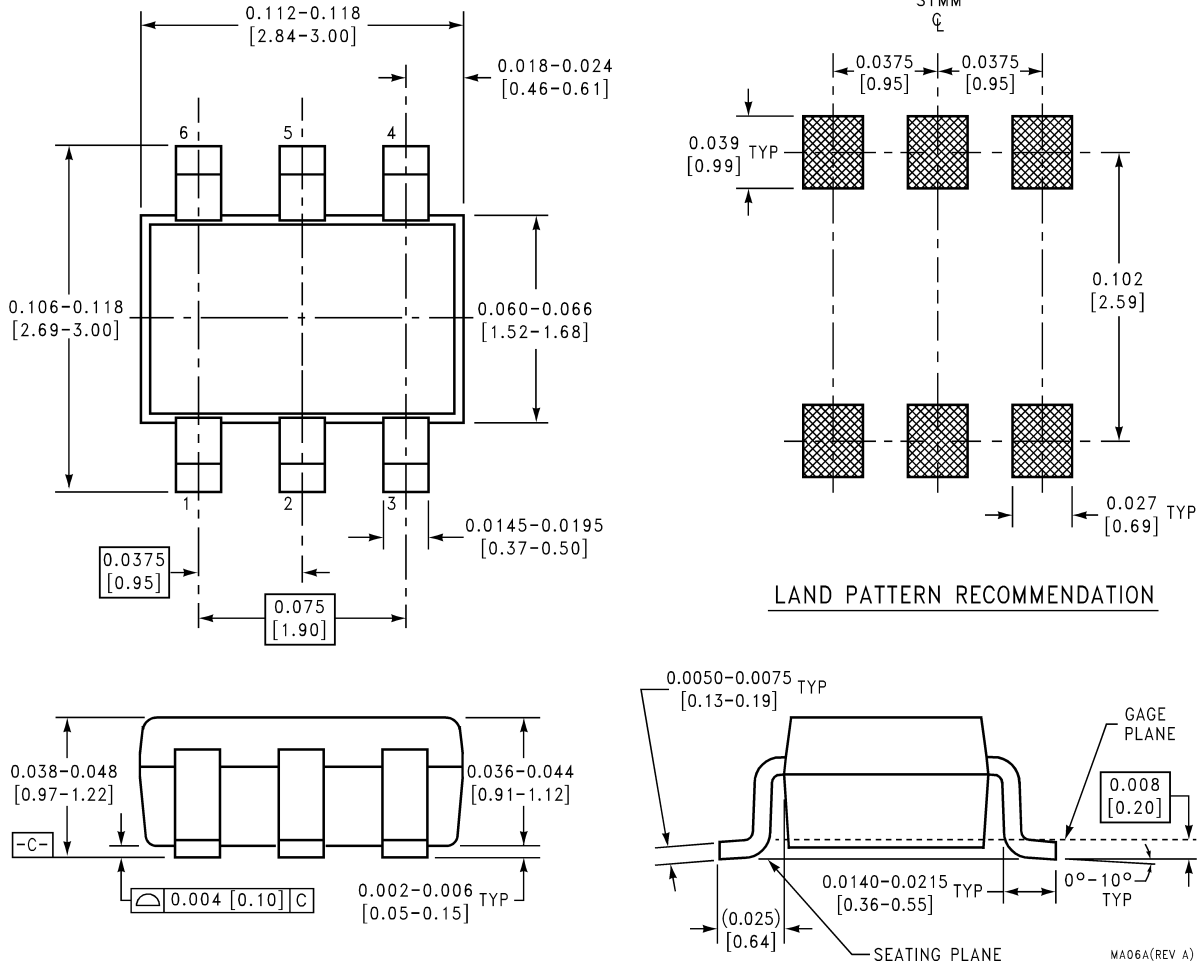
This circuit utilizes the LM385 reference to detect the power supply voltage level. When the supply voltage is 3V, the LSB = $3/256 = 11.7\text{mV}$. Since the LM385 reference sets the input to 1.2V. The output code is 102. As the supply voltage decreases, the LSB decreases and the output code increases. When the supply voltage reaches 2.7V, the LSB = 10.5 mV. The input voltage is still at 1.2V, and the output code is 114. If the supply voltage increases, the LSB increases and the output code decreases. When the supply voltage reaches 3.3V, the LSB = 12.9mV and the output code is 93.

Power Supply Level Detection



DS100104-65

Physical Dimensions inches (millimeters) unless otherwise noted



**Order Number ADCV0831M6X, ADCV0831M6
NS Package Number MA06A**

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Applications

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