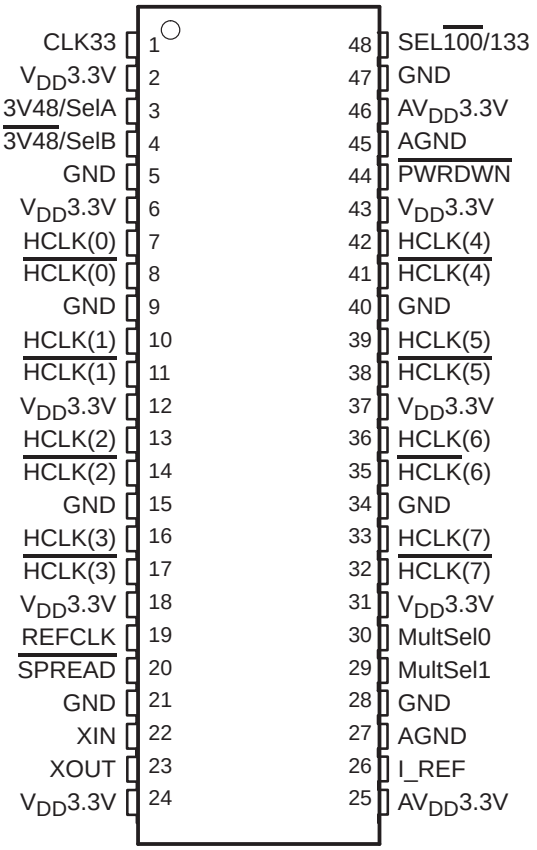
- **Generates Clocks for Next Generation Microprocessors**
- **Uses a 14.318-MHz Crystal Input to Generate Multiple Output Frequencies**
- **Includes Spread Spectrum Clocking (SSC), 0.6% Downspread for Reduced EMI With Theoretical EMI of 7 dB**
- **Power Management Control Terminals**
- **Low Output Skew and Jitter for Clock Distribution**
- **Operates From a Single 3.3-V Supply**
- **Generates the Following Clocks:**
  - **8 Host (Diff Pairs, 100/133 MHz)**
  - **1 CLK33 (3.3 V, 33.3 MHz)**
  - **1 REFCLK (3.3 V, 14.318 MHz)**
  - **2 3V48 (3.3 V, 180° Shifted Pairs, 48 MHz)**
- **Packaged in a 48-Pin TSSOP Package**

DGG PACKAGE
(TOP VIEW)



description

The CDC950 is a differential clock synthesizer/driver that generates HCLK/HCLK, CLK33, 3V48, and REFCLK system clock signals to support a computer system with next generation processors and double data rate (DDR) memory subsystems.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input can be provided at the XIN input instead of a crystal. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components.

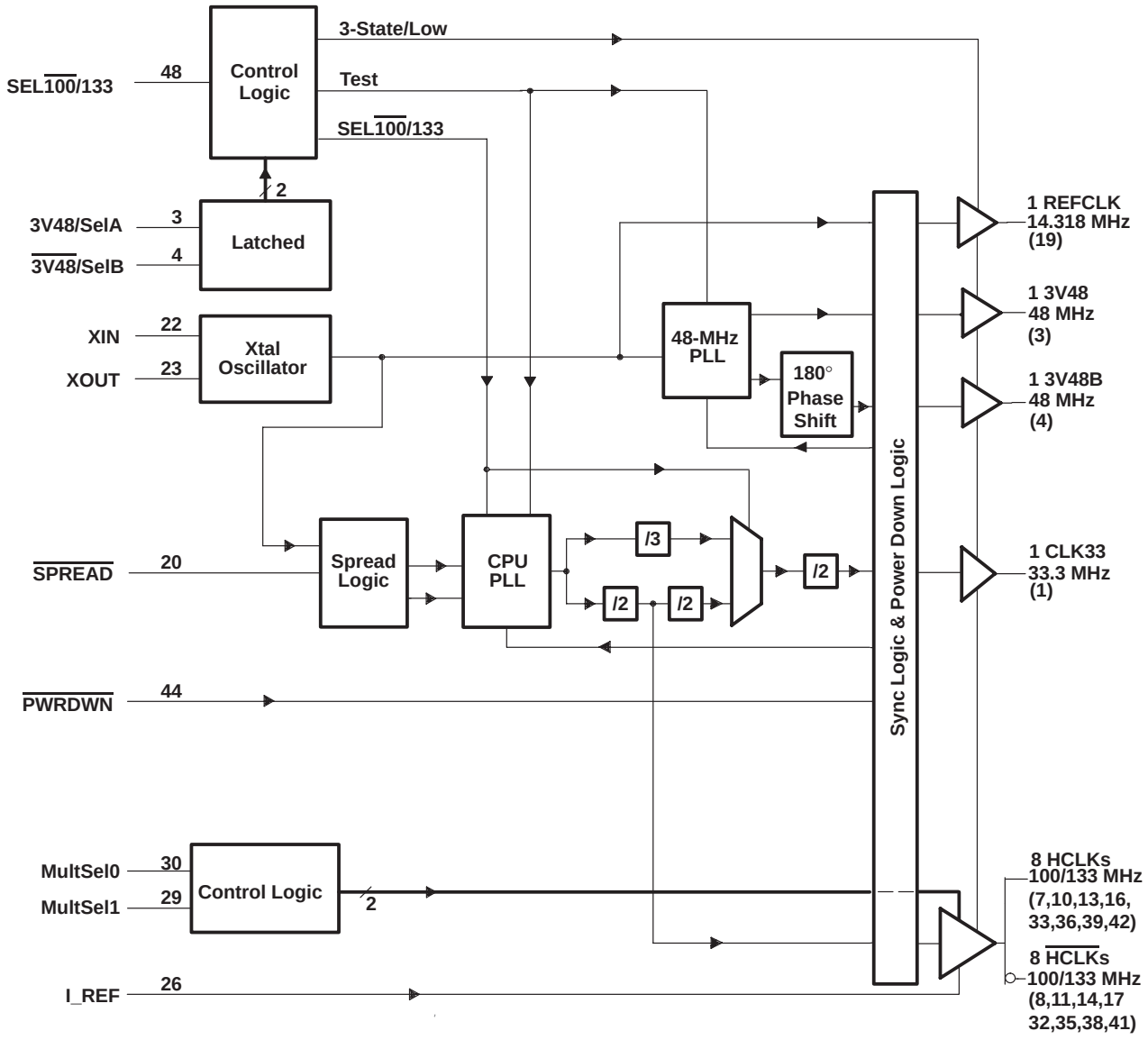
The HCLK, CLK33 clock, and 48-MHz clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected through control inputs SEL100/133, 3V48/SelA, and 3V48/SelB.

The outputs are either differential host clock or 3.3-V single-ended CMOS buffers. With a logic high-level on the PWRDWN terminal, the device operates normally. When a logical low-level input is applied, the device powers down completely with the HOST clock at $2 \times I_{REF}$, HOSTB is undriven, CLK33, 3V48, and REFCLK outputs are in a low-level output state and 3V48B is in a high-level output state.

The host bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with the corresponding setting for SEL100/133 control input. The CLK33 (PCI) frequency is fixed to 33 MHz.

Since the CDC950 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up, as well as following changes to the SEL inputs. With the use of an external reference clock, this signal must be fixed-frequency and fixed-phase prior to stabilization time starts. The CDC950 is characterized for operation from 0°C to 85°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V48/SelA, 3V48/SelB	3, 4	I/O	48-MHz 180° shifted pair clocks for USB use Logic select pins. Selects the mode of operation, see Table 1 for details.
AGND	27, 45	P	Analog ground
AV_{DD}3.3V	25, 46	P	Power. Analog power supply
CLK33	1	O	33-MHz reference clock for PCI use, host clock divided by 3 or by 4
GND	5, 9, 15, 21, 28, 34, 40, 47	P	Ground
HCLK	7, 10, 13, 16, 33, 36, 39, 42	O	CPU and host clock outputs [7:0]. These eight differential CPU clock pairs run at 100/133 MHz. The V_{OH} swing amplitude is configured by MultSel0, MultSel1 pins. See Table 5 and Intel's CK00 document for details.
$\overline{\text{HCLK}}$	8, 11, 14, 17, 32, 35, 38, 41	O	CPU and host clock outputs [7:0]. These eight differential CPU clock pairs run at 100/133 MHz. The V_{OH} swing amplitude is configured by MultSel0, MultSel1 pins. See Table 5 and Intel's CK00 document for details.
I_REF	26	I	Current reference. This pin establishes the reference current for host clock parts. See Table 5 and Intel's CK00 document for details.
MultSel0	30	I	See Table 5 and Intel's CK00 document for details.
MultSel1	29	I	See Table 5 and Intel's CK00 document for details.
$\overline{\text{PWRDWN}}$	44	I	Power-down input. 3.3-V LVTTL compatible, asynchronous input that requests the device to enter the power-down mode. See Table 2 for details.
REFCLK	19	O	14.138-MHz reference clock output: 3.3 V copy of the 14.318-MHz reference clock.
SEL$\overline{100}$/133	48	I	Active low LVTTL level logic select. SEL100/133 is used for enabling 100/133 MHz. Low = 100 MHz, high = 133 MHz
$\overline{\text{SPREAD}}$	20	U	Spread spectrum enable. 3.3-V LVTTL compatible, input that enables the spread spectrum mode when held low. See Table 4 for details.
V_{DD}3.3V	2, 6, 12, 18, 24, 31, 37, 43	P	Power. Power supply
XIN	22	I	Crystal connection or an external reference frequency input. Connect to either a 14.138-MHz crystal or an external reference signal.
XOUT	23	O	Crystal connection. An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.

Function Tables

Table 1. Select Functions

INPUTS			OUTPUTS				FUNCTION
SEL$\overline{100}$/133	SelA	SelB	HCLK, $\overline{\text{HCLK}}$	CLK33	3V48, $\overline{\text{3V48}}$	REFCLK	
0	0	0	100 MHz	33 MHz	48 MHz	14.318 MHz	Active 100 MHz
0	0	1	100 MHz	33 MHz	L, H	14.318 MHz	100 MHz mode; PLL48 powerdown
0	1	0	105 MHz	35 MHz	48 MHz	14.318 MHz	100 MHz mode 5% overclocking
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	All 3-state outputs
1	0	0	133 MHz	33 MHz	48 MHz	14.318 MHz	Active 133 MHz
1	0	1	127 MHz	31.7 MHz	48 MHz	14.318 MHz	133 MHz mode −5% underclocking
1	1	0	133 MHz	33 MHz	48 MHz	14.318 MHz	Test mode
1	1	1	TCLK/2	TCLK/8	TCLK/2	TCLK	Test mode (PLL bypass)

Table 2. Enable Functions

INPUT	OUTPUTS					
$\overline{\text{PWRDWN}}$	HCLK	$\overline{\text{HCLK}}$	CLK33	3V48	$\overline{\text{3V48}}$	REFCLK
0	$2 \times I_{REF}$	Hi-Z	L	L	H	L
1	On	On	On	On	On	On

Table 3. Output Buffer Specifications

BUFFER NAME	V_{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
3V48, REFCLK	3.135 − 3.465	20−60	TYPE 3
CLK33	3.135 − 3.465	12−55	TYPE 5
HCLK/$\overline{\text{HCLK}}$	3.135 − 3.465		TYPE X1

Table 4. Spread Spectrum Functions

INPUT	OUTPUTS
$\overline{\text{SPREAD}}$	
0	Spread spectrum clocking active, −0.6% at HCLK/$\overline{\text{HCLK}}$, CLK33
1	Spread spectrum clocking inactive

Function Tables (Continued)

Table 5. Host/$\overline{\text{HOST}}$ Output Buffer Specifications

INPUT		BOARD TARGET TRACE/TERM Z	REFERENCE R, I_{REF} = VDD/(3 Rr)		OUTPUT CURRENT I_{OH}	V_{OH} at Z
MultSel0	MultSel1					
0	**0**	**60 Ω**	**Rr = 475 1%,**	**I_REF = 2.32 mA**	**5 × I_{REF}**	**0.71 V at 60 Ω**
0	0	50 Ω	Rr = 475 1%,	I_REF = 2.32 mA	5 × I_{REF}	0.59 V at 50 Ω
0	1	60 Ω	Rr = 475 1%,	I_REF = 2.32 mA	6 × I_{REF}	0.85 V at 60 Ω
0	**1**	**50 Ω**	**Rr = 475 1%,**	**I_REF = 2.32 mA**	**6 × I_{REF}**	**0.71 V at 50 Ω**
1	0	60 Ω	Rr = 475 1%,	I_REF = 2.32 mA	4 × I_{REF}	0.56 V at 60 Ω
1	0	50 Ω	Rr = 475 1%,	I_REF = 2.32 mA	4 × I_{REF}	0.47 V at 50 Ω
1	1	60 Ω	Rr = 475 1%,	I_REF = 2.32 mA	7 × I_{REF}	0.99 V at 60 Ω
1	1	50 Ω	Rr = 475 1%,	I_REF = 2.32 mA	7 × I_{REF}	0.82 V at 50 Ω
0	0	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	5 × I_{REF}	0.75 V at 30 Ω
0	0	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	5 × I_{REF}	0.62 V at 25 Ω
0	1	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	6 × I_{REF}	0.90 V at 30 Ω
0	1	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	6 × I_{REF}	0.75 V at 25 Ω
1	0	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	4 × I_{REF}	0.60 V at 30 Ω
1	0	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	4 × I_{REF}	0.5 V at 25 Ω
1	1	30 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	7 × I_{REF}	1.05 V at 30 Ω
1	1	25 (dc equivalent)	Rr = 221 1%,	I_REF = 5 mA	7 × I_{REF}	0.84 V at 25 Ω

NOTE: The entries in **boldface** are the primary system configurations of interest. The outputs should be optimized for these configurations.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.3 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{DD} + 0.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . –0.5 V to V_{DD} + 0.5 V
Current into any output in the low state, I_O . . . . . 2 × rated I_{OL}
Input clamp current, I_{IK}: (V_I < 0) . . . . . –50 mA
(V_I > V_{DD}) . . . . . 50 mA
Output clamp current, I_{OK}: (V_O < 0) . . . . . –50 mA
V_O > V_{DD}) . . . . . 50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 89°C/W
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) . . . . . 1070 mW
Operating free-air temperature range, T_A . . . . . –0°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for the through-hole packages, which use a trace length of zero.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGG	1400 mW	11.2 mW/°C	900 mW	730 mW

† This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted device at 89°C/W

recommended operating conditions (see Note 4)

		MIN	NOM‡	MAX	UNIT
Supply voltages, V_{DD}, AV_{DD}		3.135	3.3	3.465	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Input voltage, V_I		−0.3		V_{DD} + 0.3	V
High-level output current, I_{OH}	HCLK/$\overline{\text{HCLK}}$			−40	mA
	CLK33			−18	mA
	3V48/SelA and $\overline{\text{3V48}}$/SelB			−14	mA
	REFCLK			−14	mA
Low-level output current, I_{OL}	HCLK/$\overline{\text{HCLK}}$			0	mA
	CLK33			12	mA
	3V48/SelA and $\overline{\text{3V48}}$/SelB			9	mA
	REFCLK			9	mA
Reference frequency, $f_{(XIN)}$§	Test mode		14		MHz
Crystal, $f_{(XTAL)}$¶	Normal mode	13.8	14.318	14.8	MHz
Operating free-air temperature, T_A		0		85	°C

‡ All nominal values are measured at their respective nominal V_{DD} values.
§ Reference frequency is a test clock driven on the XIN input during the device test mode or normal mode. In test mode, XIN can be driven externally up to $f_{(XIN)}$ = 16 MHz. If XIN is driven externally, XOUT is floating.
¶ This is a series fundamental crystal with fo = 14.31818 MHz
NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{DD} = 3.135 V,	I_I = –18 mA				–1.2	V
I_{IH}	High-level input current	All inputs except SelA, SelB	V_{DD} = 3.465 V,	$V_I = V_{DD}$				5	µA
I_{IL}	Low-level input current	All inputs except SelA, SelB	V_{DD} = 3.465 V,	V_I = GND				−5	µA
I_{OZ}	High-impedance -state output current	All outputs including SelA, SelB	V_{DD} = 3.465 V	3V48/SelA, $\overline{3V48}$/SelB = H, SEL100/133 = L, $V_O = V_{DD}$ or GND, $\overline{PWRDWN}$ = H				±10	µA
$I_{DD(Z)}$	High-impedance-state supply current‡		V_{DD} = 3.465 V	3V48/SelA, $\overline{3V48}$/SelB = H, SEL100/133 = L, $\overline{PWRDWN}$ = H			19	25	mA
$I_{DD(PD)}$			SelA, SelB = L $R_{(ref)}$ = 475 Ω $\overline{PWRDWN}$ = L	VDD Supply			43	47	mA
$AI_{DD(PD)}$	$\overline{PWRDWN}$ state supply current‡			AVDD Supply			3.4	4.2	mA
$I_{DD(D)}$	Dynamic supply current‡		V_{DD} = 3.465 V, R_{ref} = 475 Ω, $I_O = 6 \times I_{ref}$	$\overline{PWRDWN}$ = H SSC = ON/OFF C_L = MAX	100 MHz		173	190	mA
					133 MHz		183	200	
AI_{DD}	Analog power supply current		V_{DD} = 3.465 V	100 MHz and SSC off		19		24	mA
				133 MHz and SSC off		26		33	
				100 MHz and SSC on		26		33	
				133 MHz and SSC on		35		45	
C_I	Input capacitance§		V_{DD} = 3.3 V,	$V_I = V_{DD}$ or GND		2		5	pF
$C_{(XTAL)}$	Crystal load capacitance¶		Effective capacity between C_{IN} and C_{OUT}			13.5		22.5	

† All typical values are measured at their respective nominal V_{DD} values.
‡ C_L = MAX = 5 pF, RS = 33.2 Ω, Rp = 49.9 Ω at HCLK/$\overline{HCLK}$ (Type X1)
C_L = MAX = 20 pF, R_L = 500 Ω at 48 MHz, REF (Type 3)
C_L = MAX = 30 pF, R_L = 500 Ω at CLK33 (Type 5)
§ These parameters are assured by design and lab characterization, not 100% production tested.
¶ This is the corresponding capacitive load for the XTAL in this oscillator application (Pierce oscillator)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

HCLK/$\overline{\text{HCLK}}$ (Type X1)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
r_o	Output resistance			3000			Ω
V_O	Output voltage					1.2	V
I_O	Output current	V_{DD} = 3.30 V nom	All combinations of Table 5, See Note 5	−7% $I_{(NOM)}$		7% $I_{(NOM)}$	mA
		V_{DD} = 3.30 V, ±5%		−12% $I_{(NOM)}$		12% $I_{(NOM)}$	
C_O	Output capacitance	V_{DD} = 3.30 V nom	V_O = V_{DD} GND		3.5		pF

NOTE 5: $I_{(NOM)}$ is output current (I_{OH}) of table 5.

3V48, $\overline{\text{3V48}}$REFCLK (Type 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = min to max,	I_{OH} = –1 mA	V_{DD} – 0.1			V
			V_{DD} = 3.135 V,	I_{OH} = −14 mA	2.4			
V_{OL}	Low-level output voltage		V_{DD} = min to max,	I_{OL} = 1 mA			0.1	
			V_{DD} = 3.135 V,	I_{OL} = 9 mA		0.18	0.4	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	−29			mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		−37		
			V_{DD} = 3.465 V,	V_O = 3.135 V		−11	−23	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	29			
			V_{DD} = 3.3 V,	V_O = 1.65 V		39		
			V_{DD} = 3.465 V,	V_O = 0.4 V		16	27	
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND	4.5		7	pF
Z_o	Output impedance	High state	V_O = 0.5 V_{DD},	V_O/I_{OH}	20	40	60	Ω
		Low state	V_O = 0.5 V_{DD},	V_O/I_{OL}	20	40	60	

† All typical values are measured at their respective nominal V_{DD} values.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

CLK33 (Type 5)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = min to max,	I_{OH} = –1 mA	V_{DD} – 0.1			V
			V_{DD} = 3.135 V,	I_{OH} = −18 mA	2.4			
V_{OL}	Low-level output voltage		V_{DD} = min to max,	I_{OL} = 1 mA			0.1	
			V_{DD} = 3.135 V,	I_{OL} = 12 mA		0.15	0.4	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	−33			mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		−53		
			V_{DD} = 3.465 V,	V_O = 3.135 V		−16	−33	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	30			
			V_{DD} = 3.3 V,	V_O = 1.65 V		51		
			V_{DD} = 3.465 V,	V_O = 0.4 V		21	38	
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND	4.5		7.5	pF
Z_o	Output impedance	High state	V_O = 0.5 V_{DD},	V_O/I_{OH}	12	35	55	Ω
		Low state	V_O = 0.5 V_{DD},	V_O/I_{OL}	12	35	55	

† All typical values are measured at their respective nominal V_{DD} values.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(over)}$	Overshoot†			HCLK/$\overline{\text{HCLK}}$ 0.7-V amplitude			V_{OH} + 200	mV
$V_{(under)}$	Undershoot†						V_{OL} − 200	
$V_{(over)}$	Overshoot†			Other clocks, C_L = worst case	GND − 0.7			V
$V_{(under)}$	Undershoot†						V_{DD} + 0.7	
t_{PZL}	Output enable time from low level	SEL$\overline{100}$/133	All outputs	SEL$\overline{100}$/133 ↑ R_{ref} = 475 Ω			10	ns
t_{PZH}	Output enable time to high level	SEL$\overline{100}$/133	All outputs	SEL$\overline{100}$/133 ↑ R_{ref} = 475 Ω			10	
t_{PHZ}	Output disable time from high level	SEL$\overline{100}$/133	All outputs	SEL$\overline{100}$/133 ↓ R_{ref} = 475 Ω			10	
t_{PLZ}	Output disable time from low level	SEL$\overline{100}$/133	All outputs	SEL$\overline{100}$/133 ↓ R_{ref} = 475 Ω			10	
t_s	Stabilization time‡	V_{DD}	All outputs	After power up			0.1	ms
		$\overline{\text{PWRDWN}}$	All outputs	From $\overline{\text{PWRDWN}}$ ↑			0.25	ms

† These parameters are assured by design and lab characterization, not 100% production tested.

‡ Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time since V_{DD} achieves its nominal operating level (3.3 V) or $\overline{\text{PWRDWN}}$ transition from a low to a high level (2 V) until the output frequency is stable and operating within specification.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

HCLK/$\overline{\text{HCLK}}$ (Type X1), C_L = 2 pF, R_{ref} = 475 Ω, 6 x R_{ref}

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	HCLK clock period‡		$f_{(HCLK)}$ = 100 MHz		10		10.2	ns
			$f_{(HCLK)}$ = 133 MHz		7.5		7.65	
$T_{jit(cc)}$	Cycle-to-cycle jitter		$f_{(HCLK)}$ = 100 or 133 MHz	SSC off	−80		80	ps
				SSC on	−110		110	
t_{dc}	Duty cycle		$f_{(HCLK)}$ = 100 or 133 MHz, Crossing point		45%		55%	
$t_{sk(o)}$	HCLK bus skew		$f_{(HCLK)}$ = 100 or 133 MHz, Crossing point			70		ps
t_r	Rise time†	0.7-V amplitude	V_O = 0.14 V to 0.56 V		175		700	ps
t_f	Fall time†		V_O = 0.14 V to 0.56 V		175		700	
$v_{(cross)}$	Cross point voltages†	0.7-V amplitude	$f_{(HCLK)}$ = 100 or 133-MHz HCLK and $\overline{\text{HCLK}}$		45% V_{OH}		55% V_{OH}	V

† These parameters are assured by design and lab characterization, not 100% production tested.
‡ The average over any 1-µs period of time is greater than the minimum specified period.

CLK33 (Type 5), C_L = 30 pF, R_L = 500 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	PCI clock period†	$f_{(HCLK)}$ = 100 or 133 MHz	30	30.06	30.6	ns
$T_{jit(cc)}$	Cycle-to-cycle jitter	$f_{(HCLK)}$ = 100 or 133 MHz	−150		150	ps
$t_{(dc)}$	Duty cycle	$f_{(CLK33)}$ = 33.3 MHz	45%		55%	
t_r	Rise time	V_O = 0.4 V to 2.4 V	0.5		2	ns
t_f	Fall time	V_O = 0.4 V to 2.4 V	0.5		2	

† The average over any 1-µs period of time is greater than the minimum specified period.

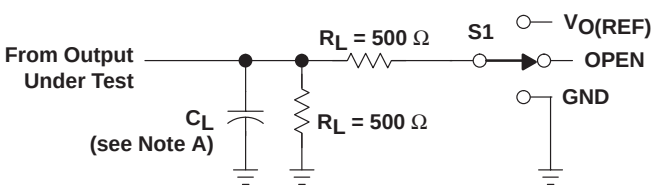
3V48 (Type 3), C_L = 20 pF, R_L = 500 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	3V48 clock period	$f_{(HCLK)}$ = 100 or 133 MHz		20.83		ns
$T_{jit(cc)}$	Cycle-to-cycle jitter	$f_{(HCLK)}$ = 100 or 133 MHz	−300		300	ps
t_{dc}	Duty cycle	$f_{(3V48)}$ = 48 MHz	45%		55%	
t_r	Rise time	V_O = 0.4 V to 2.4 V	1		4	ns
t_f	Fall time	V_O = 0.4 V to 2.4 V	1		4	

REF (Type 3), C_L = 20 pF, R_L = 500 Ω

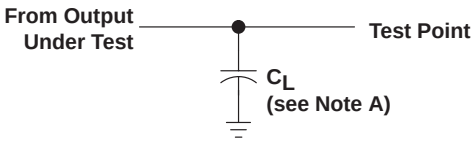
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	REF clock period	$f_{(REF)}$ = 14.318 MHz		69.84		ns
$T_{jit(cc)}$	Cycle-to-cycle jitter	$f_{(HCLK)}$ = 100 or 133 MHz	−0.5		0.5	
$t_{(dc)}$	Duty cycle	$f_{(REF)}$ = 14.318 MHz	45%		55%	
t_r	Rise time	V_O = 0.4 V to 2.4 V	1		4	ns
t_f	Fall time	V_O = 0.4 V to 2.4 V	1		4	

PARAMETER MEASUREMENT INFORMATION

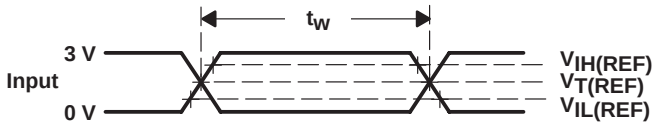


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $V_{O(REF)}$ GND

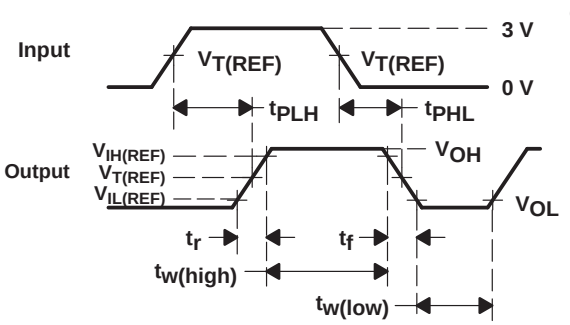
LOAD CIRCUIT For t_{pd} and t_{sk}

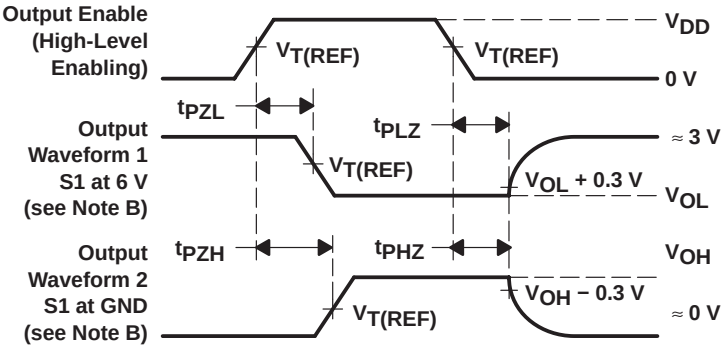


LOAD CIRCUIT for t_r and t_f



VOLTAGE WAVEFORMS





VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance. C_L = 2 pF (HCLK, $\overline{\text{HCLK}}$), C_L = 20 pF (48 MHz, REF), C_L = 30 pF (CLK33).
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

PARAMETER		3.3-V INTERFACE	UNIT
$V_{IH(REF)}$	High-level reference voltage	2.4	V
$V_{IL(REF)}$	Low-level reference voltage	0.4	
$V_{T(REF)}$	Input threshold reference voltage	1.5	
$V_{O(REF)}$	Off-state reference voltage	6	

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

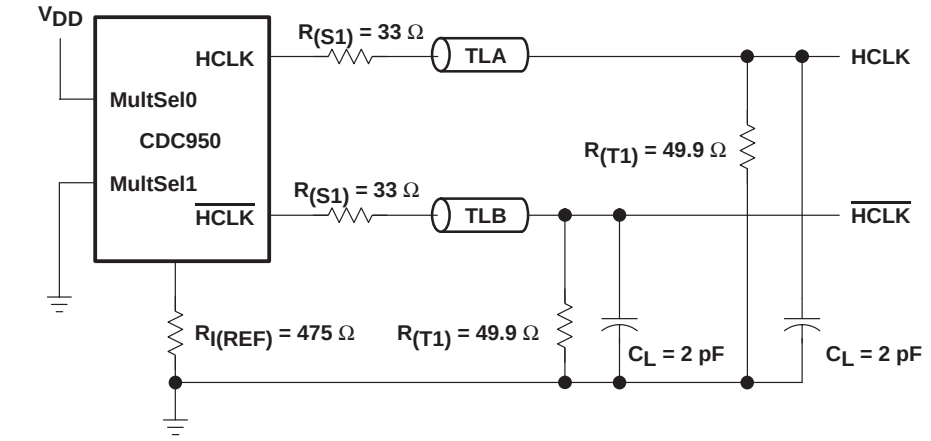


Figure 2. Load Circuit for HCLK Bus

spread spectrum clock (SSC) implementation for CDC950

Simultaneously switching at a fixed frequency generates a significant power peak at the selected frequency, which in turn causes EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL allows energy to be distributed to many different frequencies which reduces the power peak.

A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 3.

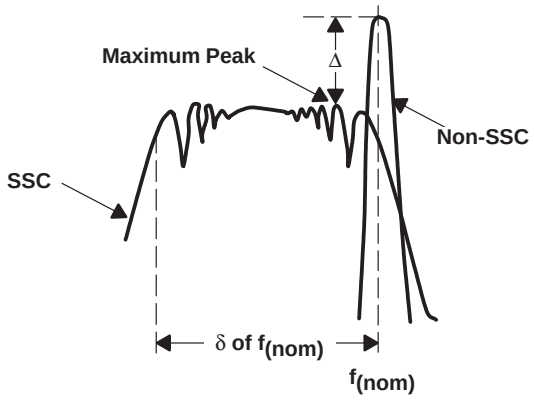


Figure 3. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution (left side) associated with the single-frequency spectrum which indicates a down-spread modulation.

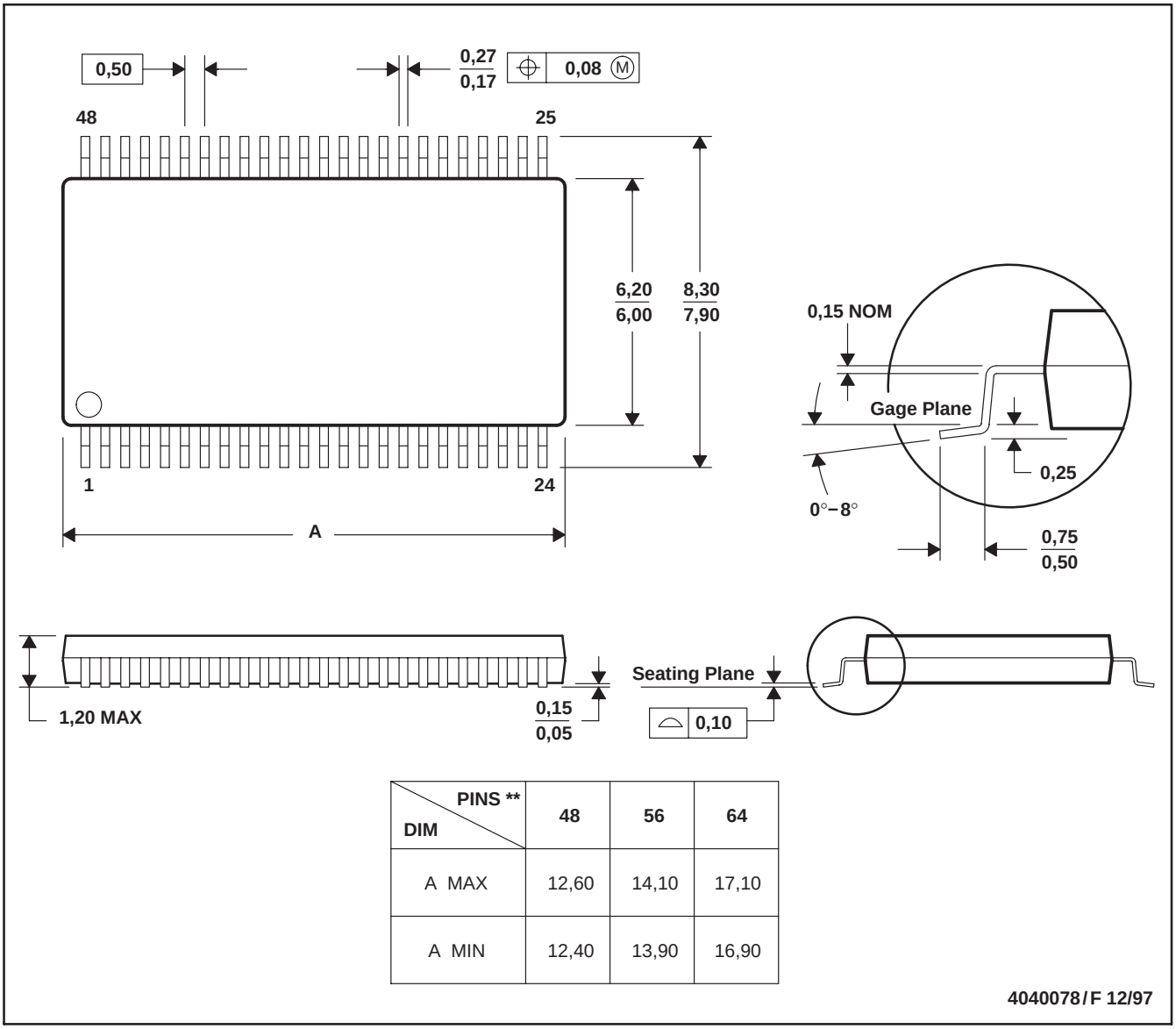
The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency close to its upper specification limit. The modulation amount was set to approximately –0.6%.

To allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The modulation frequency is approximately 31 kHz.

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265