SDLS103

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

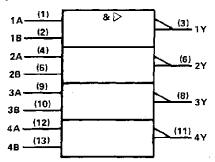
These devices contain four independent 2-input NAND buffer gates.

The SN5437, SN54LS37 and SN54S37 are characterized for operation over the full military range of -55 °C to 125 °C. The SN7437, SN74LS37 and SN74S37 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

INP	UTS	Ουτρυτ
A	B	Y
н	н	L
L	x	н
Х	L	Н

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

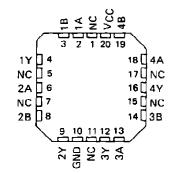
Pin numbers shown are for D, J, N, and W packages.

SN5437, SN54LS37, SN54S37, SN7437, SN74LS37, SN74S37 OUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS December 1983-Revised March 1988

> SN5437, SN54LS37, SN54S37.... J OR W PACKAGE SN7437.... N PACKAGE SN74LS37, SN74S37.... D OR N PACKAGE (TOP VIEW)

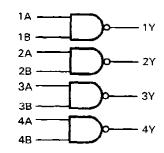
1A [] 1B []2 1Y []3 2A []4 2B []5	U 14 VCC 13 48 12 4A 11 4Y 10 3B
	10 3B
2Y 🗖 6	9 <mark>Д</mark> ЗА
GND [7	8] 3Y

SN54LS37, SN54S37 ... FK PACKAGE (TOP VIEW)



NC ~ No internal connection

logic diagram



positive logic

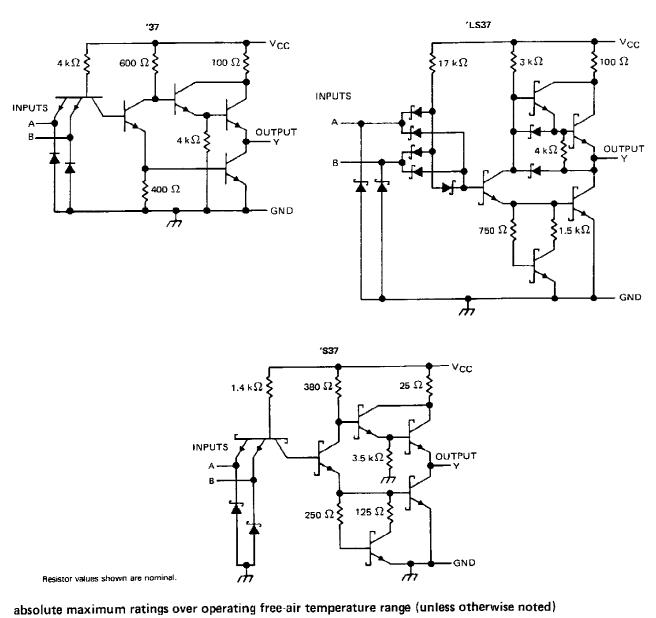
$$Y = \overline{A \cdot B}$$
 or $Y = \overline{A} + \overline{B}$

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard werrenty. Production processing does not necessarily include testing of all parameters.



SN5437, SN54LS37, SN437 SN7437, SN74LS37, SN7437 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

schematics (each gate)



)	
ʻ1 S37		
Operating free-air temperature:	\$N54'	
	SN74' ,	
Storage temperature range		

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN5437				UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH High-level input voltage		2			2			V
VIL Low-level input voltage			-	0.8			0.8	V
IOH High-level output current				- 1.2			- 1.2	mA
IOL Low-level output current				48			48	mΑ
TA Operating free-sir temperatu	re	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS T					Γ	SN7437	,	UNIT
PARAMETER	1	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT		
VIK	V _{CC} ≈ MIN,	l _l = – 12 mA				- 1.5	1		- 1.5	V
VOH	V _{CC} = MIN,	V _{IL} =0.8 V,	IOH = - 1.2 mA	2.4	3.3		2.4	3.3		V
VOL	VCC ~ MIN,	V _{IH} = 2 V,	loL = 48 mA		0.2	0.4		0.2	0.4	V
1	V _{CC} = MAX,	V ₁ = 6.5 V				1			1	mA
Тн	VCC = MAX,	V = 2.4 V				40	Γ		40	μA
ЧL	VCC = MAX,	V ₁ = 0.4 V				- 1.6	[- 1.6	mA
los§	V _{CC} = MAX			- 20		- 70	- 18	·	- 70	mA
ГССН	V _{CC} ≈ MAX,	V ₁ = 0 V			9	15.5	_	9	15.5	mA
ICCL	V _{CC} = MAX,	V ₁ = 4.5 V			34	54		34	54	mΑ

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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\$ All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$. \$ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25 $^{\circ}\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON					UNIT
tPLH	A or B	· · ·	R ₁ = 133 Ω,	C 45 pF		13	22	กร
TPHL	A 01 B	·	n 133 32,	C _L = 45 pF		8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



SN54LS37, SN74LS37 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

	SN54LS37 SN74LS37	UNIT
	MIN NOM MAX MIN NOM MAX	
V _{CC} Supply voitage	4.5 5 5.5 4.75 5 5.25	V
VIH High-level input voltage	2 2	
VIL Low-level input voltage	0.7 0.8	V
OH High-level output current	-1.2 -1.2	mA
OL Low-level output current	12 24	mA
T _A Operating free-air temperature	-55 125 0 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS T			N54LS3	37	S	N74LS	37	UNIT
FARAMETER		MIN	TYP‡	TYP‡ MAX		MIN TYP\$		UNIT		
٧IK	V _{CC} = MIN,	ŧι =18 mA			- 1.5]		- 1.5	v
V _{OH}	V _{CC} = MIN,	V _{IL} ≖ MAX,	юн = – 1.2 mA	2.5	3.4		2.7	3.4		V
Ve	V _{CC} = MIN,	V _{IH} = 2 V,	1 ₀₁ = 12 mA		0.25	0.4		0.25	0.4	v
Vol	V _{CC} = MIN,	V _{JH} = 2 V,	<u>lol = 24 mA</u>					0.35	0.5	<u> </u>
կ	V _{CC} = MAX,	V ₁ = 7 V				0.1			0.1	mΑ
ЧΗ	V _{CC} = MAX,	V _I ≠ 2.7 V				20			20	μA
μ	V _{CC} = MAX,	V ₁ = 0.4 V		_		- 0.4			- 0.4	mA
IOS §	V _{CC} = MAX			- 30		130	- 30		- 130	mA
Іссн_	VCC = MAX,	V1 = 0 V			0.9	2		0.9	2	mΑ
^I CCL	V _{CC} = MAX,	V _I = 4.5 V		_	6	12		6	12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

...

[‡] All typical values are at V_{CC} = 5 V, T_A = 25° C. § Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	MIN TYP	MAX	UNIT	
^t PLH	A or B	v	P 667 0		12	24	ns
^t PH∟	AOIB		R _L = 667 Ω,	CL = 45 pF	12	24	រាន

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



SN54S37, SN74S37 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

			SN54S37			SN74S37			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	- 5	5.25	V	
VIН	High-level input voltage	2			2		_	V	
VIL	Low-level input voltage			0.8			0.8	V	
юн	High-level output current			- 3			- 3	mA	
IOL.	Low-level output current			60			60	mA	
TA	Operating free-air temperature	- 55		125	0		70	°c	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS [†]	SN54S37	SN74S37	
PARAMETER	TEST CONDITIONS (ΜΙΝ ΤΥΡ‡ ΜΑΧ	MIN TYP: MAX	יואט ך
VIK	$V_{CC} = MIN, I_1 = -18 \text{ mA}$	- 1.2	- 1.2	V
VOH	$V_{CC} = MIN$, $V_{IL} = 0.8 V$, $l_{OH} = -3 mA$	2.5 3.4	2.7 3.4	V
VOL	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 60 mA	0.5	0.5	V
1	V _{CC} = MAX, VI = 5.5 V	1	1	mA
Чн	V _{CC} = MAX, V _I = 2.7 V	0.1	0.1	mΑ
11	V _{CC} = MAX, V _I = 0.5 V	-4	- 4	mA
los§	V _{CC} = MAX	- 50 - 225	- 50 - 225	mA
ГССН	$V_{CC} = MAX, V_1 = 0 V$	20 36	20 36	mA
ICCL	V _{CC} = MAX, V _I = 4.5	46 80	46 80	mA

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† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. ‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$. § Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 100 milliseconds.

FROM то PARAMETER TEST CONDITIONS UNIT MIN TYP MAX (INPUT) (OUTPUT) 4 6.5 ^tPLH ns C_L = 50 pF $R_{\rm L}$ = 93 Ω_{\star} 4 ^tPHL 6.5 ns Y A or B 6 ^tPLH ΠS $\mathsf{R}_{\mathsf{L}}=93~\Omega,$ C_L = 150 pF 6 [†]PHL ns

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$ (see note 2)

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.





17-Mar-2017

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-9754101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9754101Q2A SNJ54LS 37FK	Samples
5962-9754101QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QC A SNJ54LS37J	Samples
5962-9754101QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QC A SNJ54LS37J	Samples
5962-9754101QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QD A SNJ54LS37W	Samples
5962-9754101QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QD A SNJ54LS37W	Samples
SN54LS37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS37J	Samples
SN54LS37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS37J	Samples
SN54S37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S37J	Samples
SN54S37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S37J	Samples
SN74LS37N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS37N	Samples
SN74LS37N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS37N	Samples
SN74LS37NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS37N	Samples
SN74LS37NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS37N	Samples
SN74LS37NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS37	Samples
SN74LS37NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS37	Samples



PACKAGE OPTION ADDENDUM

17-Mar-2017

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S37D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	\$37	Samples
SN74S37D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S37	Samples
SN74S37N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S37N	Samples
SN74S37N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S37N	Samples
SNJ54LS37FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9754101Q2A SNJ54LS 37FK	Samples
SNJ54LS37FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9754101Q2A SNJ54LS 37FK	Samples
SNJ54LS37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QC A SNJ54LS37J	Samples
SNJ54LS37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type -55 to 12		5962-9754101QC A SNJ54LS37J	Samples
SNJ54LS37W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QD A SNJ54LS37W	Samples
SNJ54LS37W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754101QD A SNJ54LS37W	Samples
SNJ54S37FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 37FK	Samples
SNJ54S37FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 37FK	Samples
SNJ54S37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S37J	Samples
SNJ54S37J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S37J	Samples
SNJ54S37W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S37W	Samples



17-Mar-2017

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SNJ54S37W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S37W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS37, SN54S37, SN74LS37, SN74S37 :



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PACKAGE OPTION ADDENDUM

17-Mar-2017

• Catalog: SN74LS37, SN74S37

• Military: SN54LS37, SN54S37

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Texas Instruments





TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

 TAPE AND REEL INFORMATION

 *All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS37NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

14-Jul-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS37NSR	SO	NS	14	2000	367.0	367.0	38.0

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14



GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



J0014A

EXAMPLE BOARD LAYOUT

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE





D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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