GC1012B

3.3V DIGITAL TUNER CHIP

DATASHEET

October 2002

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

This datasheet is revised from the GC1012A datasheet to reflect the changes in the GC1012B replacement.

Revision	Date	Description
1.0	3 May 2002	First GC1012A datasheet. Major changes in specifications to reflect 3.3volt operation.
1.1	9 October 2002	Corrected checksum table, page 7

0.1 GC1012B TO GC1012A COMPARISON

The GC1012B is designed to be a functional and footprint compatible replacement for the GC1012A chip. The timing specifications for the GC1012B meet and exceed the timing specifications for the GC1012A. Electrically the GC1012B is a 3.3 volt only part, making it incompatible with the GC1012A's 5 volt mode. The GC1012B is fully compatible with the GC1012A's 3.3 volt mode, but at a lower power consumption. See Section 4 for timing and electrical specifications. NOTE: The GC1012B inputs are NOT 5 volt tolerant; chip damage may occur if the input voltages exceed Vcc + 0.5V (3.8 volts). Designs using the GC1012A at 5 volts will need to add a 3.3 volt supply and voltage level translators to use the GC1012B.

The function of the GC1012B has been slightly enhanced, but any enhancements are "backward" compatible with the GC1012A so that a GC1012A user will not need to change any software or processing algorithms to use the GC1012B chip. The checksums for the diagnostics have changed and are shown on page 7. Highlights of the enhancements follow.

0.1.1 Clock Loss Detect and Power Down Modes

The GC1012A chip used a slow internal clock to power down the chip or to put it into a low power mode if the clock is stopped. The slow clock has been removed in the GC1012B and replaced with a mode that will put the chip in a fully static mode if the clock has stopped. The fully static mode powers down the chip and reduces the power consumption down to a few microwatts until the clock resumes. The user can also force the power down state if desired. Two control bits (address 7 bit 5 and address 9 bit 7) are used to control the clock loss detect and power down modes. One control bit turns off the clock loss detect circuit, the other forces the power down mode. Both bits are cleared at power up to keep GC1012A compatibility.

See Section 1.9 for details.

0.1.2 Control Interface

The control interface has been enhanced to use either the R/$\overline{W}$ and $\overline{CS}$ strobes of the original GC1012A, or to use the $\overline{RE}$, $\overline{WE}$ and $\overline{CE}$ strobes used by most memory interfaces. If the $\overline{RE}$ pin is grounded, then the interface behaves in the R/$\overline{W}$ and $\overline{CS}$ mode, where the $\overline{WE}$ pin becomes the R/$\overline{W}$ pin and the $\overline{CE}$ pin becomes the $\overline{CS}$ pin. The $\overline{RE}$ pin on the GC1012B chip is a ground pin (pin 103) on the GC1012A chip, so that a GC1012B chip soldered into a GC1012A socket will automatically operate in the GC1012A R/$\overline{W}$ and $\overline{CS}$ mode.

See Section 1.3 for details.

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GC1012B DATASHEET

1.0 FUNCTIONAL DESCRIPTION

Fabricated in high speed CMOS technology, the GC1012B chip is an all digital tuner which can downconvert and band limit signals from wide band digitized sources. At full rate operation (100 MHz input rate), the input bandwidth can be up to 50 MHz wide. Any signal within the input bandwidth can be down-converted to zero frequency, low pass filtered, and output at a reduced sample rate. The chip's output can be formatted as either a complex data stream, or as a real data stream. The complex samples are output at rates equal to $F_O=F_{CK}/D$, where F_O is the output rate, D is 1, 2, 4, 8, 16, 32 or 64 and F_{CK} is the input sample (clock) rate. The real output rates are $F_O=2F_{CK}/D$ for D equal to 2, 4, 8, 16, 32, or 64.

The signal is low pass filtered to remove out of band energy before the sample rate is decreased. The filter's out of band rejection is over 75 dB and its passband ripple is less than 0.2 dB peak to peak. The passband of the output filter covers 80% of the output bandwidth.

The 28 bit accumulator in the chip's digital oscillator circuit provides a tuning accuracy equal to the input clock rate divided by 2^{28}. The tuning resolution at a clock rate of 50 MHz is less than 0.2 Hz giving a tuning accuracy of +/- 0.1 Hz. The phase noise in the oscillator is low enough to provide a spur free dynamic range of over 75 dB.

The chip's output circuit allows the user to select a real or complex data output format, to select spectral inversion, or to offset the output spectrum by half of the output sample rate. The output's signal gain can be adjusted in 0.03 dB steps. The word size of the output samples are either 10, 12, 14, or 16 bits.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 4 bit address port, read and write strobes, and a control select strobe.

I and Q output registers can be read from the control port to allow an external processor to monitor or process the chip's output samples. These registers are valuable for monitoring the chip's output power in order to set and adjust gain levels.

1.1 KEY FEATURES

- 100 million samples per second input rate
- 0.1 Hz tuning resolution
- >75 dB dynamic range
- Programmable output bandwidth
- 12 bit inputs, 10, 12, 14, or 16 bit outputs
- Real or complex output formats
- Built in strobe/sync generator
- Symmetric rounding used throughout
- Gain adjust in 0.03 dB steps
- Microprocessor interface for control, output, and diagnostics
- Power down mode
- Auto power down with clock loss detection
- Built in diagnostics
- 850 mW at 60 MHz, 3.3 volts
- 120 pin quad flat pack package

1.2 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

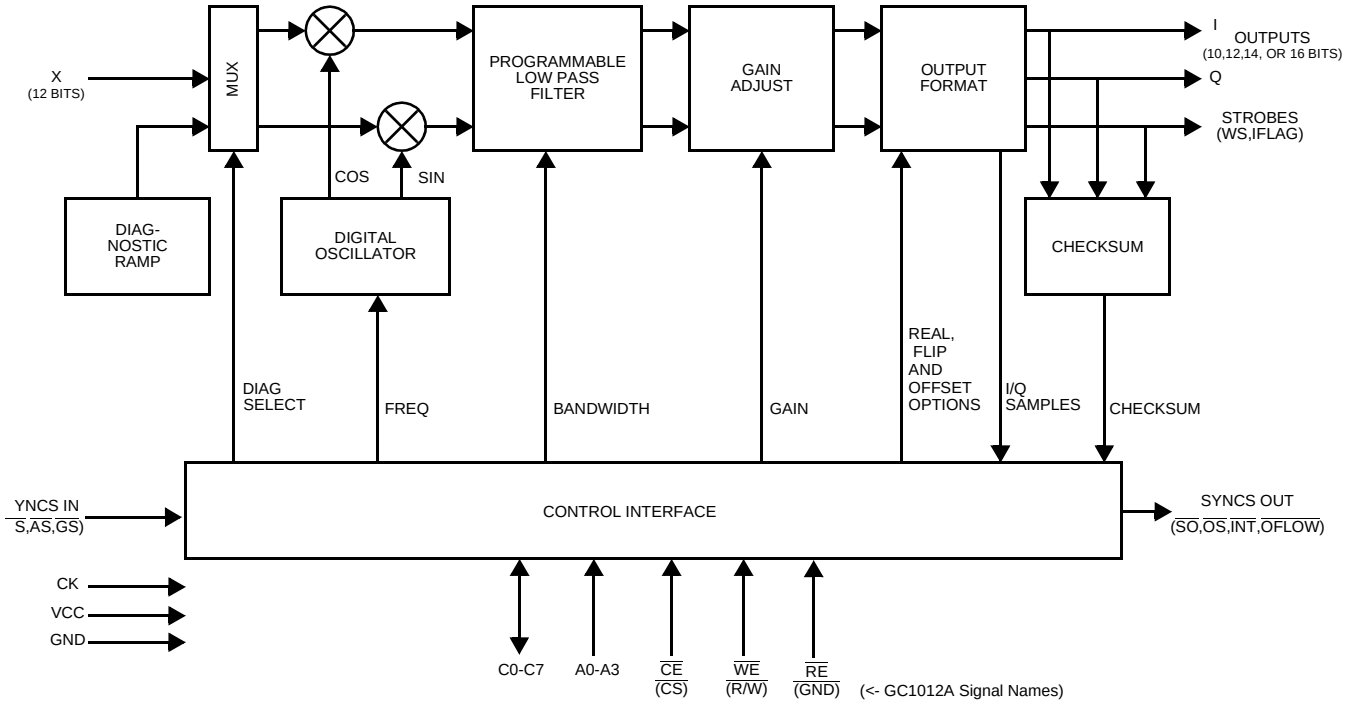


Figure 1. GC1012B Block Diagram

Each of these functions are described below.

1.3 CONTROL INTERFACE

The control interface performs four major functions: It allows an external processor to configure the chip, it allows an external processor to capture and read output samples from the chip, it allows an external processor to perform diagnostics, and it generates internal synchronization strobes.

The chip is configured by writing control information into 8 bit control registers within the chip. The contents of these control registers and how to use them are described in Section 3. The registers are written to or read from using the **C[0:7]**, **A[0:3]**, **$\overline{\text{WE}}$, $\overline{\text{RE}}$**, and **$\overline{\text{CE}}$** pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:3]** to the desired register address, setting the **$\overline{\text{CE}}$** pin low, setting **C[0:7]** to the desired value and then pulsing **$\overline{\text{WE}}$** low. **$\overline{\text{RE}}$** must remain high

To read from a control register the processor must set **A[0:3]** to the desired address, set **$\overline{\text{CE}}$** low, and then set **$\overline{\text{RE}}$** low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set **$\overline{\text{RE}}$** and **$\overline{\text{CE}}$** high. The **C[0:7]** pins are turned off (high impedance) whenever **$\overline{\text{CE}}$** is high or **$\overline{\text{WE}}$** is low.

The chip will only drive these pins when **$\overline{\text{CE}}$** is low and **$\overline{\text{RE}}$** is high. If RE is held low, then the interface will behave in the GC1012A mode, where **$\overline{\text{CE}}$** is **$\overline{\text{CS}}$**, and **$\overline{\text{WE}}$** is **R/$\overline{\text{W}}$**.

Control register addresses 12, 13, 14, and 15 are reserved to allow an external processor to read output samples from the chip. Addresses 12 and 13 are the I-registers which store the16 bit in-phase part of the output sample. Addresses 14 and 15 are the Q-registers which store the quadrature part. In the real mode the I registers store the even-time output samples and the Q registers store the odd-time output samples. Output ready and missed flags are provided in control register 9 in order to synchronize the storing and reading of the output samples. An interrupt output pin is also provided on the chip which can be used to interrupt the external processor when a new sample is ready. See the description of control register 9 in Section 3.6 for more details. The setup, hold and pulse width requirements for control read or write operations are given in Section 4.4.

Checksums are read from the chip during diagnostics using address 11. More details on the diagnostic modes is given in Section 1.11.

Address 10 is used to generate a one-shot pulse on the **$\overline{\text{OS}}$** output pin. This pulse can be used to synchronize the output timing and/or frequency oscillators of multiple GC1012B chips.

The control interface also generates the chip's internal sync strobes. The user may select to synchronize the chip using an external sync strobe (**$\overline{\text{SS}}$**), or use the chip's internal sync counter. The internal sync counter can be synchronized to **$\overline{\text{SS}}$**, or left to free run (See **SS_OFF** in Section 3.2). The period of the internal sync counter can be either 256 clocks or 2^{20} clocks. The 256 clock period is intended to be used for chip test purposes only. The internal sync counter is used during diagnostics to clear the data paths and strobe the checksum generator. The internal sync counter can also be used to periodically re-synchronize all of the counters in the chip during normal operating modes.

1.4 DIGITAL OSCILLATOR

The digital oscillator generates sine and cosine sequences which are used to mix the desired signal down to zero frequency. The digital oscillator contains a 28 bit frequency register, a 28 bit frequency accumulator, and a sine-cosine generator. The tuning frequency of the oscillator is set by loading a 28 bit frequency word from the control registers into the frequency register. If the frequency register is set to the word **FREQ**, then the tuning frequency will be: $\text{Frequency} = \frac{\text{Sample Rate}}{2^{28}}\textbf{FREQ}$. The tuning frequency should be set to the middle of the desired output bandwidth.

The frequency word **FREQ** is stored into the control registers at control addresses 0,1,2 and 3. The 28 bit word is then transferred into the frequency register using one of the following methods:

(1) The frequency register is always loading (the frequency changes immediately as the frequency word is loaded into the control registers).

(2) The frequency register is loaded when the user sets a control register bit.

(3) The frequency register is synchronously loaded when the accumulator sync strobe (**$\overline{\text{AS}}$**) goes low.

(4) The frequency register is synchronously loaded when the system sync strobe (**$\overline{\text{SS}}$**) goes low.

See Section 3.2 for more details on the frequency load modes.

The 28 bit frequency word is accumulated in the 28 bit frequency accumulator. The frequency accumulator will normally free run, but can be synchronously cleared by either the system sync (**$\overline{\text{SS}}$**) or the accumulator sync (**$\overline{\text{AS}}$**). The accumulator clear modes are controlled by bits in control register 4. See Section 3.2 for details.

The upper 13 frequency accumulator bits are used to generate the oscillator's sine and cosine outputs. These sines and cosines are generated to 12 bit accuracy. The oscillator's peak spur levels are below -75 dB.

1.5 MIXER

The mixer multiplies the 12 bit input samples by the 12 bit sine and cosine values coming from the digital oscillator. An input signal at the oscillator's tuning frequency will be centered at zero frequency after passing through the mixer. The mixer outputs are rounded to 13 bits using the "round-to-even" rounding algorithm. The "round-to-even" algorithm prevents a DC rounding bias by detecting fractions which are exactly equal to 0.5 and rounding them up half of the time and rounding them down half of the time. The choice to round up or down is made so as to always give an even result.

1.6 PROGRAMMABLE LOW PASS FILTER

The mixer's output is filtered using a programmable bandwidth low pass filter. The filter allows the output sample rate to be reduced by a factor of **D** = 2, 4, 8, 16, 32, or 64. The value of **D** is set using control register 5. The filter can be bypassed by setting **D** equal to 1. This allows the chip to be used as a mixer without any output filtering.

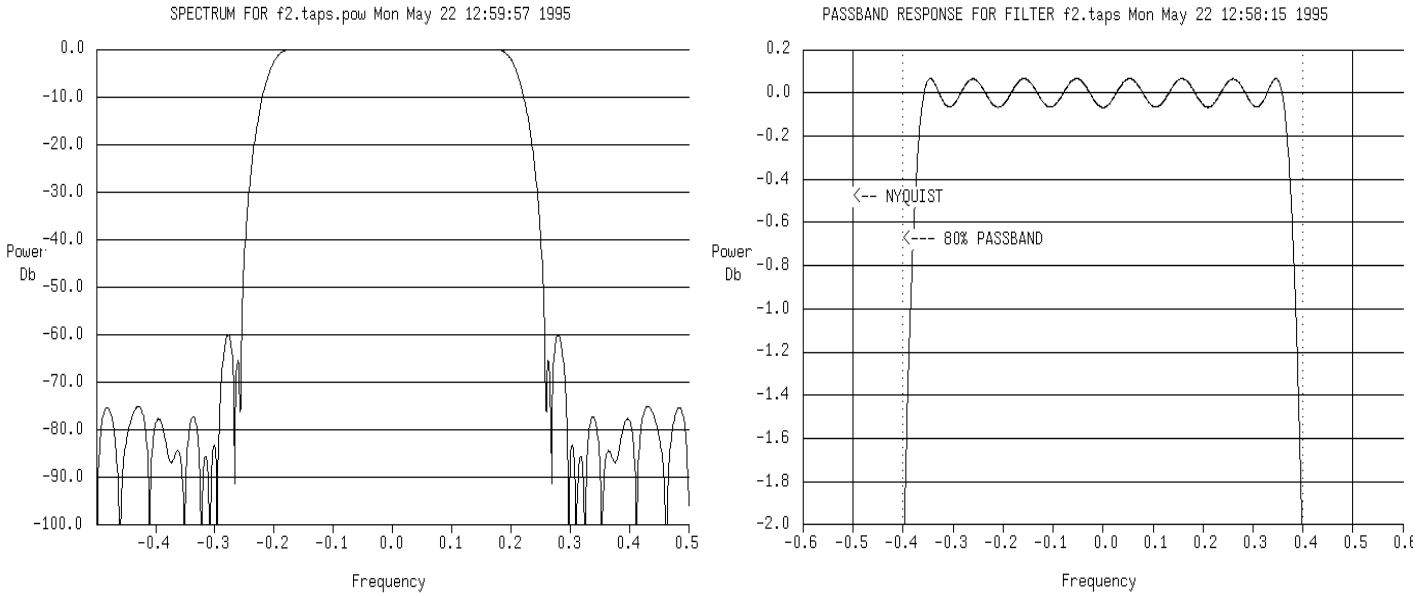
The low pass filter is a finite impulse response (FIR) filter with linear phase, 0.13 dB peak to peak ripple and over 75 dB of out of band rejection. The 2 dB output bandwidth is +/- $0.4F_S$ (80% usable bandwidth) where F_S is the complex output rate. The 0.1 dB bandwidth is +/- 0.36 F_S (72% usable bandwidth). The number of taps is equal to 20**D**.

The coefficients for the 40 tap decimate by 2 filter are:

```
-12     -42     -52     7       85      46      -110    -145    82      276
39      -396    -293    434     714     -273    -1400   -409    3115    6462
6462    3115    -409    -1400   -273    714     434     -293    -396    39
276     82      -145    -110    46      85      7       -52     -42     -12
```

The coefficients for the other filters are available from GRAYCHIP.

Figure 2 shows the spectral response of the decimate by 2 low pass filter. The decimate by 4, 8, 16, 32 and 64 filters are similar. Figure 2(a) shows the overall frequency response prior to decimation.Note that the filter rolls off quickly to 60 dB and is down below 75 dB in the region which aliases back into the passband. Figure 2(b) shows the 0.13 dB ripple in the passband.



(a) Overall (b) Passband

Figure 2. Filter Response

1.7 GAIN

The programmable bandwidth filter is followed by a gain circuit which adjusts the output level in 0.03 dB steps. The gain is controlled by the power of two gain value **S** and the fractional gain value **F**. The input to output gain of the chip is equal to $\mathbf{G} = 2^{(\mathbf{S}-B)}(1+\mathbf{F}/256)$, where **S** ranges from 0 to 15, **F** ranges from 0 to 255, and **B** is the base gain setting for each value of **D**. The base gain setting **B** gives a unity input to output gain for the chip, i.e., a 12 bit constant going into the chip will come out in the 12 MSBs of the 16 bit output word. The values of **B** are:

D	**B**
1	6
2	5
4	4
8	3
16	2
32	1
64	0

The **S** and **F** gain settings are double buffered so that they can be applied synchronously. A new gain setting takes effect either when **S** is loaded, or, if the GS_MODE control bit is used, when the $\overline{\mathbf{GS}}$ strobe is received.

The gain settings and GS_MODE bit are stored in control registers 6 and 7.

Overflow detection circuitry detects overflow conditions in the gain output words and saturates the samples to plus or minus full scale. Overflows are reported in the STATUS register and on the $\overline{\mathbf{OFLOW}}$ output pin. The overflow status can be used to detect if the gain settings are too high.

1.8 OUTPUT FORMATTING

The output format circuit allows the user to flip the output spectrum, to offset the spectrum by one-fourth the Nyquist rate, to convert the complex output stream to a real one at twice the rate, to round the samples to 10, 12, 14 or16 bits, and to multiplexes the I and Q samples together. These options are set using control register 8.

A word strobe (**WS**) is generated as an output clock signal. The **WS** strobe is either one clock cycle wide or is a 50% duty cycle clock. The polarity of **WS** is programmable.

The I and Q samples can be multiplexed together onto the I output pins by using the IQMUX mode. The **IFLAG** output pin is used in this mode to identify when the I words are being output. The **WS** strobe rate is doubled in this mode. The Q output pins are cleared in this mode.

Only the I output pins are used in the real mode. The Q pins are cleared. The output spectrum is centered from 0 to $F_O/2$ in the real mode. The spectrum is centered from $-F_O/2$ to $+F_O/2$ in the complex mode. The OFFSET control allows the spectrum to be centered from 0 to F_O.

The output format circuitry is synchronized by the $\overline{\textbf{SS}}$ input sync. This allows one to synchronize the output timing of multiple GC1012B chips.

1.9 POWER DOWN AND KEEPALIVE MODES

Unused chips in a system can be powered down by setting the POWER_DOWN control bit in register 9 (See Section 3.6). This reduces the internal clock rate down to 1 KHz to minimize the power consumed by the chip while still refreshing the internal dynamic nodes at a suitable rate.

The chip includes a “keepalive” circuit which detects when the clock has stopped for more than 2 milliseconds. The chip will automatically go into the power down mode if clock loss is detected. The keepalive detection circuit can be disabled by setting bit 5 in register 7 (See Section 3.4). NOTE: The chip will draw up to an Amp of current if the clock is stopped and the keepalive circuit is disabled.

1.10 THE ONE SHOT PULSE GENERATOR

The chip can generate a one-shot pulse which is output on the $\overline{\textbf{OS}}$ pin by writing to address 10. The pulse can be connected to the $\overline{\textbf{SS}}$, $\overline{\textbf{AS}}$, or $\overline{\textbf{GS}}$ sync input pins of GC1012B chips (including itself) to synchronize the output timing, frequency oscillators, or gain settings of multiple chips.

1.11 DIAGNOSTICS

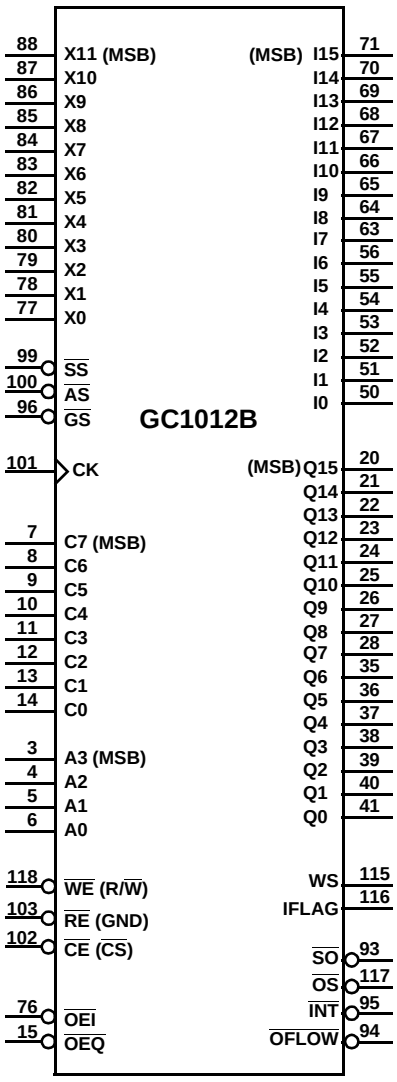
An input ramp generator, a sync period generator, and a checksum generator are provided on the chip in order to run diagnostic tests. Diagnostics are performed by turning on the ramp generator, enabling the diagnostic syncs, letting the chip operate for at least 4 sync periods, reading the checksum and comparing it to its predicted value. A new checksum is generated every sync period. The input ramp sequence is the same for every sync period and the chip is re-initialized at the beginning of each sync period so that each checksum should be the same once the chip's data path has been flushed. The chip requires at least 3 sync periods to flush, so the fourth and following checksums should be valid. The test is then repeated for several different tuning frequencies, decimation settings, and output modes.

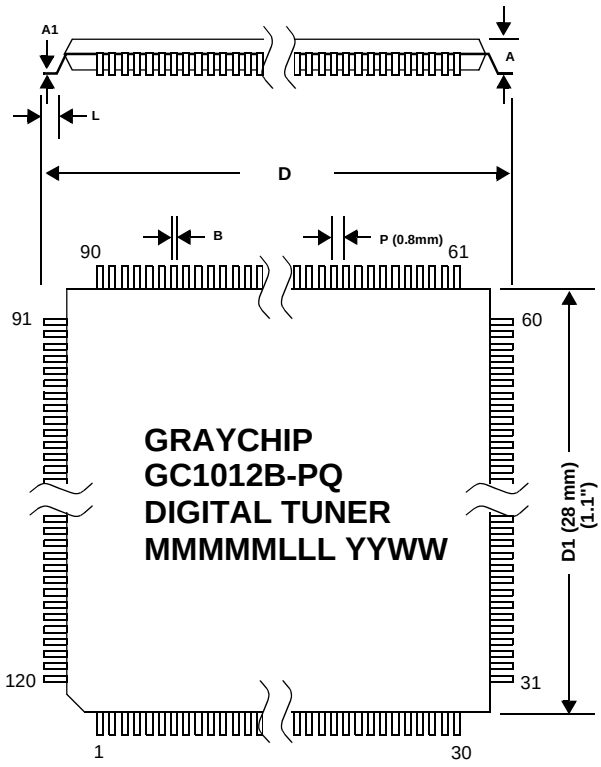
The sync period is 2^{20} clocks, or approximately 1 million clock cycles, so four sync periods will be about 4 million clocks. This represents a delay of less than 67 milliseconds for a clock rate of 60 MHz.

The following table lists the expected checksums for four test configurations. All values are in HEX.

CONTROL REGISTER	**TEST 1**	**TEST 2**	**TEST 3**	**TEST 4**
FREQ (REG 0,1,2,3)	0000101	0F0F0F0	55AA55A	AA55AA5
SYNC MODE (REG 4)	A9	A9	A9	A9
FILTER MODE (REG 5)	82	93	E4	D7
GAIN FRACTION (REG 6)	AA	55	00	FF
GAIN EXPONENT (REG 7)	5	4	3	0
OUTPUT (REG 8)	16	46	21	80
EXPECTED CHECKSUMS (REG 11)	C5	05	12	C9

2.0 PIN DESCRIPTIONS





120 PIN QUAD FLAT PACK PACKAGE

GC1012B-PQ = Enhanced Thermal Plastic Package

Package Markings: MMMMM = Mask Code
LLL = Lot Number
YYWW = Date Code

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	31.2 mm (1.228")	32.0 mm (1.260")
D1	(width body)	28.0 mm (1.102")	28.0 mm (1.102")
P	(pin pitch)	0.8 mm (0.031")	0.8 mm (0.031")
B	(pin width)	0.35 mm (0.014")	0.35 mm (0.014")
L	(leg length)	0.88 mm (0.035")	0.70 mm (0.028")
A	(height)	4.07 mm (0.160")	3.25 mm (0.128")
A1	(pin thickness)	0.17 mm (0.007")	0.2 mm (0.008")

VCC PINS: 2,16,17,29,32,33,43,44,47,48,58,59,62,74,75,89,91,97, 104,105,106,109,110,114,119

GND PINS: 1,18,19,30,31,34,42,45,46,49,57,60,61,72,73,90,92,98, 107,108,111,112,113,120

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

SIGNAL	DESCRIPTION
X[0:11]	**INPUT DATA.** *Active high* The 12 bit two's complement input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
CK	**CLOCK INPUT.** *Active high* The clock input to the chip. The **X**, **$\overline{SS}$**, **$\overline{GS}$** and **$\overline{AS}$** signals are clocked into the chip on the rising edge of this clock. The **I**, **Q**, **WS**, **IFLAG**, **$\overline{OS}$**, **$\overline{OFLOW}$** and **$\overline{SO}$** signals are clocked out on the rising edge of this clock.
$\overline{SS}$	**SYSTEM SYNC**. *Active low* The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{SS}$**. Bits in control register 4 (see Section 3.2) determine the operation of **$\overline{SS}$**. This sync is clocked into the chip on the rising edge of the clock.
$\overline{AS}$	**ACCUMULATOR SYNC**. *Active low* The accumulator sync is provided to synchronously change tuning frequencies. This sync can be used to load a new tuning frequency into the frequency register and/or to clear the frequency accumulator. This signal is clocked into the chip on the rising edge of the clock.
$\overline{GS}$	**GAIN SYNC**. *Active low* The gain sync is provided to synchronously change gain settings. This signal is clocked into the chip on the rising edge of the clock.
I[0:15]	**IN-PHASE OUTPUT DATA**. *Active high* The I part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEI}$	**IN-PHASE OUTPUT ENABLE**. *Active low* The **I[0:15]** output pins are put into a high impedance state when this pin is high.
Q[0:15]	**QUADRATURE OUTPUT DATA**. *Active high* The Q part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEQ}$	**QUADRATURE OUTPUT ENABLE**. *Active low* The **Q[0:15]** output pins are put into a high impedance state when this pin is high.
WS	**WORD STROBE**. *Programmable active high or low level* This strobe is output synchronous with the **I** and **Q** data words. The strobe occurs once per bit and is either one clock wide or has a 50% duty cycle. The high/low polarity of the strobe is programmable. See Section 3.5 for details.
IFLAG	**IN-PHASE STROBE**. *Active high* This strobe identifies the in-phase half of a complex pair when the outputs are in the IQ_MUX mode. See Section 3.5 for details. This signal is high when the I-half is output and is low when the Q-half is output.
$\overline{SO}$	**SYNC OUT**. *Active low* This signal is either a delayed version of the input system sync **$\overline{SS}$**, or, if SS_MUX in control register 4 is set, is the internally generated sync which has a period of 2^{20} clocks.
$\overline{INT}$	**INTERRUPT OUT**. *Active low* This signal is the READY flag from control register 9. This interrupt goes active when a new output sample is ready in control registers 12, 13, 14, and 15.
$\overline{OS}$	**ONE SHOT STROBE**. *Active low* This output is a one-shot sync strobe generated by writing to control address 10. The strobe is one clock cycle wide.
$\overline{OFLOW}$	**OVERFLOW FLAG**. *Active low* This signal goes low when an overflow is detected in the gain circuit. The signal will either pulse low for one clock cycle or will stay low depending upon the state of the OFLOW_MODE bit in control register 9.
C[0:7]	**CONTROL DATA I/O BUS**. *Active high* This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.
A[0:3]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the 16 control registers within the chip. Each of the 16 control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:3]** to the register's address.
$\overline{RE}$	**READ STROBE**. *Active low* The **$\overline{RE}$** strobe is used to read the control registers. Control register data is output when both **$\overline{RE}$** and **$\overline{CE}$** are low.
$\overline{WE}$	**WRITE STROBE.** *Active low* The **$\overline{WE}$** strobe is used to write the control registers. Control register data is written when both **$\overline{WE}$** and **$\overline{CE}$** are low.
$\overline{CE}$	**CHIP ENABLE**. *Active low* This control enables the read or write operation. The contents of the register selected by **A[0:3]** will be output on **C[0:7]** when **$\overline{RE}$** is low and **$\overline{CE}$** is low. If **$\overline{WE}$** is low when **$\overline{CE}$** goes low, then the selected register will be loaded with the contents of **C[0:7].**

3.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 16 eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{\text{CS}}$**, **$\overline{\text{WE}}$**, **$\overline{\text{RE}}$**, **A[0:3]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	FREQ byte 0	8	Output Mode
1	FREQ byte 1	9	Status
2	FREQ byte 2	10	One Shot
3	FREQ byte 3	11	Checksum
4	Sync mode	12	I-output byte 0
5	Filter mode	13	I-output byte 1
6	Gain Fraction	14	Q-output byte 0
7	Gain Exponent	15	Q-output byte 1

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

3.1 FREQUENCY WORD REGISTERS

Registers 0, 1, 2, and 3 contain the 28 bit frequency tuning word. Bit 0 is the LSB, bit 27 is the MSB.

ADDRESS 0: FREQUENCY BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[0:7]	Byte 0 (least significant) of frequency word

ADDRESS 1: FREQUENCY BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[8:15]	Byte 1 of frequency word

ADDRESS 2: FREQUENCY BYTE 2

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[16:23]	Byte 2 of frequency word

ADDRESS 3: FREQUENCY BYTE 3

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**FREQ**[24:27]	4 most significant bits of the frequency word
4-7	R/W	-	unused

If the desired tuning frequency is **F**, then the frequency word should be set to:

$$\mathbf{FREQ} = 2^{28}\mathbf{F}/(\text{clock rate})$$

3.2 SYNC MODE REGISTER

The sync mode register controls the action of the **$\overline{\text{SS}}$** and **$\overline{\text{AS}}$** sync strobes and how they affect the chip's internal timers, counters, and accumulators.

ADDRESS 4: Sync Mode Register

BIT	TYPE	NAME	DESCRIPTION
0 (LSB)	R/W	SS_OFF	This bit disables the **$\overline{\text{SS}}$** input.
1	R/W	AS_ON	Enables the accumulator sync **$\overline{\text{AS}}$**. Normally the frequency accumulator will free run. This bit causes the frequency accumulator to be initialized to the contents of the frequency register when **$\overline{\text{AS}}$** goes low. **$\overline{\text{SS}}$**, instead of **$\overline{\text{AS}}$**, will reset the accumulator if AS_MUX is set and **$\overline{\text{SS}}$** is not disabled by SS_OFF.
2	R/W	AS_MUX	Use **$\overline{\text{SS}}$** for the accumulator sync. The **$\overline{\text{AS}}$** input is ignored and the **$\overline{\text{SS}}$** strobe is used in its place when this bit is set and **$\overline{\text{SS}}$** is not disabled by SS_OFF. (See AS_ON and AS_FREQ).
3	R/W	LD_FREQ	Load the frequency register in the digital oscillator with the contents of the frequency word registers. If left on, this bit will cause the frequency register to load whenever a frequency word register is changed.
4	R/W	AS_FREQ	Enables the synchronous frequency load mode. When this bit is set and **$\overline{\text{AS}}$** goes low, the frequency register will be synchronously loaded with the contents of the frequency control registers. **$\overline{\text{SS}}$**, instead of **$\overline{\text{AS}}$**, will load the frequency register if AS_MUX is set and **$\overline{\text{SS}}$** is not disabled by SS_OFF.
5	R/W	SS_DIAG	Enables diagnostic syncs. This bit routes the internal sync to the checksum generator and to all accumulators and control counters within the chip. This forces the chip to re-initialize at the start of every sync period. The internal sync period will be 2^{20} clocks if SS_MUX is set, otherwise it will be determined by the period of an externally provided **$\overline{\text{SS}}$** strobe.
6	R/W	TEST	Shortens the internal sync counter period from 2^{20} clocks to 2^{8} clocks. This mode is used to test chips at the factory.
7 (MSB)	R/W	SS_MUX	Use the sync counter's terminal count strobe for the internal sync instead of the sync input **$\overline{\text{SS}}$**. The internal sync is output on the **$\overline{\text{SO}}$** pin.

The operation of these control bits are illustrated in Figure 3.

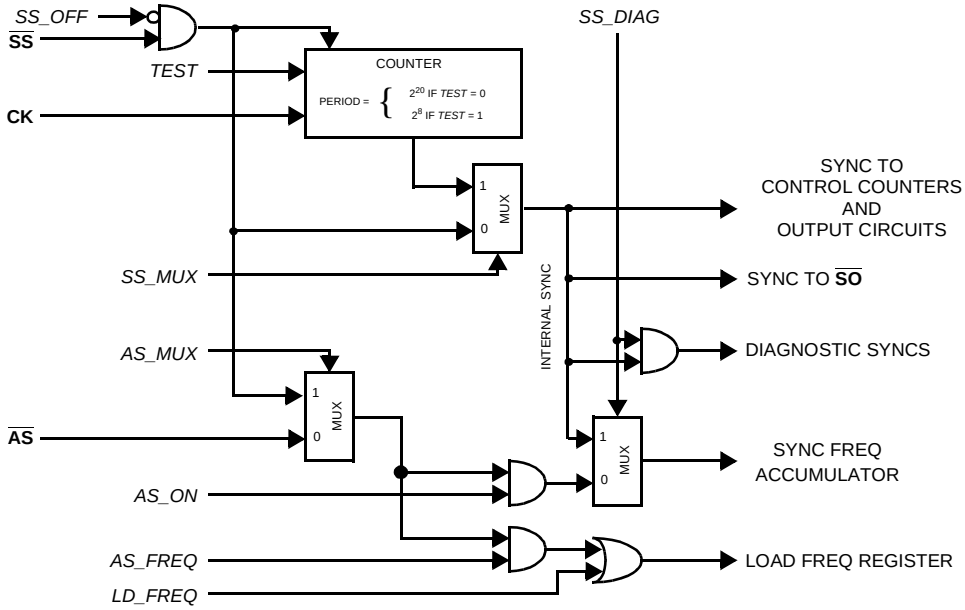


Figure 3. Sync Controls

3.3 FILTER MODE REGISTER

This register controls filtering, output formatting and the diagnostic input mode.

ADDRESS 5: Filter Mode Register

BIT	TYPE	NAME	DESCRIPTION
0-2	R/W	**DEC[0:2]**	The decimation mode. The output sample rate is set using **DEC** according to the following table:

	F_O **DECCOMPLEX** (REAL = 0)	F_O **REAL** (REAL = 1)
0 or 1	F_{CK}	?
2	$F_{CK}/2$	F_{CK}
3	$F_{CK}/4$	$F_{CK}/2$
4	$F_{CK}/8$	$F_{CK}/4$
5	$F_{CK}/16$	$F_{CK}/8$
6	$F_{CK}/32$	$F_{CK}/16$
7	$F_{CK}/64$	$F_{CK}/32$

Where F_{CK} is the input rate and F_O is the output rate.

3	R/W	-	Unused.
4	R/W	REAL	Output real samples instead of complex samples. The output spectrum is centered from 0 to $F_O/2$ where F_O is the output rate (see **DEC** above for the REAL mode). NOTE: The FLIP bit described below is active low in the real mode.
5	R/W	OFFSET	Offset the complex output spectrum. Used in the complex output mode (REAL=0) to force the output spectrum to be centered at $F_O/2$, where F_O is the output sample rate (see **DEC** above for the COMPLEX mode). This mode is useful for single-sideband AM signals because it moves the lower band edge up to zero frequency where it belongs. The upper half of the spectrum will appear as negative frequencies.
6	R/W	FLIP	Flip the output spectrum. This bit inverts the output spectrum. In the complex mode the spectrum is flipped about zero. In the real mode the spectrum is flipped about $F_O/4$, where F_O is the real mode's output sample rate. In the complex mode FLIP=1 flips the spectrum. In the real mode FLIP=0 flips the spectrum.
7	R/W	DIAG	Use the diagnostic ramp for the input to the chip instead of the **X** input. The ramp counts from -2048 to +2047 and then starts over again.

The effect on the output spectrum of the REAL, OFFSET and FLIP bits is illustrated in the following diagram. (F_O is the output sample rate)

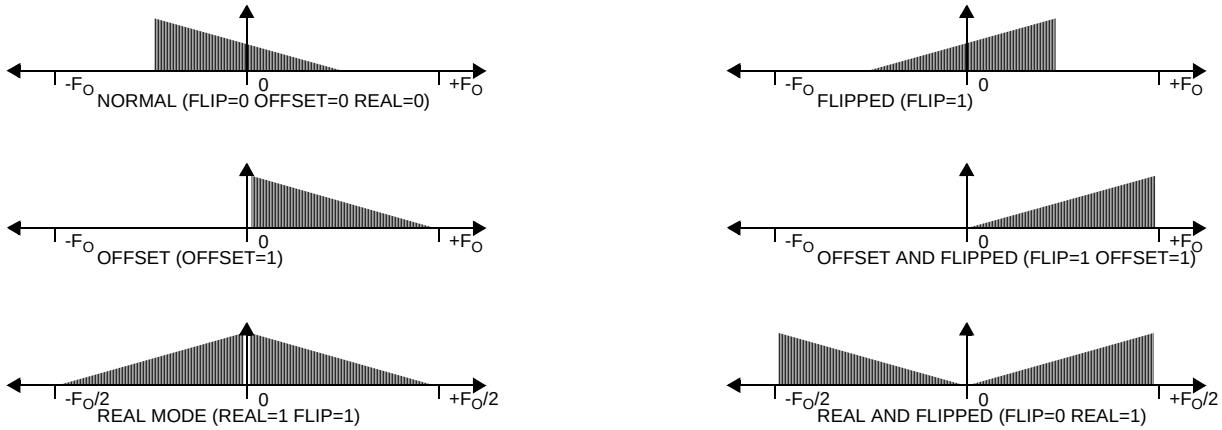


Figure 4. Output Spectral Formats

3.4 GAIN CONTROL REGISTERS

These registers set the output gain.

ADDRESS 6: Gain Control Register

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**F[0:7]**	The 8 bit gain fraction.

ADDRESS 7: Gain Exponent Register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**S[0:3]**	The 4 bit gain exponent.
4	R/W	GS_MODE	Turns on the synchronous gain mode. See below.
5	R/W	CKDET_DISABLE	Provided for testability. Turns off the clock loss detect function in the powerdown circuit. This bit powers up low and should be kept low.
6	R	-	unused
7	R	-	unused.

The chip's input to output gain is set using **F** and **S** according to the formula:

$$GAIN = 2^{(\mathbf{S}-\mathbf{B})}(1+\mathbf{F}/256)$$

where **B** is the base gain setting which is a function of the decimation mode of the chip. The unity gain setting (**S**=**B** and **F**=0) means that a 12 bit DC input will show up in the upper 12 bits of the 16 bit output.

The values of **B** are:

DEC	B
0 or 1	6
2	5
3	4
4	3
5	2
6	1
7	0

The GS_MODE control bit determines when new gain settings are applied to the output. New gain settings are double buffered so that they can be synchronized with the output words. If GS_MODE is low, then the gain settings are applied to the output samples immediately after **S** has been loaded. If GS_MODE is high, then the new gain settings are not used until $\overline{\mathbf{GS}}$ goes low.

NOTE: The gain settings must be loaded in the correct order- **F** first and then **S**. The circuit detects new gain settings by sensing when **S** is loaded. this means that **S** must be loaded even if one only wishes to change **F**.

3.5 OUTPUT MODE REGISTER

The output mode register controls the output formatting.

ADDRESS 8: Output mode register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	IQ_MUX	The IQ_MUX control is used in the complex mode to multiplex the I and Q output words onto the **I[0:15]** output pins. Normally the I and Q halves are output on separate ports. When this bit is high, the halves are multiplexed together so that the I half is output first, followed by the Q half. The word strobe (**WS**) rate is doubled in this mode. The **IFLAG** output signal is used in this mode to identify the I half of each complex pair. The **Q[0:15]** output pins are forced low in this mode.
1	R/W	WS_POL	Changes the polarity of **WS**.
2	R/W	WS_MODE	Changes the mode of **WS**. Normally **WS** pulses high during the clock cycle before an **I** or **Q** output transition. This bit changes **WS** so that it is a 50% duty cycle clock with its rising edge in the middle of each output period
3	R/W	-	Unused
4	R/W	R10	Round the output samples to the 10 bits MSBs of the output word.
5	R/W	R12	Round the output samples to the 12 bits MSBs of the output word.
6	R/W	R14	Round the output samples to the 14 bits MSBs of the output word.
7	R/W	R16	Round the output samples to the 16 bits MSBs of the output word.

One and only one of the rounding options should be selected. Unused LSBs are cleared.

The IQ_MUX and WS_MODE controls are illustrated in the timing diagrams shown in Figure 5. Note that the polarity shown for **WS** can be changed using the WS_POL control.

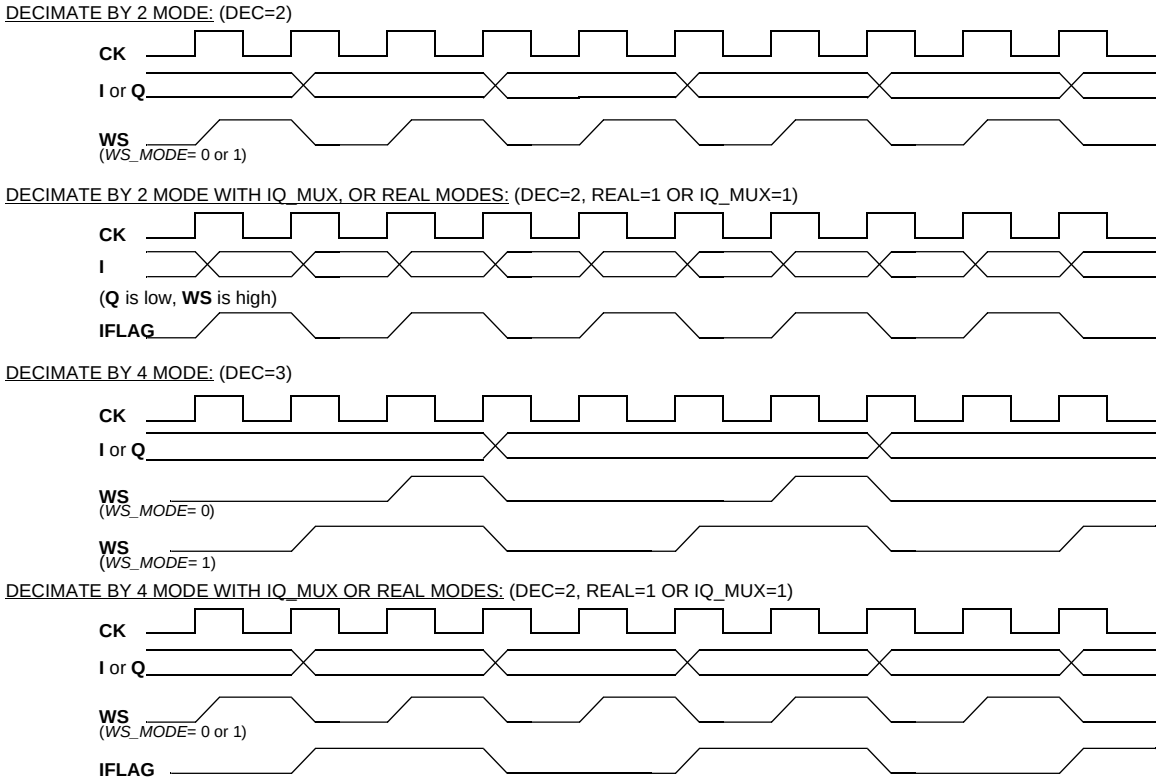


Figure 5. Timing For Output Modes

3.6 OUTPUT STATUS REGISTER

This register contains flags and status information for the output samples.

ADDRESS 9: Output Status Register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	READY	Tells the chip that the user is ready to capture an output sample. The chip clears this bit when it has captured the sample. See Notes below.
1	R/Clear	MISSED	The chip sets this bit high if a new output sample was ready but the user had not set READY high. This lets the user know if a sample has been missed. This bit is cleared by writing a 0 to the bit. Attempting to write a 1 to this bit does nothing.
2	R/W	INT_ENABLE	This bit is used to turn on the interrupt output. If this bit is off the **$\overline{\text{INT}}$** output pin is forced high. When this bit is high the **$\overline{\text{INT}}$** output pin is equal to READY. When READY goes low, meaning that a new sample has been captured, the **$\overline{\text{INT}}$** pin will go low. If **$\overline{\text{INT}}$** is tied to a processor's interrupt input, then the processor will be interrupted whenever a new sample is ready.
3	R/W	-	Unused
4	R/W	OFLOW_MODE	This bit sets the mode of the **$\overline{\text{OFLOW}}$** output. When OFLOW_MODE is low the **$\overline{\text{OFLOW}}$** output is an inverted version of OVERFLOW (see bit 6 below). If OFLOW_MODE and OFLOW_ENABLE are high, then the **$\overline{\text{OFLOW}}$** output pulses low for one clock cycle each time there is an overflow.
5	R/W	OFLOW_ENABLE	This bit enables the overflow modes. If this bit is low, then OVERFLOW (see bit 6 below) will not be set and the **$\overline{\text{OFLOW}}$** output will not go low. This bit does not affect the overflow detection and saturation logic in the gain circuit.
6	R/Clear	OVERFLOW	The chip sets this bit when an overflow occurs and OFLOW_ENABLE is turned on. This bit can be used to indicate if the gain is set too high. This bit stays high until the user clears it. The bit is cleared by writing a 0 to it. Attempting to write a 1 to this bit does nothing.
7	R/W	POWER_DOWN	This bit is used to put the chip into a power down (standby) mode. In this mode the chip is put into a static powerdown mode. All control register settings are preserved, but the output data will be invalid.

The READY signal is used to capture output samples and to read them into an external processor. The user captures outputs by setting the READY bit and then waiting for the bit to be cleared by the chip. When the bit goes low the processor can read the samples out of the I and Q output registers described in section 3.9. The processor can wait for READY to go low by either continuously reading this register, or it can use the interrupt output **$\overline{\text{INT}}$** to tell it when the sample is ready. To use the interrupt output mode the user must tie the **$\overline{\text{INT}}$** output pin from the chip to an interrupt input of the processor. The processor can then capture samples by setting READY and then setting INT_ENABLE (INT_ENABLE should be set after READY in order to avoid a spurious interrupt due to the interrupt being enabled before READY has settled to its high state). The processor will be interrupted when READY goes low again. When it is interrupted the processor can turn off INT_ENABLE, read the I/Q outputs, and then start over again.

The MISSED flag is provided to let the processor know if it has taken too long to read the I/Q samples before rearming the READY bit. If the processor wants to use the MISSED flag it should clear the flag the first time it sets the READY bit and then check it after setting the READY bit thereafter. The READY bit is set and the MISSED bit cleared by writing a 01(hex) to this register. The READY bit is set and the MISSED bit is left alone by writing a 03(hex) to this register.

NOTE: The READY bit will not be cleared if the sample is captured while the user is setting the READY bit. This will cause the READY bit to stay high after the output is captured and will not allow the chip to capture any more samples until the bit is cleared and set again. The user can detect this incorrect "ready" state by always clearing the MISSED bit when setting the READY bit. The incorrect state is detected if MISSED goes high when READY is high. The work-around to guarantee capturing an output sample is to always clear READY before setting it.

3.7 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 10. This is a write-only address and the data written to it is irrelevant.

ADDRESS 10: ONE SHOT

3.8 CHECKSUM REGISTER

This read-only register stores the checksums generated in the diagnostic mode.

ADDRESS 11: CHECKSUM

BIT	TYPE	NAME	DESCRIPTION
0-7	R	CHECK[0:7]	The 8 bit checksum. The checksum is generated as a non-linear feedback accumulation of the **BS**, **FS**, **I**, and **Q** output bits. The current checksum is stored in this register and the checksum generator is cleared whenever the internal sync goes low (see SS_MUX in Section 3.2 for the modes of the internal sync).

3.9 I AND Q OUTPUT REGISTERS

These registers are used to capture output samples.

ADDRESS 12: I-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[0:7]**	Least significant 8 bits of the **I** output.

ADDRESS 13: I-Output Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[8:15]**	Most significant 8 bits of the **I** output.

ADDRESS 14: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**Q[0:7]**	Least significant 8 bits of the **Q** output.

ADDRESS 15: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**QI[8:15]**	Most significant 8 bits of the **Q** output.

The user reads the **I** and **Q** outputs through these read-only registers. The captured samples can be used for gain control, analysis, display, or diagnostics.

4.0 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	4.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	°C	
Lead Soldering Temperature (10 seconds)			300	°C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the clock loss detect circuit will power down the chip. If the clock loss detect circuit is disabled (bit 5, address 7) and the clock is stopped, the chip may draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

4.2 RECOMMENDED OPERATING CONDITIONS

Table 2: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	3.6	V	
Temperature Ambient, no air flow	T_A	-40	+85	°C	1
Junction Temperature	T_J		125	°C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

4.3 THERMAL CHARACTERISTICS

Table 3: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC1012B-PQ			UNITS
		2 Watts	4 Watts	6 Watts	
Theta Junction to Ambient	θja	18	11	10	°C/W
Theta Junction to Case	θjc	4	4	4	°C/W

Note: Air flow will reduce **θja** and is highly recommended.

4.4 DC CHARACTERISTICS

All parameters are industrial temperature range of 0 to 85 ^{o}C ambient unless noted.:

Table 4: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	1
Voltage input high	V_{IH}	2.0		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1
Control data capacitance (**C[0:15]** I/O pins)	C_{CON}	Typical 6		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.

4.5 AC CHARACTERISTICS

Table 5: AC Characteristics (0 TO +85^{o}C Ambient, unless noted)

PARAMETER	SYMBOL	3.3V +/- 5%		UNITS	NOTES
		MIN	MAX		
Clock Frequency	F_{CK}	0.01	100	MHz	2, 3, 4
Clock low period (Below V_{IL})	t_{CKL}	4		ns	1
Clock high period (Above V_{IH})	t_{CKH}	4		ns	1
Data setup before **CK** goes high (**X, SS, AS** or **GS**)	t_{SU}	4		ns	1
Data hold time after **CK** goes high	t_{HD}	2		ns	1
Data output delay from rising edge of **CK**. (**I, Q, WS, IFLAG, OS, OFLOW, SO**	t_{DLY}	0	8	ns	1, 5
Data to tristate delay (**I** or **Q** to hiZ from **OEI** or **OEQ**)	t_{DZ}	2	5		1
Tristate to data output delay (**I** or **Q** valid from **OEI** or **OEQ**)	t_{ZD}	3	8	ns	1, 5
Control Setup before **CS** goes low (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CSU}	5		ns	1
Control hold after **CS** goes high (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CHD}	5		ns	1
Control strobe (**CS**) pulse width (Write operation)	t_{CSPW}	20		ns	1,6
Control output delay **CS** low to **C** (Read Operation)	t_{CDLY}		20	ns	1,6
Control tristate delay after **CS** goes high	t_{CZ}		5	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz)	I_{CCQ}		200	uA	1
Supply current (F_{CK} =100MHz)	I_{CC}		400	mA	1, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 85 deg C for the given specification.
3. Temperature range is verified by lot sampling.
4. The chip may not operate properly at clock frequencies below MIN and MAX.
5. Current load is 2ma. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or Falling below V_{IL}.
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{5}\right)\left(\frac{F_{CK}}{100M}\right)400mA$

5.0 APPLICATION NOTES

5.1 POWER AND GROUND CONNECTIONS

The GC1012B chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC1012B chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC1012B chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC1012B chip may not operate properly if these power and ground guidelines are violated.

5.2 STATIC SENSITIVE DEVICE

The GC1012B chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

5.3 100 MHZ OPERATION

Care must be taken in generating the clock when operating the GC1012B chip at its full 100 MHz clock rate. The user must insure that the clock is above 2 volts for at least 4 nanoseconds and is below 0.8 volts for at least 4 nanoseconds. At 1000 MHz the clock period is only 10 nanoseconds so that the clock must have a duty cycle of exactly 50%, and the rise and fall times can only be 1 nanosecond each. One must also be careful to prevent clock undershoot below ground. An ideal clock at 100 MHz would be a square wave with a low voltage of 0.5 volts and a high voltage of 2.5 volts.

5.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC1012B chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements. When operating at a reduced voltage, GRAYCHIP recommends driving the GC1012B chip inputs with 5 volt to 3 volt interface chips.

5.5 SYNCHRONIZING MULTIPLE GC1012B CHIPS

A system containing a bank of GC1012B chips will need to be synchronized so that the output frames from each chip are aligned, and, if desired, so that their frequency accumulators are running synchronously. The GC1000 Input Switch chip has built in sync counters which are designed specifically for this purpose. If the GC1000 chip is not used, then the one-shot strobe (see Section 3.7) can be used. The bank of chips should be interconnected so that the **$\overline{\text{OS}}$** pin of one GC1012B chip is tied to the **$\overline{\text{SS}}$** input of all of the chips. The one-shot strobe mode can then be used to simultaneously synchronize all of the chips. The **$\overline{\text{OS}}$** pin of a second GC1012B chip should be tied to the **$\overline{\text{AS}}$** input of all of the chips. The one-shot mode of the second chip can be used to synchronize the frequency accumulators whenever the tuning frequency has been changed.

5.6 PROCESSING COMPLEX DATA

Two GC1012B chips can be used to process complex input data by using one chip to process the I-input data and the other to process the Q-input data. If the two chips are synchronized as discussed above, then the complex output stream can be reconstructed by adding and subtracting the I and Q outputs of the two chips. A programmable gate array chip such as from XILINX would be ideal for this post-processing. The configuration for processing complex data is illustrated in Figure 6.

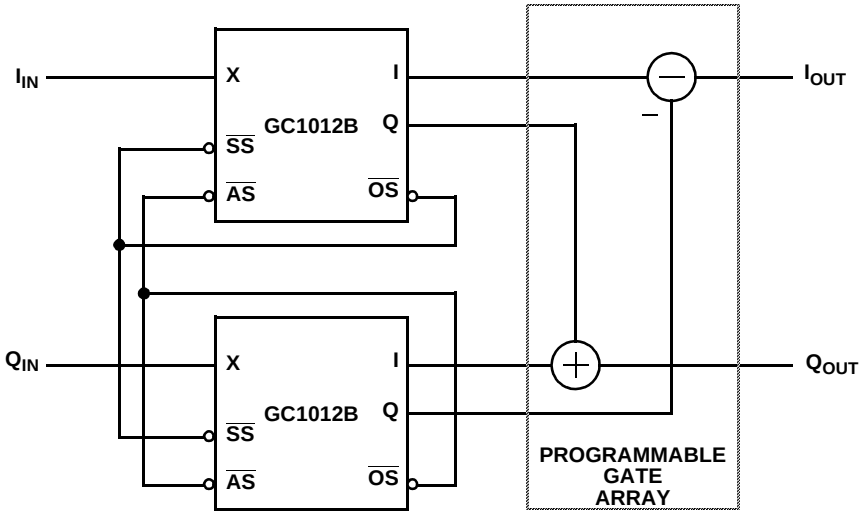


Figure 6. Processing Complex Input Data

5.7 EXAMPLE RECEIVER ARCHITECTURE

An example digital receiver architecture using the GC1012B chip is shown in Figure 7.

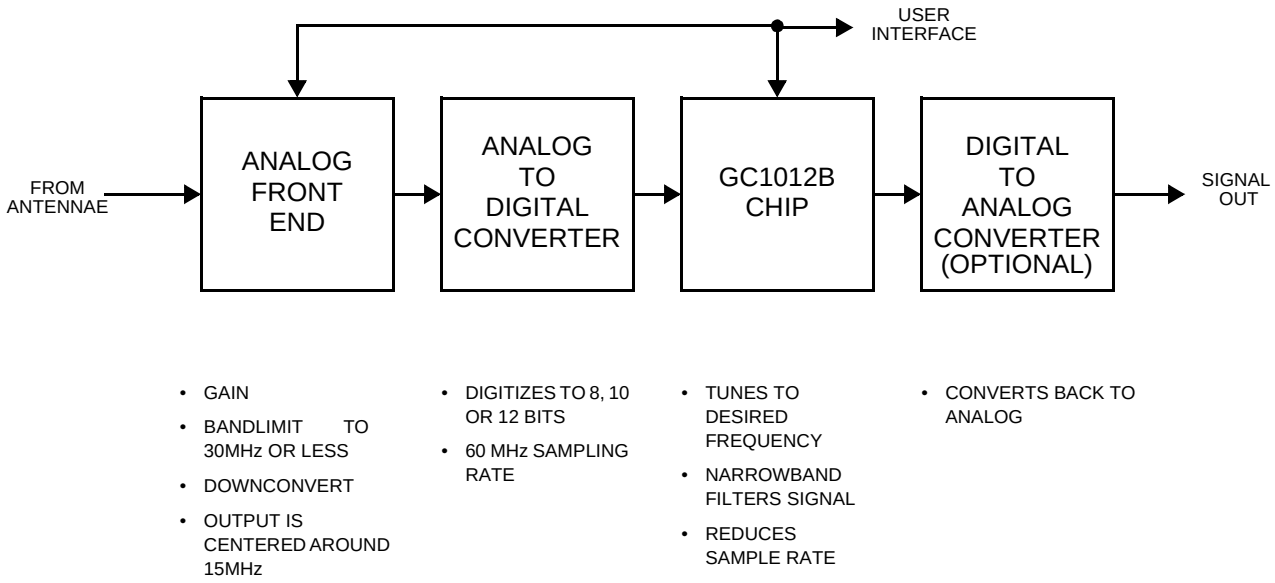


Figure 7. Example Digital Receiver Architecture

The receiver contains an analog front end which downconverts up to 30MHz of radio spectrum to an IF frequency around 15MHz[1]. It also adjusts the gain of the signal so that it fills the dynamic range of the analog to digital converter (ADC). The ADC digitizes the signal using up to 12 bits of resolution at a sampling rate up to 60 MHZ. The GC1012B chip tunes, downconverts, and narrowband filters desired frequencies from within the 30 MHz band. The GC1012B output can either be converted back to analog or kept in its digital state for subsequent signal processing.

1. Note that the HF spectrum (1 to 30MHz) can be digitized directly.

5.8 LATENCY THROUGH THE GC1012B

Two latencies are of interest, the latency from a step function in to a step function out (midpoint), and the latency from a step function until the end of the “ringing” in the step function output (endpoint). These latencies are:

Table 6: Latency

Output Mode	Midpoint	Endpoint	Values of D (decimation)
Real	41 + 20D	41 + 40D	1, 2, 4, 8, 16 and 32
Complex	35 + 10D	35 + 20D	2, 4, 8, 16, 32 and 64

Another latency of interest is the delay from SS input to stable WS. The WS strobe becomes stable and is low after 9 clocks, before 9 clocks the WS is unknown and may go high at any time. The delay until the first valid high WS is a function of decimation. For decimate by 2 the delay from SS is 10 clocks, for 4 the delay is 12 clocks, for 8 the delay is 16 clocks and for decimation ratios of 16, 32 and 64 the delay is 24 clocks. WS is high at clock 24 for all decimations.

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